128M X 72 Bit (1GB) 240-Pin DDR2 Registered RDIMM ECC (PC2-3200) Very Low Profile (VLP) 1 Rank x 4; RoHS Compliant

GENERAL DESCRIPTION

The SL72P4M128M8M-B05AY(W)U is a 128M x 72 bit (1GB) 240-pin Double Data Rate 2 (DDR2) Registered Dual In-line Memory Module (RDIMM) with ECC.

The module consists of eighteen CMOS 32M x 4 bit x 4 bank DDR2 SDRAMs in lead-free BGA packages mounted in 1 rank on a 240-pin glass epoxy substrate. The user has the option of choosing industrial temperature rated SDRAM components.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors are mounted across the power supply.

Damping resistors are added in series for DQ, DQS, and DM signals. A PLL supplies clocks to the DDR2 SDRAMs from one clock input.

All control and address signals are re-driven through registers to the DDR2 SDRAM devices. The control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

The module has gold edge connections and is intended for mounting into 240-pin RDIMM edge connector sockets keyed for 1.8V.

FEATURES

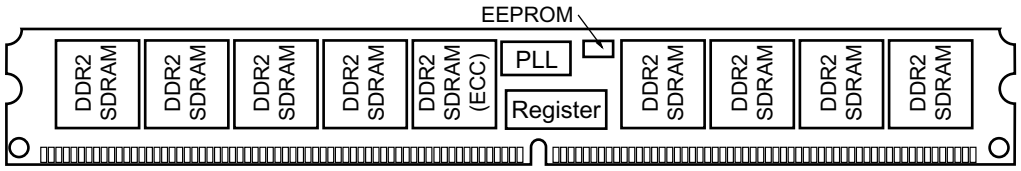
- PC2-3200 Compliant (DDR2-400 200MHz-5ns@CL-t_{RCD}-t_{RP}: 3-3-3)
- 240-Pin RDIMM form factor
- Industrial operating temperature option: (W) = -40°C to 95°C (Ambient)
- Average Refesh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE < 95°C
- VDD=VDDQ=1.8V ± 0.1V
- VDDSPD=1.7V to 3.6V JEDEC standard 1.8V I/O (SSTL_18 compatible)
- DDR2 architecture: Two data accesses per clock cycle, differential clock inputs (CK, /CK), bi-directional differential data strobe (DQS, /DQS), Off-Chip Driver (OCD) Impedance Adjustment, On Die Termination (ODT), On Chip Delay Locked Loop (DLL); four-bit prefetch architecture
- Commands entered on each rising CK edge; DQS-edge aligned with data for READs and center-aligned with data for WRITES; DLL to align DQ and DQS transitions with CK
- Four internal component banks for concurrent operation
- Concurrent Auto Precharge option is supported
- Data Mask (DM) for masking write data
- Programmable Burst lengths: 4, 8
- Programmable /CAS Latency (CL): 3, 4, 5
- Posted /CAS Additive Latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency-1 tCK
- READ burst interrupt supported by another READ; WRITE burst interrupt supported by another WRITE
- Adjustable data-output drive strength
- Serial Presence Detect (SPD) with EEPROM
- ECC, 1-bit error detection and correction
- Gold Edge contacts
- RoHS Compliant, lead free

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72P4M128M8M-B05AY(W)U	3	200	3.2 GB/s

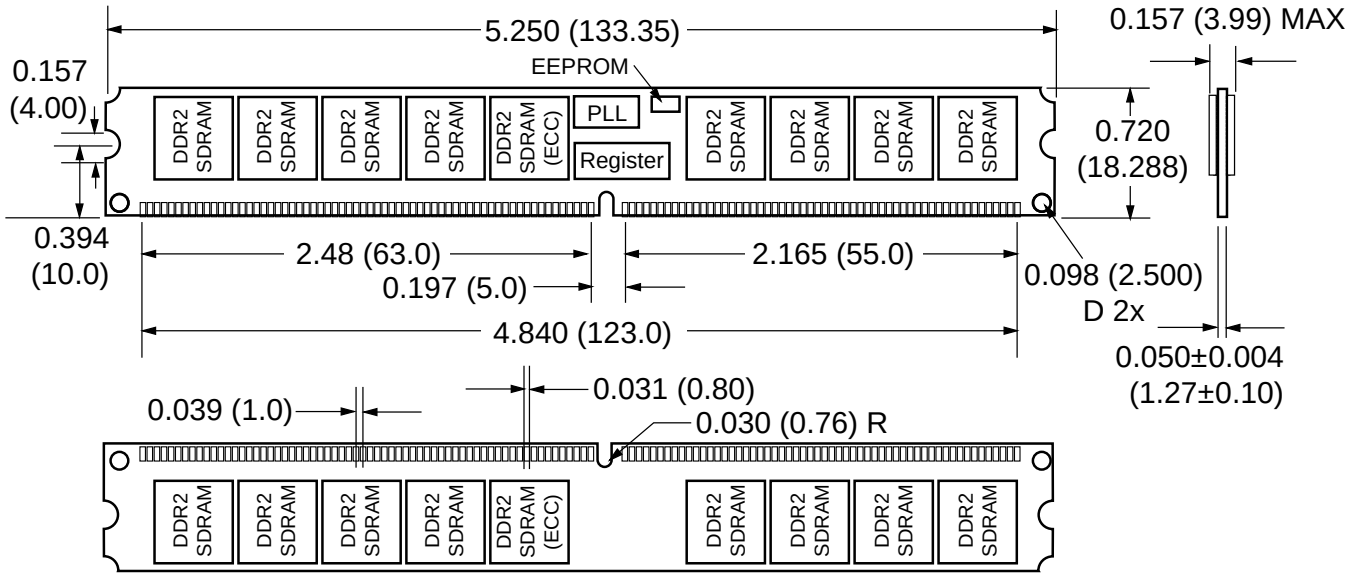
Note: Adding the second (W) to the part number selects the module with industrial temperature rated components.

240-PIN RDIMM ILLUSTRATION



DIMENSIONS *(Board No. 1235)*

Units are in inches (millimeters). All dimensions are typical unless otherwise specified.



PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Line** = **Key**)

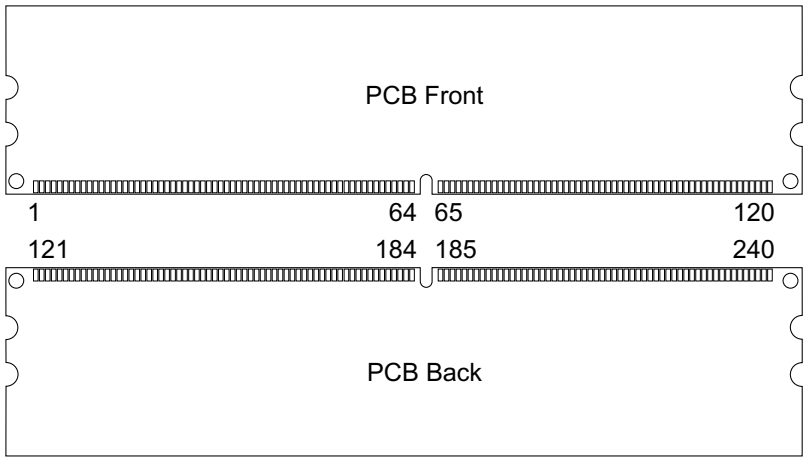
240-Pin DIMM Front Pinout

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS
2	VSS	32	VSS	62	VDDQ	92	/DQS5
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	VSS
5	VSS	35	VSS	65	VSS	95	DQ42
6	/DQS0	36	/DQS3	66	VSS	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	VSS
8	VSS	38	VSS	68	PAR-IN	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	VSS
11	VSS	41	VSS	71	BA0	101	SA2
12	DQ8	42	CB0	72	VDDQ	102	NC
13	DQ9	43	CB1	73	/WE	103	VSS
14	VSS	44	VSS	74	/CAS	104	/DQS6
15	/DQS1	45	/DQS8	75	VDDQ	105	DQS6
16	DQS1	46	DQS8	76	/S1*	106	VSS
17	VSS	47	VSS	77	ODT1*	107	DQ50
18	/RESET	48	CB2	78	VDDQ	108	DQ51
19	NC	49	CB3	79	VSS	109	VSS
20	VSS	50	VSS	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	VSS	112	VSS
23	VSS	53	VDD	83	/DQS4	113	/DQS7
24	DQ16	54	BA2	84	DQS4	114	DQS7
25	DQ17	55	ERR-OUT	85	VSS	115	VSS
26	VSS	56	VDDQ	86	DQ34	116	DQ58
27	/DQS2	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	VSS	118	VSS
29	VSS	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

240-Pin DIMM Back Pinout

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	VDDQ	211	DQS14
122	DQ4	152	DQ28	182	A3	212	/DQS14
123	DQ5	153	DQ29	183	A1	213	VSS
124	VSS	154	VSS	184	VDD	214	DQ46
125	DQS9	155	DQS12	185	CK0	215	DQ47
126	/DQS9	156	/DQS12	186	/CK0	216	VSS
127	VSS	157	VSS	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	VSS
130	VSS	160	VSS	190	BA1	220	RFU
131	DQ12	161	CB4	191	VDDQ	221	RFU
132	DQ13	162	CB5	192	/RAS	222	VSS
133	VSS	163	VSS	193	/S0	223	DQS15
134	DQS10	164	DQS17	194	VDDQ	224	/DQS15
135	/DQS10	165	/DQS17	195	ODT0	225	VSS
136	VSS	166	VSS	196	A13	226	DQ54
137	RFU	167	CB6	197	VDD	227	DQ55
138	RFU	168	CB7	198	VSS	228	VSS
139	VSS	169	VSS	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	CKE1*	201	VSS	231	VSS
142	VSS	172	VDD	202	DQS13	232	DQS16
143	DQ20	173	NC	203	/DQS13	233	/DQS16
144	DQ21	174	NC	204	VSS	234	VSS
145	VSS	175	VDDQ	205	DQ38	235	DQ62
146	DQS11	176	A12	206	DQ39	236	DQ63
147	/DQS11	177	A9	207	VSS	237	VSS
148	VSS	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	VSS	240	SA1

Pin Locations



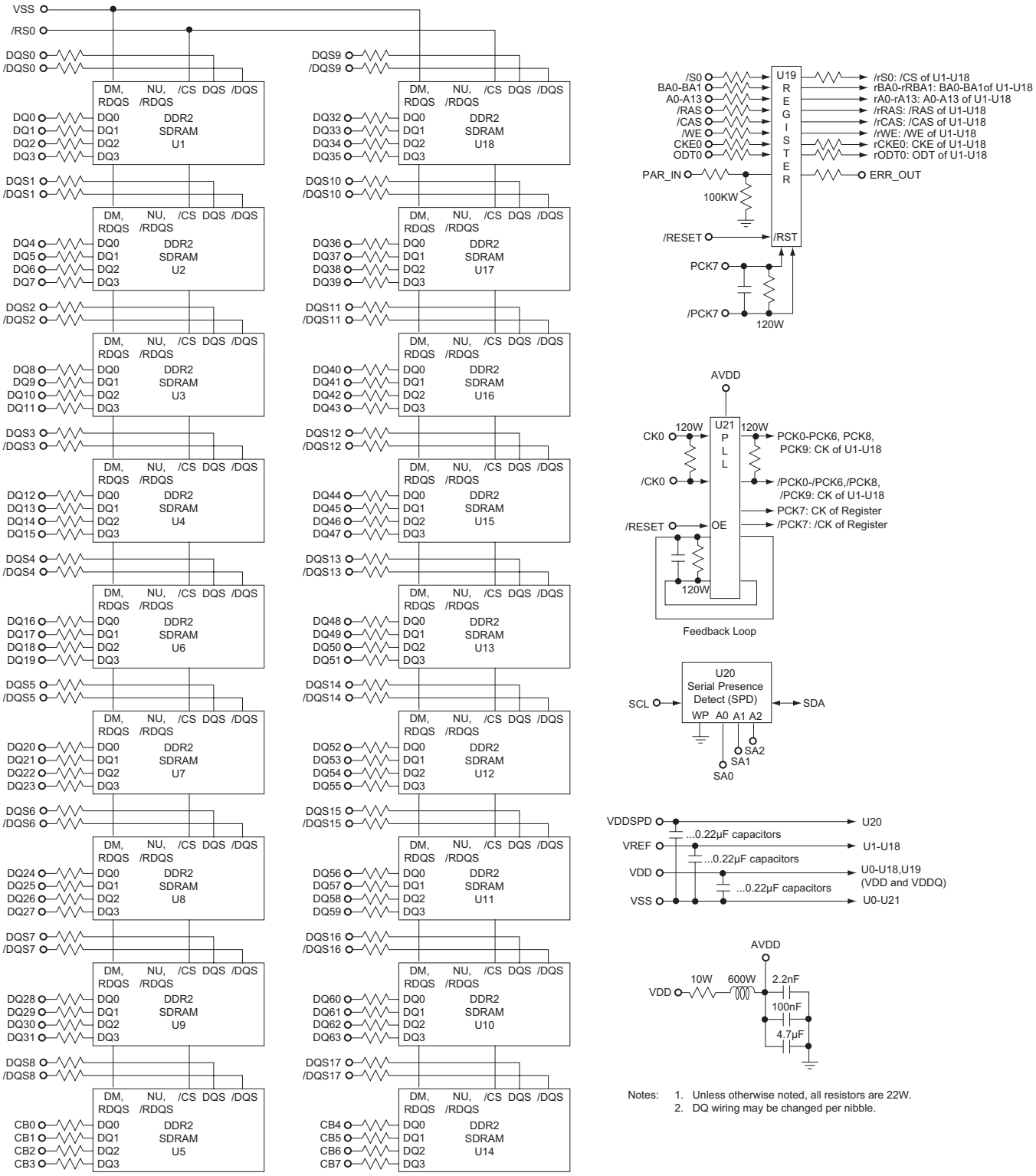
(Pin Configuration continued on next page)

PIN CONFIGURATION *continued (* = Not Used; / = Active Low)*

Pin Functions

Symbol	Type	Function
CK0, /CK0	Input	Clock
CKE0	Input	Clock Enable
/S0	Input	Chip Select
ODT0	Input	On Die Termination
/RAS, /CAS, /WE	Input	Command Inputs (along with /S)
BA0-BA1	Input	Bank Address Inputs
A0-A13	Input	Address Inputs
DQ0-DQ63	Input/Output	Data
CB0-CB7	Input/Output	Check Bits
DQS0-DQS17, /DQS0-/DQS17	Input/Output	Data Strobe
SCL	Input	Serial Clock for Presence Detect
SA0-SA2	Input	Presence Detect Address Inputs
SDA	Input /Output	Serial Presence Detect Data
/RESET	Input	Reset
NC		No Connect
RFU		Reserved for Future Use
VDDQ	Supply	DQ Power Supply: 1.8V±0.1V
VDD	Supply	Power Supply: 1.8V±0.1V
VSS	Supply	Ground
VREF	Supply	Reference Voltage
VDDSPD	Supply	Serial EEPROM Positive Power Supply: 1.7V to +3.6V
PAR-IN	Input	Parity Bit for the Address and Command Bus (“1”: odd, “0”: even)
ERR-OUT	Output	Parity Error Found in the Address or Command Bus

FUNCTIONAL BLOCK DIAGRAM



Notes:
1. Unless otherwise noted, all resistors are 22W.
2. DQ wiring may be changed per nibble.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes Used by STEC	128	80
1	Total Number of Bytes in SPD Device	256	08
2	Fundamental Memory Type	SDRAM DDR2	08
3	Number of Row Addresses on Assembly	14	0E
4	Number of Column Addresses on Assembly	11	0B
5	DIMM Height and Module Ranks	18.288mm, planar, 1 rank	60
6	Module Data Width	72	48
7	Reserved	Undefined	00
8	Module Voltage Interface Levels	SSTL 1.8V	05
9	SDRAM Cycle Time, tCK (CAS Latency= 5)	5.0ns	50
10	SDRAM Access from Clock,tAC (CAS Latency = 5)	±0.6ns	60
11	Module Configuration Type	ECC	02
12	Refresh Rate/Type	7.81µs/SELF	82
13	SDRAM Device Width (Primary SDRAM)	x4	04
14	Error-checking SDRAM Data Width	x4	04
15	Reserved	Undefined	00
16	Burst Lengths Supported	4, 8	0C
17	Number of Banks on SDRAM Device	4	04
18	CAS Latencies Supported	3, 4, 5	38
19	Reserved	Undefined	00
20	DDR2 DIMM Type	Regular RDIMM	01
21	SDRAM Module Attributes	Undefined	00
22	SDRAM Device Attributes: General	Supports weak driver	01
23	SDRAM Cycle Time, tCK, (CAS Latency= 4)	5.0ns	50
24	SDRAM Access from CK, tAC, (CAS Latency = 4)	±0.6ns	60
25	SDRAM Cycle Time, tCK, (CAS Latency = 3)	5.0ns	50
26	SDRAM Access from CK, tAC, (CAS Latency = 3)	±0.6ns	60
27	Minimum Row Precharge Time, tRP	15ns	3C
28	Minimum Row Active to Row Active, tRRD	7.5ns	1E
29	Minimum RAS# to CAS# Delay, tRCD	15ns	3C
30	Minimum RAS# Pulse Width, tRAS	40ns	28
31	Module Rank Density	1GB	01
32	Address and Command Setup Time, tIS	0.35ns	35
33	Address and Command Hold Time, tIH	0.47ns	47
34	Data/ Data Mask Input Setup Time, tDS	0.15ns	15
35	Data/ Data Mask Input Hold Time, tDH	0.27ns	27
36	Write Recovery Time, tWR	15ns	3C
37	Write to Read CMD Delay, tWTR	10ns	28
38	Read to Precharge CMD Delay, tRTP	7.5ns	1E
39	Mem Analysis Probe	Undefined	00
40	Extension for bytes 41 and 42	Undefined	00
41	Min Active Auto Refresh Time, tRC	55ns	37
42	Min. Auto Refresh to Active/ Auto Refresh Command Period, tRFC	105ns	69
43	SDRAM Device Max Cycle Time, tCKMAX	8ns	80
44	SDRAM Device Max DQS-DQ Skew Time, tDQSQ	0.35ns	23

(Serial Presence Detect Information continued on next page)

SERIAL PRESENCE DETECT INFORMATION *continued*

Byte	Description	Entry	Hex Value
45	SDRAM Device Max Read Data Hold Skew Factor, tQHS	0.45ns	2D
46	PLL Relock Time	15µs	0F
47-61	Reserved	Reserved	00
62	SPD Revision	Release 1.0	10
63	Checksum For Bytes 0-62	JEDEC calc.	00
64	Manufacturer's JEDEC ID Code STEC	Continuation code	7F
65	Man. JEDEC ID code (continued)	STEC's ID	A8
66-71	Reserved	Undefined	00
72	Manufacturing Location	STEC USA/Malaysia	01/02
73-90	Module Part Number (ASCII)	P/N	xx
91	PCB Identification Code	PCB ID code	xx
92	Reserved	Undefined	00
93	Year of Manufacture in BCD	Year	yy
94	Week of Manufacture in BCD	Week	w w
95-98	Module Serial Number	Serial Number	ss
99-127	Manufacturer-Specific Data (RSVD)	Undefined	00

ABSOLUTE MAXIMUM DC RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Units
VDD	VDD Supply Voltage Relative to VSS		-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to VSS		-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to VSS		-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to VSS		-0.5	2.3	V
TSTG	Storage Temperature		-55	100	°C
TOPR	SDRAM Device Operating Temperature (See Notes 1, 2, 3)				
	Commercial Operating Temperature		0	85	°C
	Industrial Operation Temperature		0	95	°C
Ta	Ambient Operating Temperature				
	Commercial Operating Temperature		0	55	°C
	Industrial Operation Temperature		-40	85	°C
II	Input Leakage Current; Any input 0V<=VIN<=VDD;	Command/Address,	-5	5	µA
	VREF input 0V>=VIN>=0.95V; /RAS, /CAS, /WE,	/S, CKE, ODT	-5	5	µA
	(All other pins not under test = 0V)	CK, /CK	-5	5	µA
IOZ	Output Leakage Current; 0V>=VOUT>=VDDQ;	DQ, DQS, /DQS	-5	5	µA
	DQs and ODT are disabled				
IVREF	VREF Leakage Current; VREF=Valid VREF Level		-36	36	µA

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 to 85 °C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 to 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to VSS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply Voltage	VDD	1.7	1.8	1.9	V	1
VDDL Supply Voltage	VDDL	1.7	1.8	1.9	V	4
I/O Supply Voltage	VDDQ	1.7	1.8	1.9	V	4
I/O Reference Voltage	VREF	0.49 x VDDQ	0.50 x VDDQ	0.51 X VDDQ	V	2
I/O Termination Voltage (system)	VTT	VREF - 40	VREF	VREF + 40	mV	3

Notes:

1. VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peakto- peak noise (non-common mode) on VREF may not exceed ±1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed ±2 percent of VREF (DC). This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Input DC Logic Levels

All voltages referenced to VSS.

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	VIH(DC)	VREF + 125	VDDQ + 300	mV
Input Low (Logic 0) Voltage	VIL(DC)	-300	VREF - 125	mV

Input AC Logic Levels

All voltages referenced to VSS.

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	VIH(AC)	VREF + 250	-	mV
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 250	mV

IDD SPECIFICATIONS AND CONDITIONS

IDD specifications are tested after the device is properly initialized. 0°C ≤ TOPR ≤ +55°C. VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VDDL = +1.8V ±0.1V, VREF = VDDQ/ 2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DQS, and DQS#. IDD values must be met with all combinations of EMR bits 10 and 11.

Definitions for IDD Conditions:

- LOW is defined as VIN≤VIL (AC) (MAX)
- HIGH is defined as VIN≥VIH (AC) (MIN)
- STABLE is defined as inputs stable at a HIGH or LOW level
- FLOATING is defined as inputs at VREF = VDDQ/2
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
- Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes

General IDD Parameters

IDD Parameter	DDR2-400	Units
CL (IDD)	3	tCK
tRCD (IDD)	15	ns
tRC (IDD)	55	ns
tRRD (IDD)	7.5	ns
tCK (IDD)	5	ns
tRAS MIN (IDD)	40	ns
tRAS MAX (IDD)	70,000	ns
tRP (IDD)	15	ns
tRFC (IDD)	105	ns

IDD7 Conditions

IDD7: Operating Current, specifies detailed timing requirements for IDD7. Changes will be required if timing parameter changes are made to the specification.

IDD7 Operating Current

All Bank Interleave Read operation; legend: A = active; RA = read auto precharge; D = deselect

All device banks are being interleaved at minimum tRC (IDD) without violating tRRD (IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA.

Speed Grade	IDD7 Timing Patterns
DDR2-400	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D

DDR2 IDD Specifications and Conditions

Notes: 1–5. Values shown for DDR2 SDRAM components only.

Symbol—Parameter/Condition

IDD0—Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD1—Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.

IDD2P—Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.

IDD2Q—Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.

IDD2N—Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD3P—Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.

IDD3N—Active standby current; All device banks open; tCK = tCK(IDD), tRAS = tRAS MAX (IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD4W—Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, / CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD4R—Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD5—Burst refresh current; tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.

IDD6—Self refresh current; CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.

IDD7—Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.

Max DDR2 IDD Values

Symbol	DDR2-400	Units
IDD0	1,710	mA
IDD1	1,800	mA
IDD2P	144	mA
IDD2Q	450	mA
IDD2N	540	mA
IDD3P Fast PDN Exit MR[12] = 0	540	mA
IDD3P Slow PDN Exit MR[12] = 1	270	mA
IDD3N	1,170	mA
IDD4W	2,340	mA
IDD4R	2,520	mA
IDD5	3,330	mA
IDD6	99	mA
IDD7	4,770	mA

CAPACITANCE

Vdd = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VREF = VSS, f = 100 MHz, 0°C ≤TOPR ≤+55°C, VOUT (DC) = VDDQ/2, VOUT (peak to peak) = 0.1V; DM input is grouped with I/O pins because DM and the I/O pins are matched in loading.

Parameter	Symbol	Max	Units
Input Capacitance: CK, /CK (PLL Inputs)	CI1	8	pF
Input Capacitance: BA0, BA1, BA2, A0–A13, /S, /RAS, /CAS, /WE, CKE, ODT (Registered Buffer Inputs)	CI2	8.5	pF
Input/Output Capacitance: DQ, DQS	CIO	9	pF

AC OPERATING CONDITIONS

Notes: 1–5; 0°C ≤ TOPR ≤ +55°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics		DDR2-400			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Clock					
Clock cycle time CL = 5	tCK (5)	5,000	8,000	ps	16, 25
CL = 4	tCK (4)	5,000	8,000	ps	16, 25
CL = 3	tCK (3)	5,000	8,000	ps	16, 25
CK high-level width	tCH	0.45	0.55	tCK	19
CK low-level width	tCL	0.45	0.55	tCK	19
Half clock period	tHP	MIN(tCH, tCL)		ps	20
Clock jitter	tJIT	TBD	TBD	ps	18
Data					
DQ output access time from CK, /CK	tAC	-600	+600	ps	
Data-out high-impedance window from CK, /CK	tHZ		tAC MAX	ps	8, 9
Data-out low-impedance window from CK, /CK	tLZ	tAC MIN	tAC MAX	ps	8, 10
DQ input setup time relative to DQS	tDSa	400		ps	7, 15, 22
DQ input hold time relative to DQS	tDHa	400		ps	7, 15, 22
DQ input setup time relative to DQS	tDSb	150		ps	7, 15, 22
DQ input hold time relative to DQS	tDHb	275		ps	7, 15, 22
DQ input pulse width (for each input)	tDIPW	0.35		tCK	
Data hold skew factor	tQHS		450	ps	
DQ–DQS hold, DQS to first DQ to go nonvalid, per access	tQH	tHP -tQHS		ps	15, 17
Data valid output window (DVW)	tDVW	tQH -tDQSQ		ns	15, 17
Data Strobe					
DQS input high pulse width	tDQSH	0.35		tCK	
DQS input low pulse width	tDQSL	0.35		tCK	
DQS output access time from CK, /CK	tDQSCK	-500	+500	ps	
DQS falling edge to CK rising – setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising – hold time	tDSH	0.2		tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access	tDQSQ		350	ps	15, 17
DQS read preamble	tRPRE	0.9	1.1	tCK	36
DQS read postamble	tRPST	0.4	0.6	tCK	36
DQS write preamble setup time	tWPRES	0		ps	12, 13
DQS write preamble	tWPRE	0.35		tCK	
DQS write postamble	tWPST	0.4	0.6	tCK	11
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	tCK	

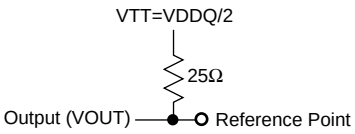
(AC Operating Conditions continued on next page)

AC OPERATING CONDITIONS (continued)

AC Characteristics		DDR2-400			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Command and Address					
Address and control input pulse width for each input	tIPW	0.6		tCK	
Address and control input setup time	tISa	600		ps	6, 22
Address and control input hold time	tIHa	600		ps	6, 22
Address and control input setup time	tISb	350		ps	6, 22
Address and control input hold time	tIHb	475		ps	6, 22
/CAS to /CAS command delay	tCCD	2		tCK	
ACTIVE to ACTIVE (same bank) command	tRC	55		ns	34
ACTIVE BANK *a* to ACTIVE bank *b* command	tRRD	7.5		ns	28
ACTIVE to READ or WRITE delay	tRCD	15		ns	
Four Bank Activate Period	tFAW	37.5		ns	31
ACTIVE to PRECHARGE command	tRAS	40	70,000	ns	21, 34
Internal READ to precharge command delay	tRTP	7.5		ns	24, 28
Write recovery time	tWR	15		ns	28
Auto precharge write recovery + precharge time	tDAL	tWR + tRP		ns	23
Internal WRITE to READ command delay	tWTR	10		ns	28
PRECHARGE command period	tRP	15		ns	32
PRECHARGE ALL command period	tRPA	tRP + tCK		ns	32
LOAD MODE command cycle time	tMRD	2		tCK	
CKE low to CK,CK# uncertainty	tDELAY	5.83	5.83	ns	29
Self Refresh					
REFRESH to Active or REFRESH command interval	tRFC	105	70,000	ns	14
Average periodic refresh interval	tREFI		7.8	µs	14
Exit self refresh to non-READ command	tXSNR	tRFC(MIN)+10		ns	
Exit self refresh to READ command	tXSRD	200		tCK	
Exit self refresh timing reference	tISXR	350		ps	6, 30
ODT					
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC MIN)	tAC(MAX)+1000	ps	26
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(MIN)	tAC(MAX)+600	ps	27
ODT turn-on (power-down mode)	tAONPD	tAC(MIN)+ 2,000	2xtCK+tAC (MAX)+1,000	ps	
ODT turn-off (power-down mode)	tAOFPD	tAC(MIN)+ 2,000	2.5xtCK+tAC (MAX)+1,000	ps	
ODT to power-down entry latency	tANPD	3		tCK	
ODT power-down exit latency	tAXPD	8		tCK	
Power Down					
Exit active power-down to READ command, MR[bit12=0]	tXARD	2		tCK	
Exit active power-down to READ command, MR[bit12=1]	tXARDS	6 - AL		tCK	
Exit precharge power-down to any non-READ command	tXP	2		tCK	
Exit precharge power-down to READ command	tXPRD	6 - AL		tCK	
CKE minimum high/low time	tCKE	3		tCK	35

NOTES

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between VIL (AC) and VIH (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using tISb and the Setup and Hold Time Derating Values table. tIS timing (tISb) is referenced from VIH (AC) for a rising signal and VIL(AC) for a falling signal. tIH timing (tIHb) is referenced from VIH(AC) for a rising signal and VIL(DC) for a falling signal. The timing table also lists the tISb and tIHb values for a 1.0V/ns slew rate; these are the “base” values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. tDS timing (tDSb) is referenced from VIH (AC) for a rising signal and VIL (AC) for a falling signal. tIH timing (tIHb) is referenced from VIH(DC) for a rising signal and VIL(DC) for a falling signal. The timing table lists the tDSb and tDHb values for a 1.0V/ns slew rate. If the DQS, /DQS differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS, /DQS. Data timing is now referenced to VREF, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to VIH(AC) for a rising DQS and VIL(DC) for a falling DQS.
8. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (tHZ) or begins driving (tLZ).
9. This maximum value is derived from the referenced test load. tHZ (MAX) will prevail over tDQSCK (MAX) + tRPST (MAX) condition.
10. tLZ (MIN) will prevail over a tDQSCK (MIN) + tRPRE (MAX) condition.
11. The intent of the Don’t Care state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above VIHDC(min) then it must not transition low (below VIH(DC) prior to tDQSH(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on tDQSS.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, a REFRESH command must be asserted at least once every 70.3µs or tRFC (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Each byte lane has a corresponding DQS.
16. CK and /CK input slew rate must be ≥ 1V/ns (≥ 2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - tHP. (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. tJIT specification is currently TBD.
19. MIN(tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50 percent of the period, less the half period jitter [tJIT(HP)] of the clock source, and less the half period jitter due to cross talk [tJIT(cross talk)] into the clock traces.
20. tHP (MIN) is the lesser of tCL minimum and tCH minimum actually applied to the device CK and /CK inputs.

(Notes continued on next page)

***NOTES** (continued)*

21. READS AND WRITES WITH AUTO PRECHARGE are allowed to be issued before tRAS (MIN) is satisfied since tRAS lockout feature is supported in DDR2 SDRAM devices.
22. VIL/VIH DDR2 overshoot/undershoot. REFER TO the 256Mb, 512Mb, or 1Gb DDR2 SDRAM data sheet for more detail.
23. tDAL = (nWR) + (tRP/tCK): For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period; nWR refers to the tWR parameter stored in the MR[11,10,9]. Example: For -53E at tCK = 3.75 ns with tWR programmed to four clocks. tDAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. The minimum READ to internal PRECHARGE time. This parameter is only applicable when tRTP/(2*tCK) > 1. If tRTP/(2*tCK) ≤ 1, then equation AL + BL/2 applies. Notwithstanding, tRAS (MIN) has to be satisfied as well. The DDR2 SDRAM device will automatically delay the internal PRECHARGE command until tRAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
26. ODT turn-on time tAON (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time tAON (MAX) is when the ODT resistance is fully on. Both are measured from tAOND.
27. ODT turn-off time tAOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time tAOF (MAX) is when the bus is in high impedance. Both are measured from tAOFD.
28. This parameter has a two clock minimum requirement at any tCK.
29. tDELAY is calculated from tIS + tCK + tIH so that CKE registration LOW is guaranteed prior to CK, /CK being removed in a system RESET condition.
30. tISXR is equal to tIS and is used for CKE setup time during self refresh exit.
31. No more than 4 bank ACTIVE commands may be issued in a given tFAW(min) period. tRRD(min) restriction still applies. The tFAW(min) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
32. tRPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, tRP timing applies. tRPA(MIN) applies to all 8-bank DDR2 devices.
33. Value is minimum pulse width, not the number of clock registrations.
34. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time (tWR) during auto precharge.
35. tCKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 * tCK + tIH.
36. This parameter is not referenced to a specific voltage level, but specified whwen the device output is no longer driving (tRPST) or beginning to drive (tRPRE).

REGISTER ELECTRICAL CHARACTERISTICS

0°C≤TOPR≤+70°C; VDD=VDDQ=+2.5V ±0.2V; Unless otherwise stated

Symbol	Parameters	Conditions	VDDQ	Min	Typ	Max	Units
VIK		II = -18mA				-1.2	V
VOH		IOH = -100µA IOH = -16mA	1.7V - 1.9V 1.7V	VDDQ - 0.2 1.95			V
VOL		IOL = 100µA IOL = 16mA	1.7V - 1.9V 1.7V			0.2 0.35	V V
II	All Inputs	VI = VDD or GND	1.9V			±5	µA
		0.01	µA				
IDD	Standby (Static) Operating (Static)	/RESET = GND, IO = 0 VI = VIH(AC) or VIL(AC), /RESET = VDD, IO = 0	1.9V 1.9V		 TBD	0.01	mA
IDDD	Dynamic operating (clock only) Dynamic Operating (per each data input)	/RESET = VDD, IO = 0, VI = VIH(AC) or VIL(AC), CLK and /CLK switching 50% duty cycle. /RESET = VDD, IO = 0 VI = VIH(AC) or VIL (AC), CLK and CLK# switching 50% duty cycle. One data input switching at half clock	1.8V 1.8V		TBD TBD		µ/clock MHz µA/clock MHz/data
rOH	Output High	IOH = -20m					Ω
rOL	Output Low	IOL = 20mA					Ω
rO(D)	[rOH - rOL] each separate bit	IO = 20mA, TA = 25° C				4	Ω
Ci	Data Inputs CLK and /CLK /RESET	VI = VREF ±350mV VICR = 1.25V, VI(PP) = 360mV VI = VDDQ or GND		2.5 2	 2.5	3.5 3	pF pF pF

REGISTER TIMING REQUIREMENTS

Over recommended operating free-air temperature range, unless otherwise noted; VDD=+1.8V ±0.1V

Symbol	Parameters		Min	Max	Units
fclock	Clock frequency			300	MHz
tS	Setup time	Data before CLK ↑, /CLK ↓ Data before CLK ↑, /CLK ↓	0.75 0.9		ns ns
Th	Hold time, fast slew rate[2,4], Hold time, slow slew rate[3,4]	Data after CLK ↑, /CLK ↓ Data after CLK ↑, /CLK ↓	0.50 0.70		ns ns

1. Guaranteed by design, not 100% tested in production.
2. For data signal input slew rate of 1V/ns.
3. For data signal input slew rate of 0.5V/ns and < 1V/ns.
4. CLK, /CLK signal input slew rate of 1V/ns.

REGISTER SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range, unless otherwise noted; VDD=+1.8V ±0.1V

Symbol	From (Input)	To (Output)	Min	Typ	Max	Units
fmax			270			MHz
tPDM[1]	CLK, /CLK	Q	1.41		1.75	ns
tPDMSS[2]	CLK, /CLK	Q				
tphl	/RESET	Q			3	ns

1. Includes 350ps test-load transmission-line delay
2. Guaranteed by design, not 100% tested in production.

PLL CLOCK DRIVER ELECTRICAL CHARACTERISTICS

0°C≤TOPR≤+70°C; AVDDQ=VDDQ=+1.8V ±0.1V; Unless otherwise stated

Symbol	Parameters	Conditions	Min	Typ	Max	Units
IIH	Input High Current (CLK_INT, CLK_INC)	VI = VDDQ or GND			±250	µA
IIL	Input Low Current (OE, OS, FB_INT, FB_INC)	VI = VDDQ or GND			±10	µA
IODL	Output Disabled Low Current	OE = L, VODL = 100mV	100			µA
IDD1.8 IDDLD	Operating Supply Current	CL = 0pf @ 270MHz CL = 0pf			300 500	mA µA
VIK	Input Clamp Voltage	VDDQ = 1.7V Iin = -18mA			-1.2	V
VOH	High-level output voltage	IOH = -100 µA IOH = -9 mA	VDDQ - 0.2 1.1	 1.45		V V
VOL	Low-level output voltage	IOL=100 µA IOL=9 mA		0.25	0.10 0.6	V V
CIN	Input Capacitance	VI = GND or VDDQ	2		3	pF
COUT	Output Capacitance	VOUT = GND or VDDQ	2		3	pF

PLL CLOCK DRIVER TIMING REQUIREMENTS

0°C≤TOPR≤+70°C; AVDDQ=VDDQ=+1.8V ±0.1V; Unless otherwise stated

Symbol	Parameters	Conditions	Min	Max	Units
freqOP	Max clock frequency	1.8V+0.1V @ 25°C	95	370	MHz
freqAPP	Application Frequency Range	1.8V+0.1V @ 25°C	160	350	MHz
dTIN	Input clock duty cycle		40	60	%
tSTAB	CLK stabilization			15	µs

PLL CLOCK DRIVER SWITCHING CHARACTERISTICS

0°C≤TOPR≤+70°C; AVDDQ=VDDQ=+1.8V ±0.1V; Unless otherwise stated

Symbol	Parameters	Conditions	Min	Typ	Max	Units
tEN	Output enable time	OE to any output		4.73	8	ns
tDIS	Output disable time	OE to any output		5.82	8	ns
tJIT(PER)	Period jitter		-30		30	ps
tJIT(HPER)	Half-period jitter		-60		60	ps
SLr1(i)	Input slew rate	Input Clock Output Enable (OE), (OS)	1 0.5	2.5	4	v/ns v/ns
SLr1(o)	Output clock slew rate		1.5	2.5	3	v/ns
tJIT(cc+) tJIT(cc-)	Cycle-to-cycle period jitter		0 0		40 -40	ps ps
t( )DYN	Dynamic Phase Offset		-20		20	ps
tSPO	Static Phase Offset[1]		-50	0	50	ps
tSKEW	Output to Output Skew				40	ps
	SSC modulation frequency deviation		30.00		33	kHz
	SSC clock input frequency		0.00		-0.50	%
	PLL Loop bandwidth (-3 dB MHz from unity gain)		2.0			MHz

1. Static phase offset shifted by design.

REVISION HISTORY

Rev.	Change Description from Previous Revision
-101	07/16/2004. Initial release.
-102	08/06/2004. Board height updated from 18mm to 18.3mm.
-103	01/27/2005. Preliminary notice removed. P/N changed to -D05AYU.
-104	04/18/2005. P/N changed to -B05AYU from -D05AYU. tCK(5) speeds added in SPD and AC Characteristics. Bytes 32-35 of SPD corrected. Block Diagram corrected to show series resistors on S, CKE, and ODT.
-105	01/26/2007. Added “W” designator to part number suffix and ordering information to indicate that the product can be ordered with industrial operating temperature grade components.
-106	07/27/2007. Updated logo, web address and SPD.