

# LatticeECP2/M Family

## Exceptional Performance – Uncommon Value

The LatticeECP2™ (Economy Plus 2nd generation) and LatticeECP2M™ families, collectively referred to as LatticeECP2/M, redefine the low-cost FPGA category. By integrating features and capabilities previously available only on higher cost / high performance FPGAs, these families dramatically expand the range of applications that can take advantage of low-cost FPGA products.

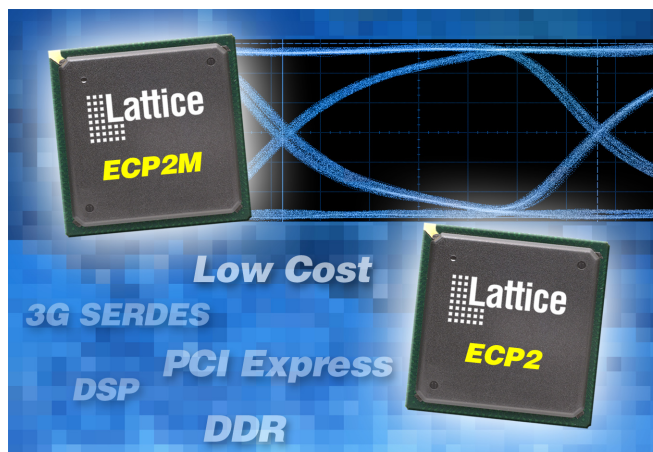
Features that the LatticeECP2 family brings to the low cost FPGA category include high performance DSP blocks, up to 70K LUT capacity, support for DDR2 memory interfaces at 533Mbps and up to 840Mbps generic LVDS performance. The LatticeECP2 also provides enhanced FPGA configuration options with features such as dual boot, bitstream encryption and TransFR™ I/O capability.

The LatticeECP2M includes embedded SERDES, increases density to 95K LUTs at under 0.35W static power, and provides significantly higher memory capacity, up to 5.3Mbits. The SERDES supports many common serial packet protocols including PCI Express and Ethernet (1GbE & SGMII).

The LatticeECP2/M devices are an excellent choice for a wide variety of applications, including, low-cost networking, blade servers, network access equipment, consumer electronics, industrial, medical, software defined radio, wireless communications, military and automotive.

### FPGA Fabric Features and Capabilities

- **Low Cost FPGAs**
  - Features optimized for mainstream applications
  - Balanced logic-memory-I/O resources
- **Lowest Power SERDES-based FPGA**
  - 95K LUTs with under 0.35W static power
- **Extensive Density and Package Options**
  - 6K to 95K LUT4s, 90 to 583 I/O
  - Density migration supported
  - TQFP, PQFP and fpBGA packaging options
  - Pb-free / RoHS-compliant options
- **Embedded and Distributed Memory**
  - 12K to 202K bits distributed memory
  - 55K to 5.3M bits sysMEM™ block memory
- **Flexible sysIO™ Buffers**
  - LVCMOS 33/25/18/15/12
  - PCI
  - SSTL3/2/18 & HSTL15 & HSTL18
  - LVDS, RSDS, Bus-LVDS, MLVDS & LVPECL
- **sysCLOCK™ PLL and DLL**
  - 2 DLLs per device
  - 2 to 8 PLLs per device
- **System Level Support**
  - IEEE 1149.1 boundary scan
  - 1.2-volt power supply



### LatticeECP2 Features and Benefits

#### EMBEDDED SERDES

- 3.125Gbps with Low 100mW Power per Channel
- Receive Equalization and Transmit Pre-emphasis
- Supports PCI Express, Ethernet (1GbE & SGMII) Plus Multiple Other Standards

#### LOW POWER

- 95K LUTs with under 0.35W Static Power
- Improve Thermal Management, System Reliability and Reduce Overall System Cost

#### sysDSP™ BLOCKS

- Multiply, Accumulate, Addition & Subtraction in Dedicated Blocks
- Implement High-Performance DSP Functions Such as FIR, FFT and NCO in a Low-Cost FPGA
- Up to 168 18x18 Multipliers Give 63 GMAC DSP Performance

#### HIGH-SPEED I/O

- I/O Cells Include Dedicated DDR Mux/Demux, DQS Alignment and Gearbox Logic
- Pre-Engineered Source Synchronous Interfaces
  - DDR1 400Mbps; DDR2 533Mbps
  - SPI4.2 750Mbps
  - Generic 840Mbps

#### SUPERIOR CONFIGURATION OPTIONS

- Industry Standard SPI Boot Flash Interface
- Bitstream Encryption Prevents Design Piracy
- Dual Boot Provides Backup Configuration Copy
- TransFR I/O Supports Updates While System Operates

# LatticeECP2/M Architecture

## Architecture Overview

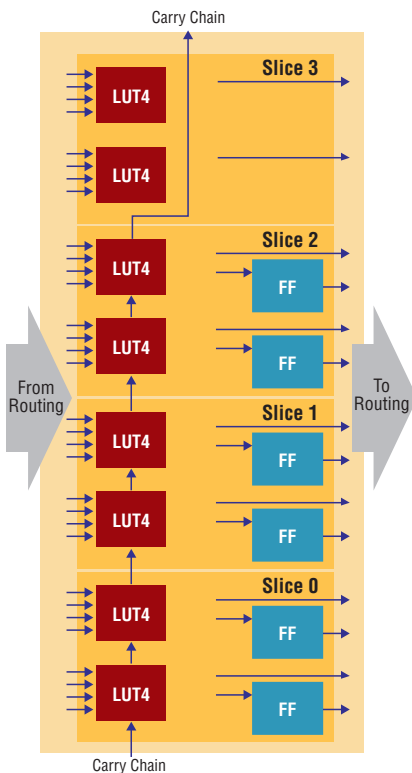
The LatticeECP2 family is designed to offer exceptional functionality, performance and low power. Built with an extremely efficient architecture, these low-cost FPGAs deliver low power, high-performance DSP blocks, sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interfaces, source synchronous interfaces, sysIO buffers, and enhanced configuration capabilities including encryption, dual-boot and TransFR field updates. The ECP2M devices provide all the features of the LatticeECP2 family and adds a high performance SERDES block capable of supporting many common packet based protocols including PCI Express, Ethernet (1GbE and SGMII) and related packet protocol standards.

## Programmable Function Unit Blocks (PFU)

The core of LatticeECP2/M devices consists of an array of optimized Programmable Functional Units (PFU). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

- Four Slices per PFU
- Optimized LUT to Register Ratio
- Distributed Memory Supported in Selected Slices
- Each Slice Individually Programmable
- Concatenate Slices for Longer Functions
- Concatenate PFUs for Complex Functions

## PFU BLOCK DIAGRAM



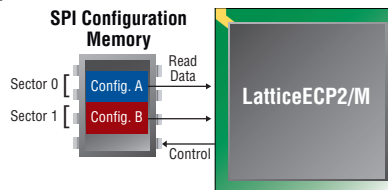
## Enhanced Configuration

Each LatticeECP2/M device can be configured using:

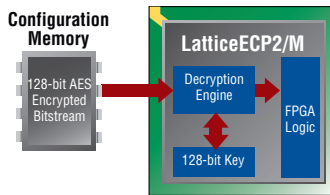
- A Low-Cost SPI Flash Memory
- The LatticeECP2/M JTAG Port
- The LatticeECP2/M Serial or Parallel Microprocessor Port

The configuration interface has a number of enhanced features, including:

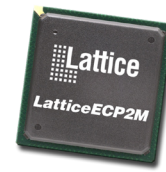
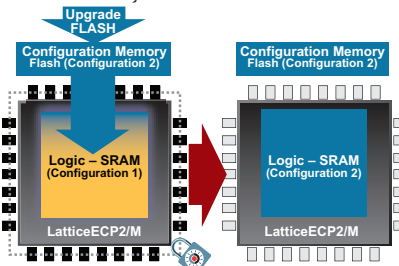
**Dual Boot Operation** – Supports the storage of multiple configurations in SPI memory, adding flexibility and reliability, particularly for systems that require field updates.



**Bitstream Encryption** – LatticeECP2/M devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and preventing design piracy.



**TransFR I/O** – LatticeECP2/M devices feature TransFR I/O that allows I/O states to be frozen during device configuration. This allows device field updates with a minimum of system downtime.



Low-cost LatticeECP2M devices offer more of the best with 3.125Gbps SERDES, up to 95K LUTs at under 0.35W static power, 533Mbps DDR2 interface, dual boot support, and up to 168 18x18 multipliers.

## LatticeECP2M Block Diagram

**Programmable Function Unit (PFU)** perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

**Flexible sysIO Buffers** support LVCMOS, HSTL, SSTL, LVDS and more.

**sysCLOCK PLLs & DLLs** for clock management.

**On-Chip Oscillator**

**Advanced Configuration Logic** supports dual boot, encryption, and TransFR I/O.

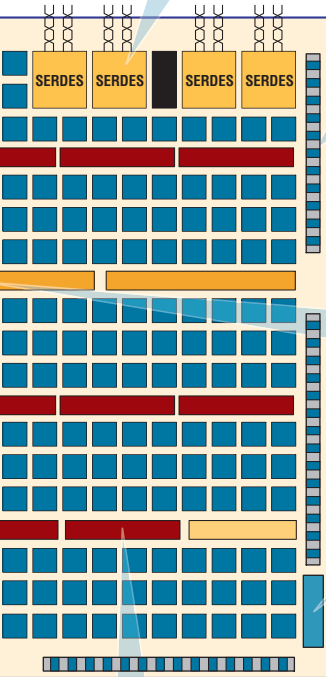
## High-Speed sysDSP Blocks

LatticeECP2/M devices include up to 42 high-performance sysDSP blocks per device. sysDSP blocks are optimized for processing intensive applications and allow designers to quickly implement DSP functions. Each sysDSP block provides:

- Configurable Multiplier Widths:
  - One 36x36
  - Four 18x18
  - Eight 9x9
- Programmable Addition, Subtraction, and Accumulate Modes
- Programmable Pipelining – Input, Intermediate and Output
- 375MHz Performance



**Embedded 3.125Gbps SERDES** support PCI Express, Ethernet (1GbE, SGMII, CPRI, and OBSAI).



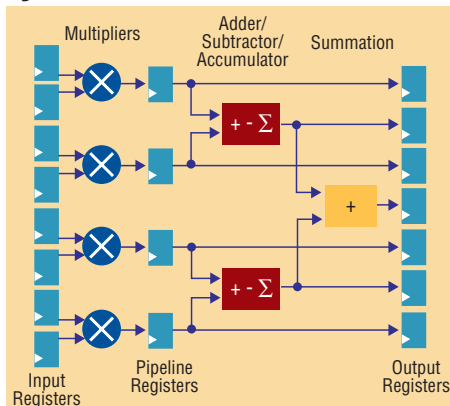
**Pre-Engineered Source Synchronous Support** implements DDR2 at 533Mbps, SPI4.2 at 750Mbps and generic interfaces up to 840Mbps.

**sysDSP Blocks** implement multipliers, adders, subtractors, accumulators.

**Configuration Port** supports SPI, serial and parallel configuration.

**sysMEM Embedded Block RAM (EBR)** provides 18kbit dual port RAM.

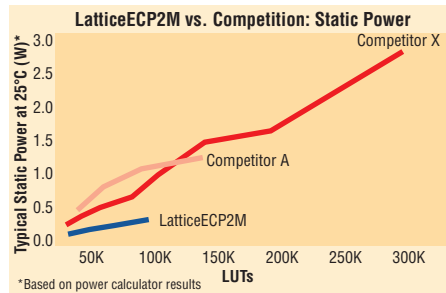
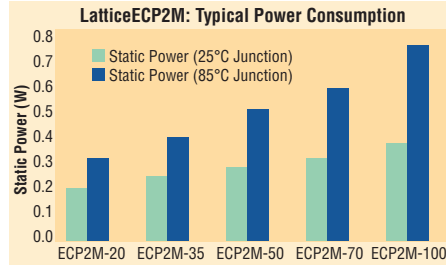
### sysDSP BLOCK DIAGRAM



One LatticeECP2/M device can provide up to 63,000 Million Multiply Accumulates per second (MMACs)!

### Optimized for Low Power

LatticeECP2/M devices are optimized to offer high functionality and low power. The static power advantage is achieved by using various process and architectural enhancements as well as software power optimization techniques.

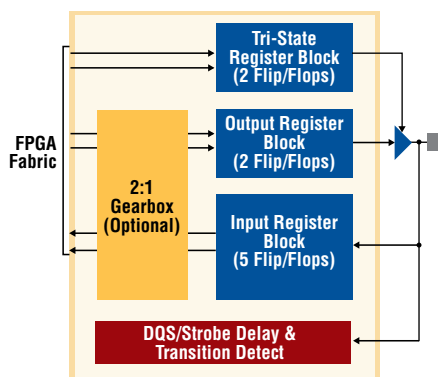


### Pre-Engineered Source Synchronous I/O

The I/O cells in the LatticeECP2/M devices contain a number of pre-engineered elements to allow the easy implementation of source synchronous interfaces such as those found on DDR1/2 memories, SPI4.2 systems and high-speed ADC/DACs.

- Precision DQS/Strobe Delay Control
- Dedicated DDR Registers (For Mux and Demuxing)
- Automatic DQS to System Clock Transfer
- 2:1 Gearbox Logic to Match I/O Speed with FPGA Fabric
- Low Skew Edge Clocks

### I/O CELL BLOCK DIAGRAM



### sysMEM Embedded Block RAM (EBR)

LatticeECP2/M FPGAs include flexible sysMEM EBR blocks. sysMEM EBR blocks provide on-chip memory resources to support a broad range of features.

- Up to 5.3Mb sysMEM Embedded Block RAM (EBR)
- 3 to 288 Memory Blocks per Device
- Configurable Width and Depth
- Single Port, Dual Port and Pseudo Dual Port Modes
- Bus Size Matching
- RAM Initialization and ROM Operation
- Memory Cascading

### sysCLOCK PLLs & DLLs for Timing Control

- PLLs
  - Frequency Range 2 to 420MHz Programmable Phase/Duty Cycle (22.5 degree steps)
  - Programmable Input, Scaling, Feedback and Secondary Counters
  - Internal and External Feedback
- DLLs
  - Frequency Range 100 to 500MHz
  - Programmable Phase (11.25 degree steps)
  - Optional Duty Cycle Correction
  - Additional Matched Delay Block

### sysIO Buffer Supports High-Bandwidth I/O Standards

With Lattice's sysIO interfaces, LatticeECP2/M devices can easily communicate with a variety of devices, supporting many single-ended and differential I/O standards.

- LVCMOS / LVTTTL
  - Hotsocketing capable
  - Programmable slew rate
  - Programmable drive strength
  - Programmable pull-up, pull-down, bus friendly
  - Programmable open drain
- PCI, LVDS, SSTL, HSTL, Differential HSTL, Differential SSTL, LVPECL, BLVDS, RSDS and MLVDS
- Eight General Purpose I/O Banks Per Device

## LatticeECP2 (Economy Plus FPGAs with sysDSP Blocks, & Source Synchronous I/O)

Parameter	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
Number of PFUs	756	1512	2646	4032	5994	8514
LUTs (K)	6	12	21	32	48	68
18x18 Embedded Multipliers	12	24	28	32	72	88
Distributed RAM (K bits)	12	24	42	65	96	136
Number of EBR SRAM Blocks	3	12	15	18	21	60
EBR Block SRAM (K bits)	55	221	276	332	387	1106
Number of PLLs/DLLs	2/2	2/2	2/2	2/2	4/2	6/2
V <sub>CC</sub> Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2
Maximum Available I/O	190	297	402	450	500	583
<b>Packages &amp; I/O Combinations</b>						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

## LatticeECP2M (Economy Plus FPGAs with SERDES, sysDSP Blocks, & Source Synchronous I/O)

Parameter	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
Number of PFUs	2403	4275	5958	8316	11844
LUTs (K)	19	34	48	67	95
18x18 Embedded Multipliers	24	32	88	96	168
Distributed RAM (K bits)	41	71	101	145	202
Number of EBR SRAM Blocks	66	114	225	246	288
EBR Block SRAM (K bits)	1217	2101	4147	4534	5308
Number of PLLs/DLLs	8/2	8/2	8/2	8/2	8/2
V <sub>CC</sub> Voltage (V)	1.2	1.2	1.2	1.2	1.2
Maximum Available I/O	304	410	438	452	520
<b>Packages &amp; SERDES / I/O Combinations</b>					
256-ball fpBGA (17 x 17 mm)	4/140	4/140			
484-ball fpBGA (23 x 23 mm)	4/304	4/303	4/270		
672-ball fpBGA (27 x 27 mm)		4/410	8/372		
900-ball fpBGA (31 x 31 mm)			8/410	16/416	16/416
1152-ball fpBGA (35 x 35 mm)				16/436	16/520

### Applications Support

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