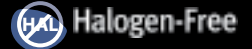


## EPC2014 – Enhancement Mode Power Transistor

 $V_{DSS}$ , 40 V $R_{DS(ON)}$ , 16 m $\Omega$  $I_D$ , 10 A

NEW PRODUCT



Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(ON)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2014 eGaN® FETs are supplied only in passivated die form with solder bumps

**Applications**

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

**Benefits**

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra low  $Q_G$
- Ultra small footprint

Maximum Ratings			
$V_{DS}$	Drain-to-Source Voltage	40	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $\theta_{JA} = 50$ )	10	A
	Pulsed ( $25^\circ\text{C}$ , $t_{pulse} = 300 \mu\text{s}$ )	40	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Negative Gate-to-Source Voltage	-5	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)					
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 125 \mu\text{A}$	40		V
$I_{DSS}$	Drain Source Leakage	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$		50	$\mu\text{A}$
$I_{GSS}$	Gate-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.4	mA
	Gate-Source Reverse Leakage	$V_{GS} = -5\text{ V}$		0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 2\text{ mA}$	0.7	1.4	V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 5\text{ A}$		12	m $\Omega$
<b>Dynamic Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)					
$C_{ISS}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$		300	pF
$C_{OSS}$	Output Capacitance			150	
$C_{RSS}$	Reverse Transfer Capacitance			10.2	
$Q_G$	Total Gate Charge	$V_{DS} = 20\text{ V}$ , $V_{GS} = 5\text{ V}$ , $I_D = 10\text{ A}$		2.48	nC
$Q_{GD}$	Gate to Drain Charge	$V_{DS} = 20\text{ V}$ , $I_D = 10\text{ A}$		0.48	
$Q_{GS}$	Gate to Source Charge			0.67	
$Q_{OSS}$	Output Charge			4.8	
$Q_{RR}$	Source-Drain Recovery Charge			0	
<b>Source-Drain Characteristics</b> ( $T_J = 25^\circ\text{C}$ unless otherwise stated)					
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$ , $T = 25^\circ\text{C}$		1.3	V
		$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$ , $T = 125^\circ\text{C}$		1.4	

Figure 1: Typical Output Characteristics

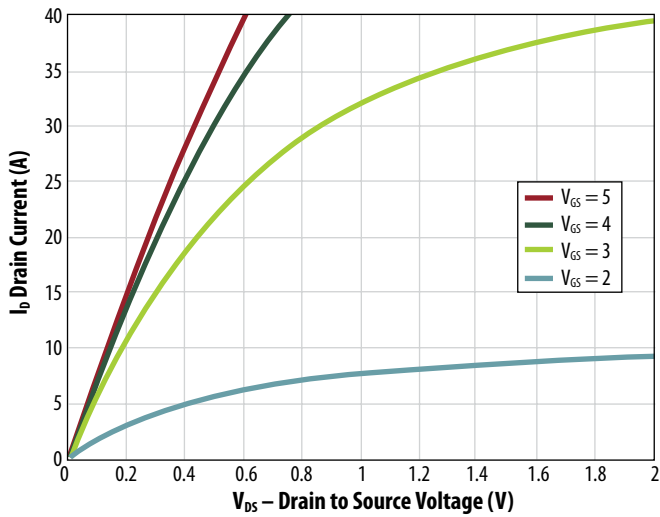


Figure 2: Transfer Characteristics

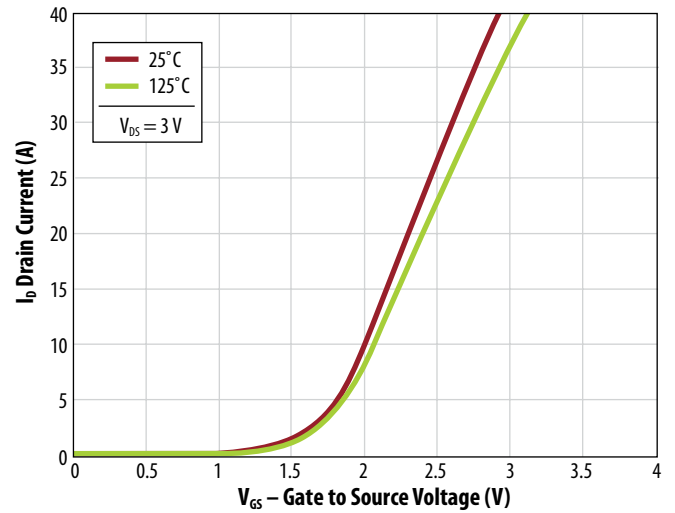


Figure 3:  $R_{DS(ON)}$  vs.  $V_{GS}$  for Various Drain Current

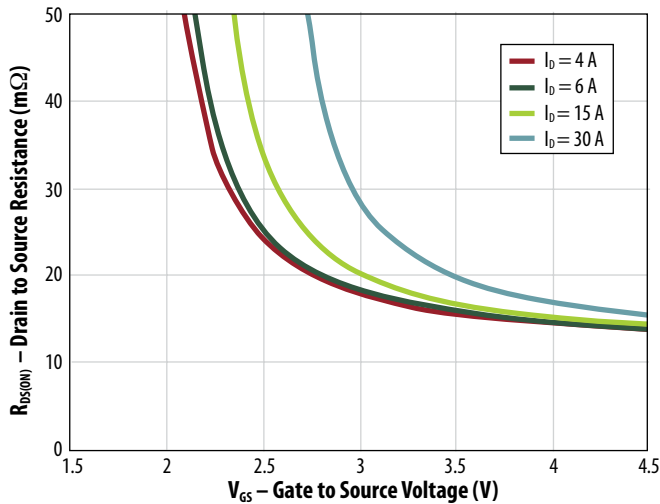


Figure 4:  $R_{DS(ON)}$  vs.  $V_{GS}$  for Various Temperatures

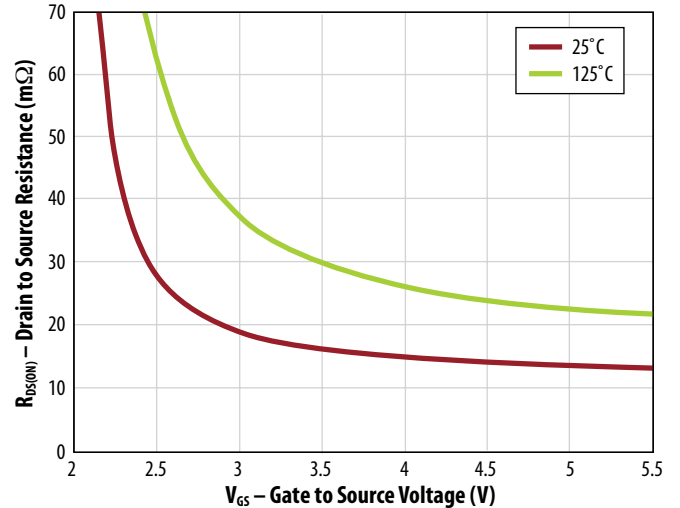


Figure 5: Capacitance

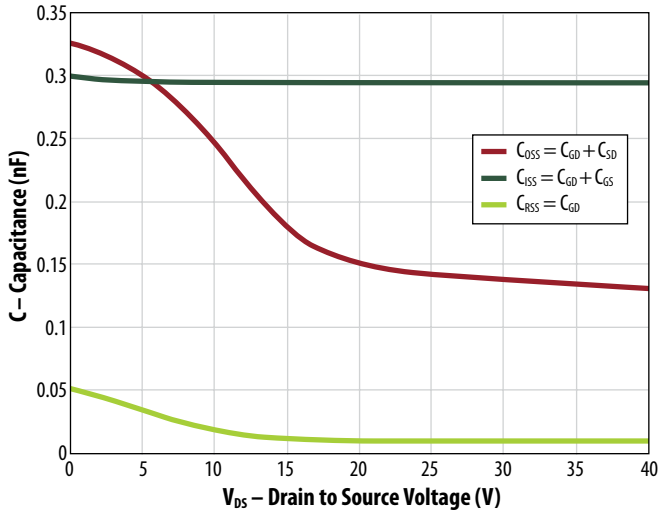


Figure 6: Gate Charge

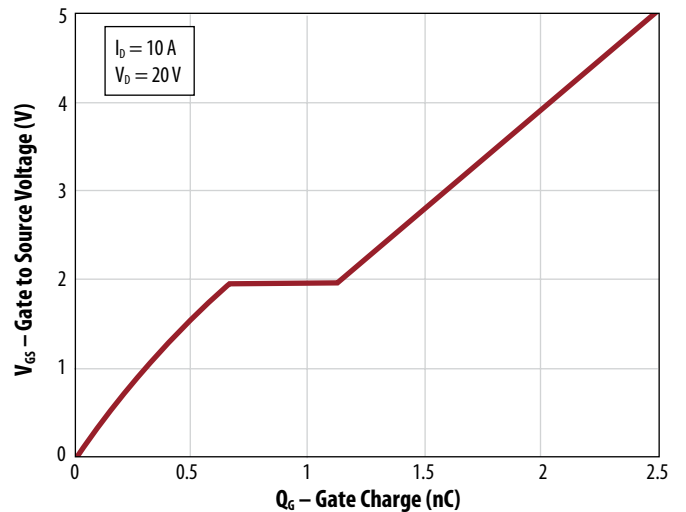


Figure 7: Reverse Drain-Source Characteristics

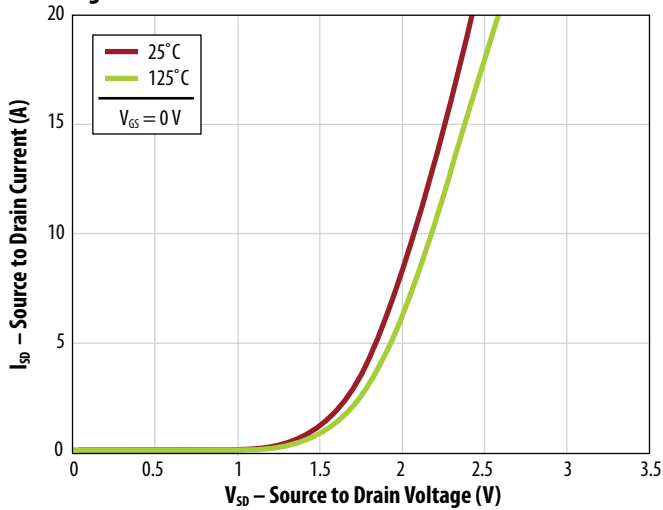


Figure 8: Normalized On Resistance vs. Temperature

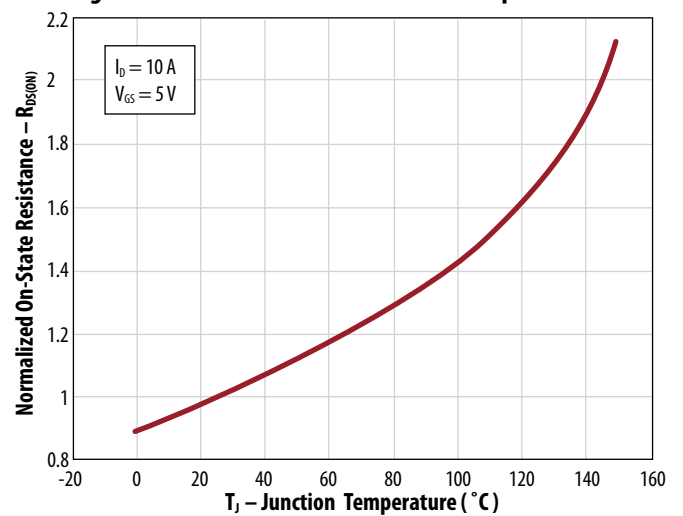


Figure 9: Normalized Threshold Voltage vs. Temperature

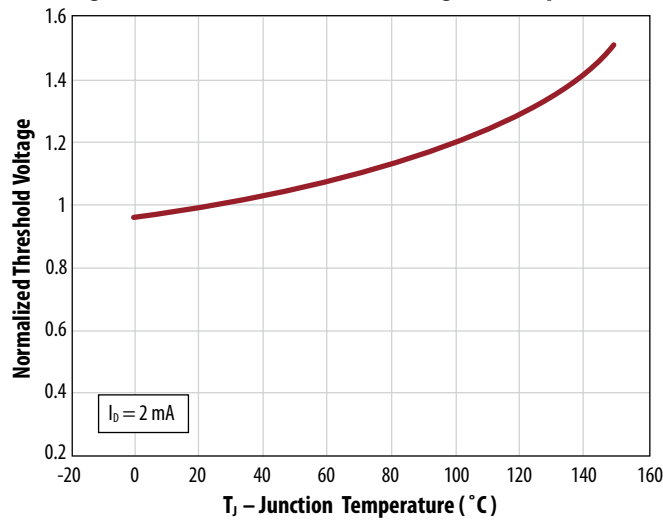
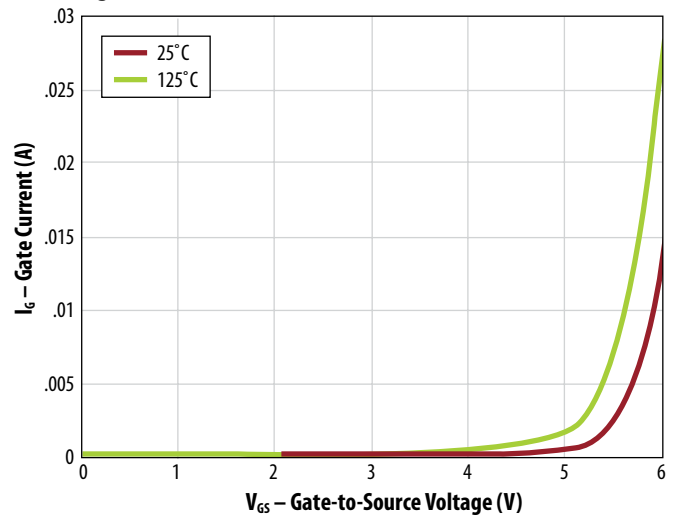
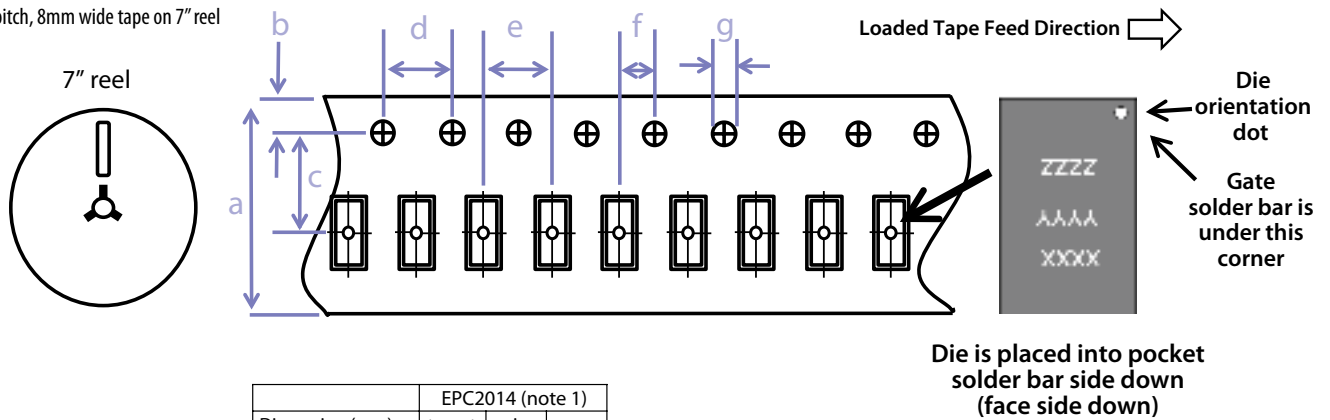


Figure 10: Gate Current



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel



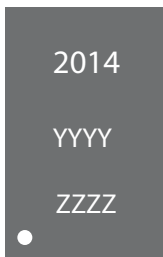
Dimension (mm)	EPC2014 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

**DIE MARKINGS**

Die orientation dot

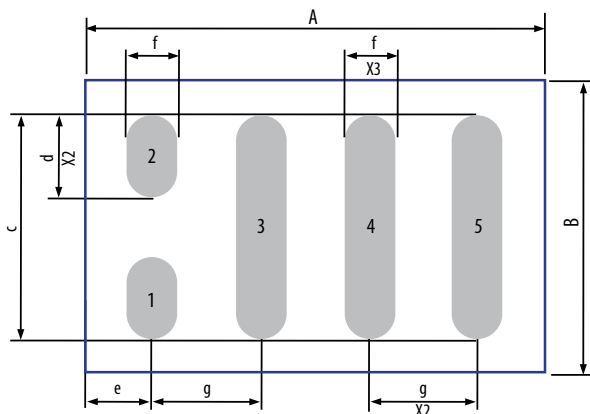
Gate Pad bump is under this corner



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2014	2014	YYYY	ZZZZ

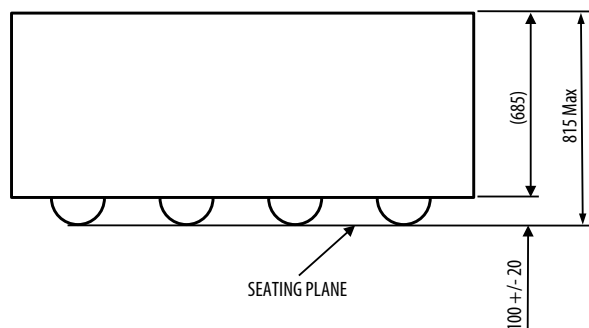
**DIE OUTLINE**

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1672	1702	1732
B	1057	1087	1117
c	834	837	840
d	327	330	333
e	235	250	265
f	195	200	205
g	400	400	400

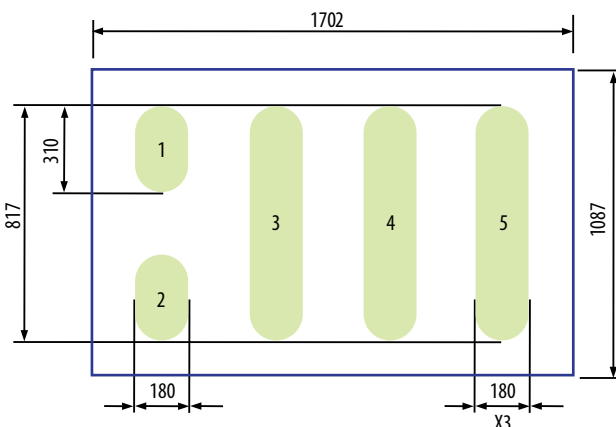
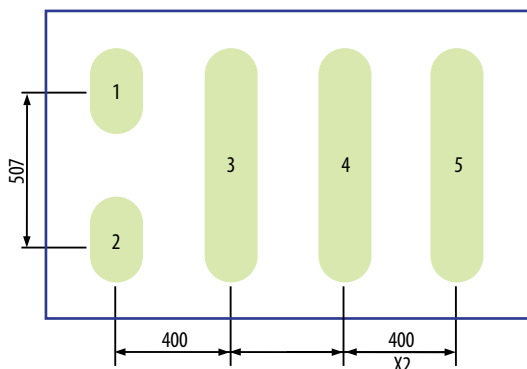
Side View



**RECOMMENDED LAND PATTERN**

(measurements in  $\mu\text{m}$ )

The land pattern is solder mask defined  
Solder mask is 10um smaller per side than bump



- Pad no. 1 is Gate
- Pad no. 2 is Substrate
- Pad no. 3 and 5 are Drain
- Pad no. 4 is Source

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revised August 2011