

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add three vendors, 18324, 1FN41, and 66579. Add device types 04, 05, 06, and 07. Add margin test method C. Update vendor's PIN. Change code indent. no. to 67268. Editorial changes throughout.	87-12-17	M. A. Frye
B	Add device type 08 with vendors CAGE 1FN41 and CAGE 66579. Added time temperature regression equation for unbiased bake. Removed vendor CAGE 66302. Made technical changes to table I, 4.2 back end margin test method step 3, 4.3.1 step C, table II, and table III. Editorial changes throughout. Added vendor's PIN from XMB/883 to either LM/883 for appropriate device types. Deleted the top CE waveform on figure 6. This was incorrect for this device.	89-01-01	M. A. Frye
C	Added vendor CAGE 34335 to the drawing as a source of supply for device types 01 through 07. Add vendor CAGE number 66579 to device types 01 through 04, also add vendor CAGE number 01295 to devices 04XX and 05XX. Add test condition A to 4.2 and 4.3.2. Add margin test method E for vendor CAGE number 34335. Change to vendor similar PIN for vendor CAGE numbers 1FN41 and 66579. Change to figure 3, margin test method C for vendor CAGE 01295 and change to programming waveforms. Change to 4.5. Editorial changes throughout. Add case outline Z for vendor CAGE number 1FN41.	90-12-05	M. A. Frye
D	Changes in accordance with NOR 5962-R130-92.	92-01-30	M. A. Frye
E	Add case outline U. Add device types 09 and 10. Remove vendor 27014 from drawing. Editorial changes throughout.	93-10-15	M. A. Frye
F	Changes in accordance with NOR 5962-R118-94.	94-02-16	M. A. Frye
G	Updated boilerplate. Added device types 11-21. Removed vendors 1FN41, 18324, 34335, and 61394 from drawing. Added vendor 65786 to drawing. Removed margin test methods from drawing.	97-06-11	Raymond Monnin
H	Boilerplate update, part of 5 year review. ksr	06-07-17	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

**CURRENT CAGE CODE IS 67268**

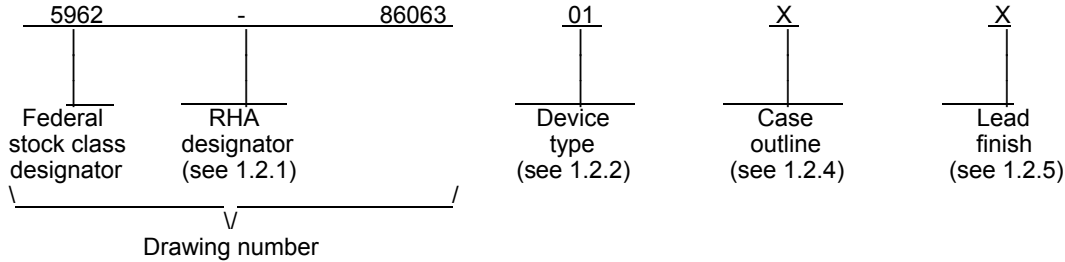
REV																				
SHEET																				
REV	H	H																		
SHEET	15	16																		
REV STATUS OF SHEETS	REV		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY James E. Jamison				<b>DEFENSE SUPPLY CENTER COLUMBUS</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a> <b>MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 262,144-BIT (32K x 8) UV ERASABLE PROM, MONOLITHIC SILICON</b>															
<b>STANDARD MICROCIRCUIT DRAWING</b> THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles Reusing																			
	APPROVED BY Michael A. Frye																			
	DRAWING APPROVAL DATE 87-02-12																			
	REVISION LEVEL H				SIZE <b>A</b>	CAGE CODE <b>14933</b>		<b>5962-86063</b>												
					SHEET		1 OF 16													

# 1. SCOPE

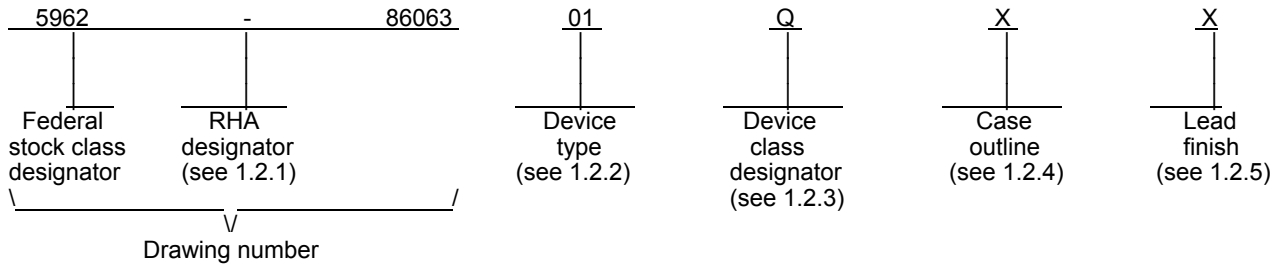
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device class M:



For device classes Q and V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01,11	(see 6.6)	32K x 8-bit UV EPROM	200 ns
02,12	(see 6.6)	32K x 8-bit UV EPROM	250 ns
03,13	(see 6.6)	32K x 8-bit UV EPROM	300 ns
04,14	(see 6.6)	32K x 8-bit UV EPROM	170 ns
05,15	(see 6.6)	32K x 8-bit UV EPROM	150 ns
06,16	(see 6.6)	32K x 8-bit UV EPROM	120 ns
07,17	(see 6.6)	32K x 8-bit UV EPROM	90 ns
08,18	(see 6.6)	32K x 8-bit UV EPROM	70 ns
09,19	(see 6.6)	32K x 8-bit UV EPROM	55 ns
10,20	(see 6.6)	32K x 8-bit UV EPROM	45 ns
21	(see 6.6)	32K x 8-bit UV EPROM	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>2</b>

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u> 1/
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	See figure 1	32	J-lead chip carrier
U	CDIP3-T28 or GDIP4-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings.

Storage temperature -----	-65°C to +150°C
Input voltages with respect to ground -----	+6.5 V dc to -0.3 V dc
Output voltages with respect to ground -----	V <sub>CC</sub> +0.3 V dc to GND -0.3 V dc
V <sub>PP</sub> supply voltage with respect to ground -----	+14.0 V dc to -0.6 V dc
Power dissipation (P <sub>D</sub> ) 2/ -----	+500 mW
Lead temperature (soldering, 10 seconds)-----	+300°C
Thermal resistance, junction-to-case (Θ <sub>JC</sub> ):	
Case outlines X, Y, and U -----	See MIL-STD-1835
Case outline Z -----	13°C/W
Junction temperature (T <sub>J</sub> ) -----	+150°C

1.4 Recommended operating conditions.

Case operating temperature (T <sub>C</sub> ) -----	-55°C to +125°C
Supply voltage (V <sub>CC</sub> )-----	+4.5 V dc to +5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Lid shall be transparent to permit ultraviolet light erasure.  
2/ Must withstand the added P<sub>D</sub> due to short circuit test; e.g., IOS.

<b>STANDARD  MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>3</b>

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 3. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6.

3.6.3 Verification of state of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>4</b>

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc unless otherwise specified	Device type	Group A subgroups	Limits		Unit					
					Min	Max						
Input load current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to 5.5 V	All	1, 2, 3		±10	μA					
Output leakage current	I <sub>LO 1/</sub>	V <sub>OUT</sub> = 0 to 5.5 V	All	1, 2, 3		±10	μA					
Operating current TTL inputs	I <sub>CC1</sub>	$\overline{CE} = \overline{OE} = V_{IL}$ V <sub>PP</sub> = V <sub>CC</sub> I <sub>0-7</sub> = 0 mA f = $\frac{1}{t_{ACC}}$ maximum	11-20	1, 2, 3		60	mA					
			01-05			50						
			06			65						
			07			70						
			08			90						
			09			115						
			10			130						
			21			85						
			Operating current CMOS inputs		I <sub>CC2</sub>			01,02, 03	1, 2, 3		25	mA
								04,05			40	
06		55										
07,11-20		60										
08,09		90										
10		100										
21		85										
Standby current TTL inputs	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$ V <sub>CC</sub> = 5.5 V, f = 0 MHz		01-05			1, 2, 3			3	mA	
				06,07,						5		
				08,09, 10						45		
			11-21		25							
Standby current CMOS inputs	I <sub>SB2</sub>		01-07, 08,09, 10	1, 2, 3		300	μA					
			11-21			45						
						25	mA					
V <sub>PP</sub> read current	I <sub>PP</sub>	V <sub>PP</sub> = V <sub>CC</sub> = 5.5 V	01-10 11-21	1, 2, 3		200 10	μA					
Input low voltage (TTL) (±10 percent supply)	V <sub>IL1</sub> 4/	V <sub>PP</sub> = V <sub>CC</sub>	All	1, 2, 3	-0.1 5/	0.8	V					
Input low voltage (CMOS)	V <sub>IL2</sub> 4/		All	1, 2, 3	-0.2 5/	0.2	V					
Input high voltage (TTL) (±10 percent supply)	V <sub>IH1</sub> 4/		All	1, 2, 3	2.0	V <sub>CC</sub> +1.0 5/	V					
Input high voltage (CMOS)	V <sub>IH2</sub> 4/		All	1, 2, 3	V <sub>CC</sub> -0.2	V <sub>CC</sub> +0.2 5/	V					

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>5</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 5.5 V	All	1, 2, 3		0.45	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	All	1, 2, 3	2.4		V
Output short circuit current	I <sub>OS</sub> 5/ 6/		All	1, 2, 3		-100	mA
V <sub>PP</sub> read voltage	V <sub>PPR</sub>		All	1, 2, 3	V <sub>CC</sub> -0.7	V <sub>CC</sub>	V
Address to output delay	t <sub>ACC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$ 7/ 8/	01,11	9, 10, 11		200	ns
			02,12			250	
			03,13			300	
			04,14			170	
			05,15			150	
			06,16			120	
			07,17			90	
			08,18			70	
			09,19			55	
			10,20			45	
			21			35	
$\overline{CE}$ to output delay	t <sub>CE</sub>	$\overline{OE} = V_{IL}$ 7/ 8/	01,11	9, 10, 11		200	ns
			02,12			250	
			03,13			300	
			04,14			170	
			05,15			150	
			06,16			120	
			07,17			90	
			08,18			70	
			09,19			55	
			10,20			45	
			21			40	
$\overline{OE}$ to output delay	t <sub>OE</sub>	$\overline{CE} = V_{IL}$ 7/ 8/	11-13	9, 10, 11		60	ns
			01			75	
			02			100	
			03			150	
			04,05			70	
			14,15			40	
			06,08,16			35	
			07,17			30	
			09,18			25	
			10,19,21			20	
			20			15	
$\overline{OE}$ high to output float	t <sub>DF</sub> 5/		01	9, 10, 11	0	55	ns
			02,11-13			60	
			03			105	
			04,05			50	
			14,15			40	
			06,08,16			35	
			07,17			30	
			09,18			25	
			10,19			20	
			20,21			15	

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>6</b>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output hold from addresses $\overline{CE}$ or $\overline{OE}$ (whichever occurred first)	t <sub>OH</sub> 5/	$\overline{CE} = \overline{OE} = V_{IL}$ 7/ 8/	All	9, 10, 11	0		ns
Input capacitance	C <sub>IN</sub> 9/	V <sub>IN</sub> = 0 V f = 1 MHz See 4.4.1c	All	4		12	pF
Output capacitance	C <sub>OUT</sub> 9/	V <sub>OUT</sub> = 0 V f = 1 MHz See 4.4.1c	All	4		14	pF
Functional tests		See 4.4.1e	All	7,8A,8B			

1/ Connect all address inputs and OE to V<sub>IH</sub> and measure I<sub>LO</sub> with the output under test connected to V<sub>OUT</sub>.

2/ Devices 11-20 operate at V<sub>CC</sub> = Maximum, I<sub>OUT</sub> = 0 mA, f = 5 Mhz.

3/ Device 21 operates at V<sub>CC</sub> = Maximum, I<sub>OUT</sub> = 0 mA, f = 10 Mhz.

4/ Tests for all input and control pins.

5/ Guaranteed if not tested.

6/ V<sub>PP</sub> may be one diode drop below V<sub>CC</sub>. It may be connected directly to V<sub>CC</sub>. Also, V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and be removed simultaneously or after V<sub>PP</sub>.

7/ See figures 4 and 5.

8/ Equivalent ac test conditions (actual load conditions vary by tester):

Output load: 1 TTL gate and C<sub>L</sub> = 100 pF.

Input rise and fall times ≤ 20 ns.

Input pulse levels: 0.45 V and 2.4 V.

Timing measurement reference levels:

Inputs = 0.8 V and 2.0 V.

Outputs = 0.8 V and 2.0 V.

9/ All pins not being tested are to be grounded.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

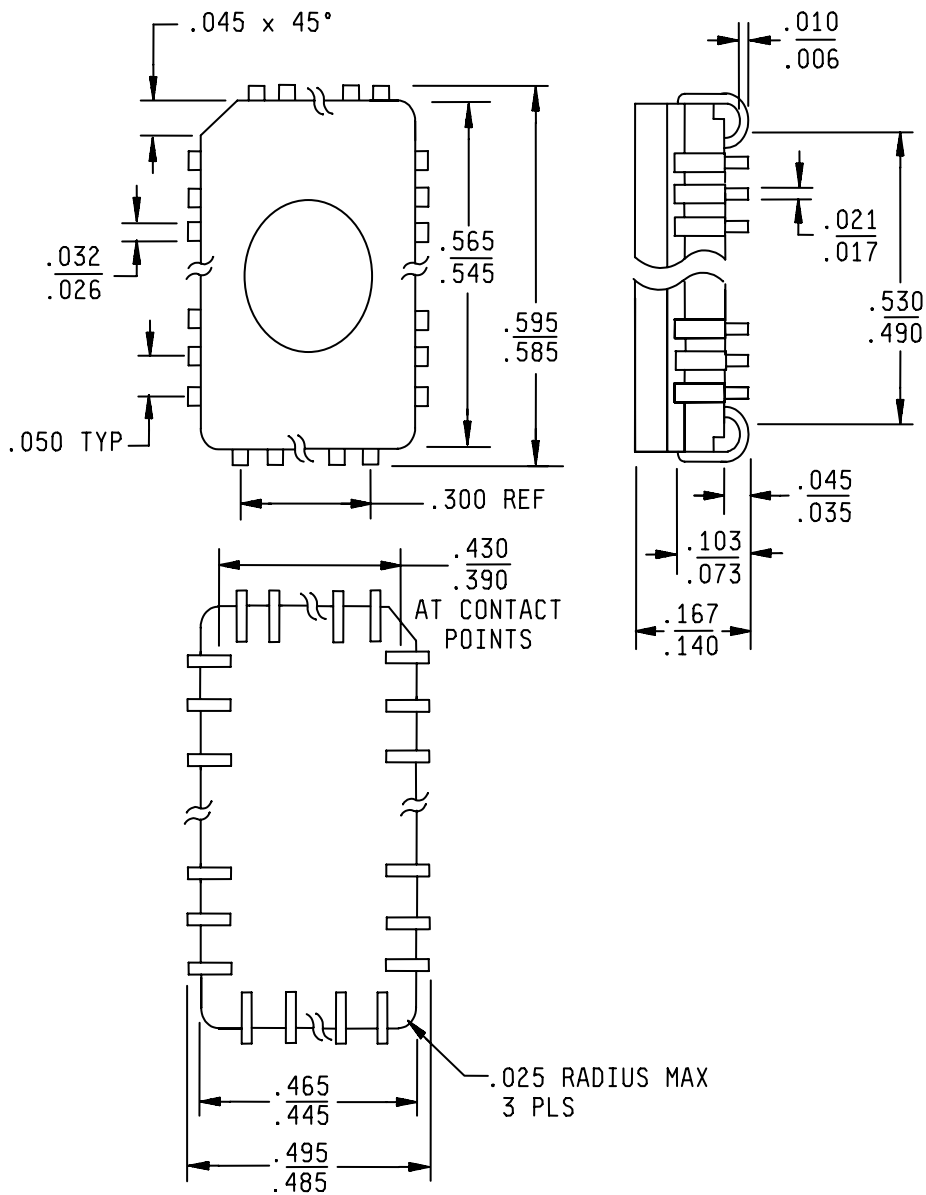
3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>7</b>

Case Z



Inches	mm
.006	0.15
.010	0.25
.017	0.43
.021	0.53
.025	0.63
.026	0.66
.032	0.81
.035	0.89
.045	1.14
.050	1.27
.073	1.85
.103	2.62
.140	3.56
.167	4.24
.300	7.62
.390	9.90
.430	10.90
.445	11.36
.465	11.83
.485	12.34
.490	12.40
.495	12.67
.530	13.53
.545	13.81
.565	14.46
.585	14.97
.595	15.11

FIGURE 1. Case outline.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>8</b>



Device types	01 thru 21	
Case outlines	X, U	Y, Z
Terminal number	Terminal symbol	
1	V <sub>PP</sub>	NC
2	A <sub>12</sub>	V <sub>PP</sub>
3	A <sub>7</sub>	A <sub>12</sub>
4	A <sub>6</sub>	A <sub>7</sub>
5	A <sub>5</sub>	A <sub>6</sub>
6	A <sub>4</sub>	A <sub>5</sub>
7	A <sub>3</sub>	A <sub>4</sub>
8	A <sub>2</sub>	A <sub>3</sub>
9	A <sub>1</sub>	A <sub>2</sub>
10	A <sub>0</sub>	A <sub>1</sub>
11	O <sub>0</sub>	A <sub>0</sub>
12	O <sub>1</sub>	NC
13	O <sub>2</sub>	O <sub>0</sub>
14	GND	O <sub>1</sub>
15	O <sub>3</sub>	O <sub>2</sub>
16	O <sub>4</sub>	GND
17	O <sub>5</sub>	NC
18	O <sub>6</sub>	O <sub>3</sub>
19	O <sub>7</sub>	O <sub>4</sub>
20	$\overline{CE}$	O <sub>5</sub>
21	A <sub>10</sub>	O <sub>6</sub>
22	$\overline{OE}$	O <sub>7</sub>
23	A <sub>11</sub>	$\overline{CE}$
24	A <sub>9</sub>	A <sub>10</sub>
25	A <sub>8</sub>	$\overline{OE}$
26	A <sub>13</sub>	NC
27	A <sub>14</sub>	A <sub>11</sub>
28	V <sub>CC</sub>	A <sub>9</sub>
29	---	A <sub>8</sub>
30	---	A <sub>13</sub>
31	---	A <sub>14</sub>
32	---	V <sub>CC</sub>

NC = no connection

FIGURE 2. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>9</b>

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$V_{PP}$ <u>2/</u>	Outputs
Read	$V_{IL}$	$V_{IL}$	$V_{CC}$	DOUT
Output disable	$V_{IL}$	$V_{IH}$	$V_{CC}$	High Z
Standby	$V_{IH}$	X <u>1/</u>	$V_{CC}$	High Z
Program	$V_{IL}$	$V_{IH}$	$V_{PP}$ <u>2/</u>	DIN
Program verify	$V_{IH}$	$V_{IL}$	$V_{PP}$ <u>2/</u>	DOUT
Program inhibit	$V_{IH}$	$V_{IH}$	$V_{PP}$ <u>2/</u>	High Z

1/ X can be either  $V_{IL}$  or  $V_{IH}$ .

2/ For  $V_{PP}$  see 4.6.

FIGURE 3. Truth table.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>10</b>

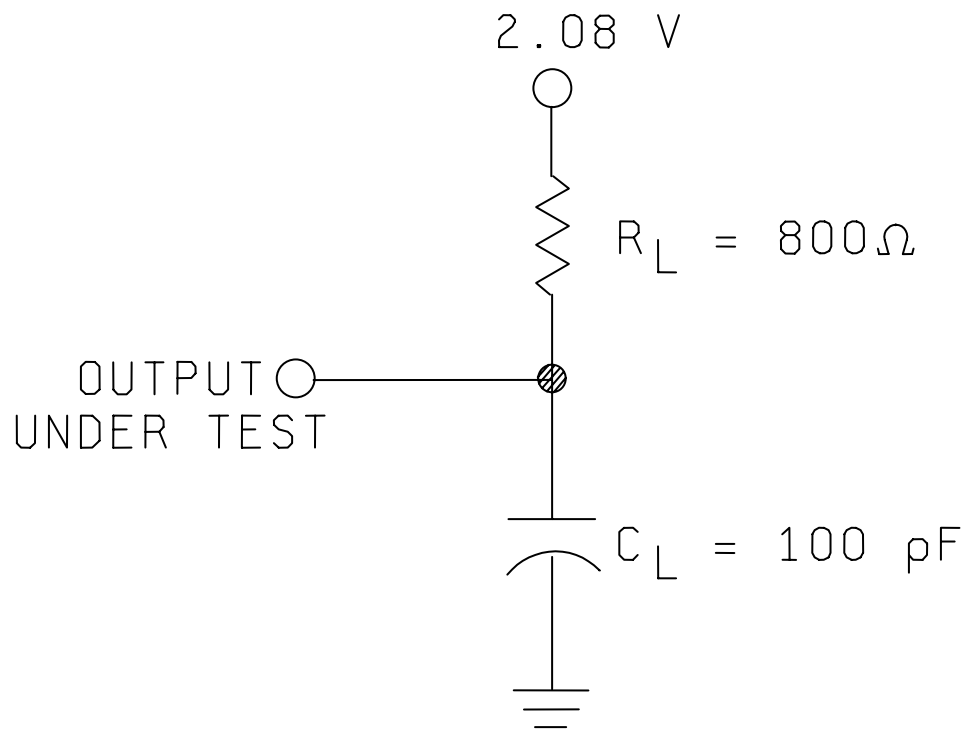
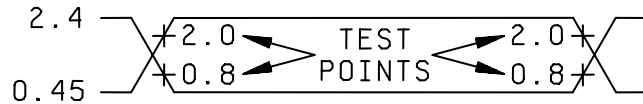


FIGURE 4. Output load circuit.

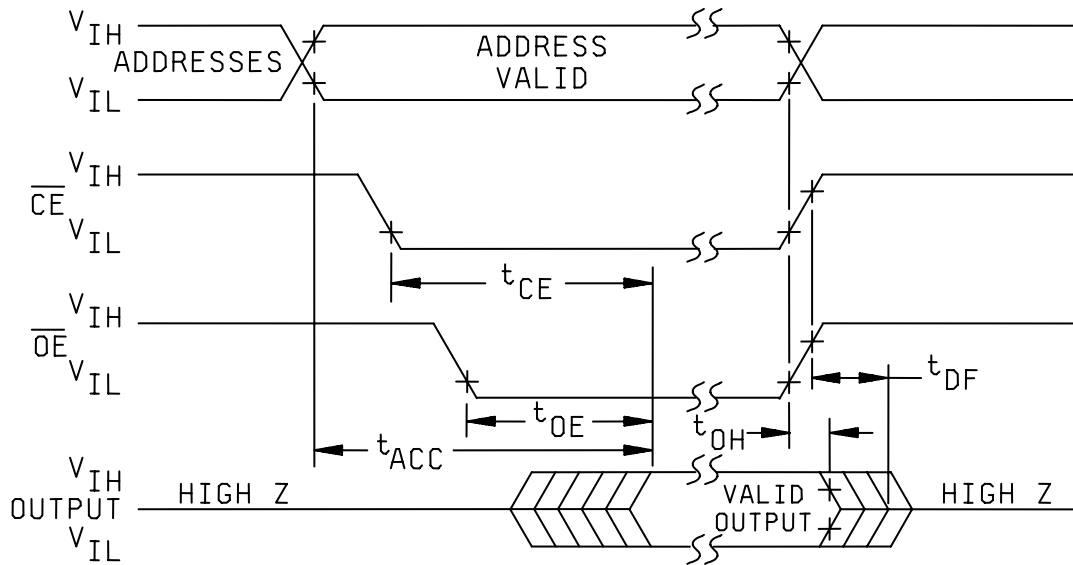
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>11</b>

### AC TESTING INPUT, OUTPUT WAVEFORM



AC TESTING: INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0".

### AC WAVEFORMS



#### Notes:

1.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
2.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .

FIGURE 5. Switching waveforms.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>12</b>

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal to 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).
- e. Subgroups 7 and 8 shall include verification of the pattern specified in 4.4.1d.

<b>STANDARD</b> <b>MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>13</b>

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Ws/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm<sup>2</sup> power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm<sup>2</sup> (1 week at 12000 μW/cm<sup>2</sup>). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.6 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	<b>SIZE A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>14</b>

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Not Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A,8B, 9	1*, 2, 3, 7*, 8A,8B, 9	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**
8	Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ (\*) indicates PDA applies to subgroups 1 and 7.

2/ (\*\*) indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

3/ (\*\*\*) see 4.4.1c.

4/ Any subgroups at the same temperature may be combined when using a multifunction tester.

5/ Subgroups 7 and 8 shall consist of verifying the applicable data pattern, see 4.4.1d.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

Table IIB. Delta limits at +25°C.

Parameter 1/	Device types All
I <sub>SB2</sub>	± 10% of the specified value in Table I
I <sub>LI</sub>	± 10% of the specified value in Table I
I <sub>LO</sub>	± 10% of the specified value in Table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>15</b>

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Symbols, definitions, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-86063</b>
		REVISION LEVEL H	SHEET <b>16</b>



STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-07-17

Approved sources of supply for SMD 5962-86063 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8606301UA	0C7V7 0C7V7	WS27C256L-20TMB AT27C256R-20/UA
5962-8606301XA	0C7V7 0C7V7 0EU86 <u>3</u> /	WS27C256L-20DMB AT27C256R-20/XA SMJ27C256-20JM MD27C256-20/B
5962-8606301YA	0C7V7 0C7V7 <u>3</u> /	WS27C256L-20CMB AT27C256R-20/YA MR27C256-20/B
5962-8606301YC	0C7V7 0C7V7	WS27C256L-20CMB AT27C256R-20/YC
5962-8606301ZA	<u>3</u> /	AT27C256R-20KM/883
5962-8606302UA	0C7V7 0C7V7	WS27C256L-25TMB AT27C256R-25/UA
5962-8606302XA	0C7V7 0C7V7 0EU86 <u>3</u> /	WS27C256L-25DMB AT27C256R-25/XA SMJ27C256-25JM MD27C256-25/B
5962-8606302YA	0C7V7 0C7V7 <u>3</u> /	WS27C256L-25CMB AT27C256R-25/YA MR27C256-25/B
5962-8606302YC	0C7V7 0C7V7	WS27C256L-25CMB AT27C256R-25/YC
5962-8606302ZA	<u>3</u> /	AT27C256R-25KM/883
5962-8606303UA	0C7V7 0C7V7	WS27C256L-30TMB AT27C256R-30/UA
5962-8606303XA	0C7V7 0C7V7 0EU86 <u>3</u> /	WS27C256L-30DMB AT27C256R-30/XA SMJ27C256-30JM MD27C256-30/B
5962-8606303YA	0C7V7 0C7V7 <u>3</u> /	WS27C256L-30CMB AT27C256R-30/YA AT27C256R-30LM/883

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8606303YC	0C7V7 0C7V7	WS27C256L-30CMB AT27C256R-30/YC
5962-8606303ZA	<u>3</u> /	AT27C256R-30KM/883
5962-8606304UA	0C7V7 0C7V7	WS27C256L-17TMB AT27C256R-17/UA
5962-8606304XA	0C7V7 0C7V7 0EU86 <u>3</u> /	WS27C256L-17DMB AT27C256R-17/XA SMJ27C256-17JM MD27C256-17/B
5962-8606304YA	0C7V7 0C7V7 <u>3</u> /	WS27C256L-17CMB AT27C256R-17/YA MR27C256-17/B
5962-8606304YC	0C7V7 0C7V7	WS27C256L-17CMB AT27C256R-17/YC
5962-8606304ZA	<u>3</u> /	AT27C256R-17KM/883
5962-8606305UA	0C7V7 0C7V7	WS27C256L-15TMB AT27C256R-15/UA
5962-8606305XA	0C7V7 0C7V7 0EU86 <u>3</u> /	WS27C256L-15DMB AT27C256R-15/XA SMJ27C256-15JM MD27C256-15/B
5962-8606305YA	0C7V7 0C7V7 <u>3</u> /	WS27C256L-15CMB AT27C256R-15/YA MR27C256-15/B
5962-8606305YC	0C7V7 0C7V7	WS27C256L-15CMB AT27C256R-15/YC
5962-8606305ZA	<u>3</u> /	AT27C256R-15KM/883
5962-8606306UA	0C7V7	AT27C256R-12/UA
5962-8606306XA	0C7V7 0C7V7 0EU86	WS27C256L-12DMB AT27C256R-12/XA AS27C256-12JM
5962-8606306YA	0C7V7 0C7V7 0EU86	WS27C256L-12CMB AT27C256R-12/YA AS27C256-12ECAM
5962-8606306YC	0C7V7 0C7V7	WS27C256L-12CMB AT27C256R-12/YC
5962-8606306ZA	<u>3</u> /	AT27C256R-12KM/883
5962-8606307UA	0C7V7	AT27C256R-90/UA
5962-8606307XA	0C7V7 0EU86 <u>3</u> /	AT27C256R-90/XA AS27C256-90JM AT27C256R-90DM/883

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8606307YA	0C7V7 0EU86 <u>3</u> /	AT27C256R-90/YA AS27C256-90ECAM AT27C256R-90LM/883
5962-8606307YC	0C7V7	AT27C256R-90/YC
5962-8606307ZA	<u>3</u> /	AT27C256R-90KM/883
5962-8606308UA	0C7V7	AT27C256R-70/UA
5962-8606308XA	0C7V7 0C7V7 0EU86 <u>3</u> /	AT27C256R-70/XA 57C256F-70 AS27C256-70JM WS57C256F-70DMB
5962-8606308YA	0C7V7 0C7V7 0EU86 <u>3</u> /	AT27C256R-70/YA 57C256F-70 AS27C256-70ECAM AT27C256R-70LM/883
5962-8606308YC	0C7V7 0C7V7 <u>3</u> /	AT27C256R-70/YC 57C256F-70 WS57C256F-70CMB
5962-8606308ZA	<u>3</u> /	AT27C256R-70KM/883
5962-8606309UA	0C7V7 0C7V7 <u>3</u> /	AT27C256R-55/UA 57C256F-55 WS57C256F-55TMB
5962-8606309XA	0C7V7 0C7V7 0EU86 <u>3</u> /	AT27C256R-55/XA 57C256F-55 AS27C256-55JM WS57C256F-55DMB
5962-8606309YA	0C7V7 0C7V7 0EU86 <u>3</u> /	AT27C256R-55/YA 57C256F-55 AS27C256-55ECAM WS57C256F-55CMB
5962-8606309YC	0C7V7 0C7V7	AT27C256R-55/YC 57C256F-55
5962-8606310UA	0C7V7 0C7V7 <u>3</u> /	AT27C256R-45/UA 57C256F-45 WS57C256F-45TMB
5962-8606310XA	0C7V7 0C7V7 <u>3</u> /	AT27C256R-45/XA 57C256F-45 WS57C256F-45DMB
5962-8606310YA	0C7V7 0C7V7 <u>3</u> /	AT27C256R-45/YA 57C256F-45 WS57C256F-45CMB
5962-8606310YC	0C7V7 0C7V7	AT27C256R-45/YC 57C256F-45

See footnotes at end of table.

## STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8606311QXA	<u>3</u> /	CY27C256A-200WMB
5962-8606311QYA	<u>3</u> /	CY27C256A-200QMB
5962-8606311UA	0C7V7	AT27C256R-20/UA
5962-8606311XA	0C7V7	AT27C256R-20/XA
5962-8606311YA	0C7V7	AT27C256R-20/YA
5962-8606312QXA	<u>3</u> /	CY27C256A-250WMB
5962-8606312QYA	<u>3</u> /	CY27C256A-250QMB
5962-8606312UA	0C7V7	AT27C256R-25/UA
5962-8606312XA	0C7V7	AT27C256R-25/XA
5962-8606312YA	0C7V7	AT27C256R-25/YA
5962-8606313QXA	<u>3</u> /	CY27C256A-300WMB
5962-8606313QYA	<u>3</u> /	CY27C256A-300QMB
5962-8606313UA	0C7V7	AT27C256R-30/UA
5962-8606313XA	0C7V7	AT27C256R-30/XA
5962-8606313YA	0C7V7	AT27C256R-30/YA
5962-8606314QXA	<u>3</u> /	CY27C256A-170WMB
5962-8606314QYA	<u>3</u> /	CY27C256A-170QMB
5962-8606314UA	0C7V7	AT27C256R-17/UA
5962-8606314XA	0C7V7	AT27C256R-17/XA
5962-8606314YA	0C7V7	AT27C256R-17/YA
5962-8606315QXA	<u>3</u> /	CY27C256A-150WMB
5962-8606315QYA	<u>3</u> /	CY27C256A-150QMB
5962-8606315UA	0C7V7	AT27C256R-15/UA
5962-8606315XA	0C7V7	AT27C256R-15/XA
5962-8606315YA	0C7V7	AT27C256R-15/YA
5962-8606316QXA	<u>3</u> /	CY27C256A-120WMB
5962-8606316QYA	<u>3</u> /	CY27C256A-120QMB
5962-8606316UA	0C7V7	AT27C256R-12/UA
5962-8606316XA	0C7V7	AT27C256R-12/XA
5962-8606316YA	0C7V7	AT27C256R-12/YA
5962-8606317QXA	<u>3</u> /	CY27C256A-90WMB
5962-8606317QYA	<u>3</u> /	CY27C256A-90QMB
5962-8606317UA	0C7V7	AT27C256R-90/UA
5962-8606317XA	0C7V7	AT27C256R-90/XA
5962-8606317YA	0C7V7	AT27C256R-90/YA
5962-8606318QXA	<u>3</u> /	CY27C256A-70WMB
5962-8606318QYA	<u>3</u> /	CY27C256A-70QMB
5962-8606318UA	0C7V7	AT27C256R-70/UA
5962-8606318XA	0C7V7	AT27C256R-70/XA
5962-8606318YA	0C7V7	AT27C256R-70/YA

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8606319QXA	<u>3/</u>	CY27C256A-55WMB
5962-8606319QYA	<u>3/</u>	CY27C256A-55QMB
5962-8606319UA	0C7V7	AT27C256R-55/UA
5962-8606319XA	0C7V7	AT27C256R-55/XA
5962-8606319YA	0C7V7	AT27C256R-55/YA
5962-8606320QXA	<u>3/</u>	CY27C256A-45WMB
5962-8606320QYA	<u>3/</u>	CY27C256A-45QMB
5962-8606321QXA	<u>3/</u>	CY27H256A-35WMB
5962-8606321QYA	<u>3/</u>	CY27H256A-35QMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number

Vendor name and address

0C7V7

QP Semiconductor  
2945 Oakmead Village Court  
Santa Clara, CA 95051

0EU86

Austin Semiconductor Inc.  
8701 Cross Park Dr.  
Austin, TX 78754-4566

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