STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCT SERIES 7-Channel Switching Regulator Controller for Digital Camera

TYPE **BD9745EKN**

PACKAGE Fig. 1 (Plastic mold) HQFN-48U package
PIN ASSIGNMENT Fig. 2
BLOCK DIAGRAM Fig. 3
APPLICATION CIRCUIT Fig. 4

FEATURES
- 1.5V Minimum input operating.
- Controls up to 7 switching regulators. Step up converter (1channel), Step-down converter (1channel), Configurable for Step-up or Step-down conversion (3channels), Positive to negative converter (1channel), Step-up converter for LED (1channel).
- Synchronous rectifying action mode (4channel), Built-in FET Transistor.
- Step-up converter for CCD,Built-in FET Transistor.
- Internal compensation.
- Operating frequency 1.2MHz(CH1～4), 600kHz(CH5～7).
- Short Circuit Protection(SCP) for Over load condition.
- Built-in load switch with soft-start for Step-up converter(CH6,7).
- Back gate control synchronous rectified DC/DC for Step-up(CH1,2,4).
- Thermally enhanced QFN48 package. (7mmX 7mm, 0.4mm pitch)

Absolute maximum ratings（Ta=25°C）

Parameter	Symbol	Limits	Units
Power Supply Voltage	VBAT, VCC, PVCC	−0.3～7	V
Power Input Voltage	PVCC5, HS6H, HS7H	−0.3～7	V
	VHx1～4	−0.3～7	V
	VLx1～4	−0.3～7	V
	VLx6	−0.3～18	V
Output Current	IomaxLx1	±1.8	A
	IomaxLx2～4	±1.5	A
Power Dissipation	Pd	0.65(*1)	W
		1.50(*2)	W
Operating Temperature	Topr	−25～+85	°C
Storage Temperature	Tstg	−55～+150	°C
Junction Temperature	Tjmax	+150	°C

(*1) Without external heat sink, the power dissipation reduces by 5.2mW/°C over25°C.

(*2) Reduced by 12mW/°C over 25°C, when mounted on a PCB (70.0mm × 70.0mm × 1.6mm).

Recommended operating conditions

Parameter	Symbol	Spec.	Units
Power Supply Voltage	VBAT	1.5 ～ 5.5	V
	VCC, PVCC	2.5 ～ 5.5	V

○ Recommended operating conditions

Parameter	Symbol	Standard value			Units	Conditions
		MIN	TYP	MAX		
VREF Pin Connect Capacitor	CVREF	0.47	1.0	4.7	μF	
VREGA Pin Connect Capacitor	CVREGA	0.47	1.0	4.7	μF	
SCP Pin Connect Capacitor	Cscp	-	-	0.47	μF	
【Oscillator】						
Oscillator Frequency	fosc	0.6	1.2	1.5	MHz	
OSC Timing Resistor	RT	47	62	120	kΩ	
【Driver】						
P-channel Drain Current(CH1～4)	Idpl	-	-	1.5	A	
N-channel Drain Current(CH1～4)	Idnl	-	-	1.5	A	
N-channel Drain Current (CH6)	Idnh	-	-	1.0	A	
P-channel Drain Current (Load SW of CH6～7)	Idpr	-	-	1.5	A	
Driver Peak Current (CH5, 7)	Idpeak	-	-	500	mA	

○Electrical characteristics（Ta=25℃, VBAT=3V, VCC=5V, RT=62kohm, STB1～7=3V）

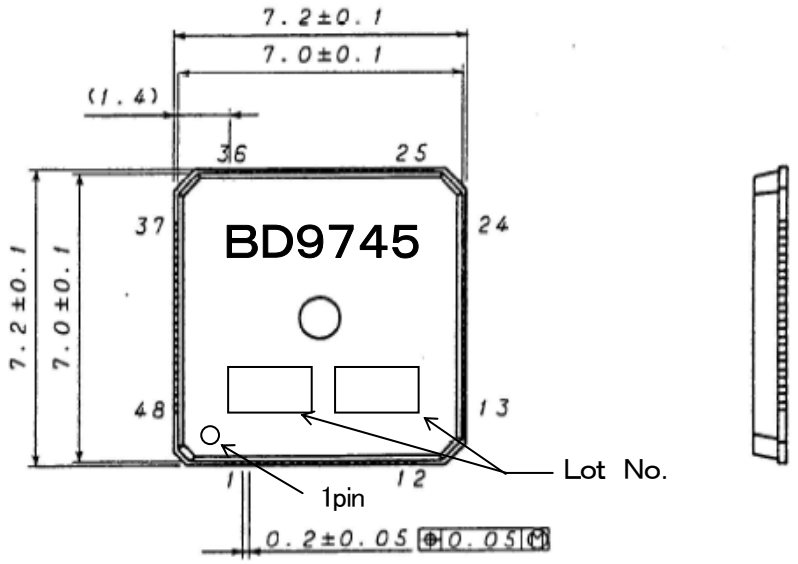
Parameter	Symbol	Spec.			Units	Conditions.	Test Circuit
		Min.	Typ.	Max			
【 Reference Voltage for CH5 】							
Reference Voltage	Vref5	0.99	1.00	1.01	V	STB5=3V	
Line Regulation	DVLi	-	4.0	12.5	mV	Vcc=2.8V～5.5V	
Load Regulation	DVLo	-	1.0	7.5	mV	Iref=10μA～100μA	
Short Circuit Output Current	Ios	0.2	1	-	mA	Vref=0V	
【 Internal Regulator 】							
REGA Output Voltage	VREGA	2.4	2.5	2.6	V	Ireg=5mA	
【 Low Voltage Input Prevented Operation Faults Circuit 】							
Threshold Voltage 2	Vstd2	2.3	2.4	2.5	V	VCC monitor	
Hysteresis width 2	ΔVst2	100	200	300	mV		
Threshold Voltage 3	Vstd3	1.6	2.0	2.3	V	VREGA monitor	
Hysteresis width 3	ΔVst3	100	200	300	mV		
【 Start up Circuit 】							
Oscillator Frequency	Fstart	150	300	600	kHz		
Minimum VBAT Voltage	Vst1	1.5	-	-	V		
Soft-start time	Tss1	2.6	4.2	7.4	msec		
【 Soft-Start 】							
Soft-start time (CH2～4,CH6,7)	Tss4	6.8	8.5	10.2	msec		
Soft-start time CH5	Tss3	5.8	7.7	9.6	msec	VREF5monitor	
【 Protection Circuit 】							
Timer Start Threshold Voltage	Vtcfb	2.1	2.2	2.3	V	Error Amp Output monitor CH1,5～7	
Timer Start Threshold Voltage	Vtcinv	0.56	0.64	0.72	V	INV monitor CH2～4	
SCP Standby Voltage	Vssc	-	22	170	mV		
SCP Output Current	Iscp	2	4	6	μA	VSCP=0.1V	
SCP Threshold Voltage	Vscp	0.9	1.0	1.1	V		
【 Triangular wave oscillator 】							
Oscillator Frequency CH1～4	fosc1	1.0	1.2	1.4	MHz	RT=62kohm	
Oscillator Frequency CH5～7	fosc2	500	600	700	kHz	RT=62kohm	
【 Error Amp 】							
Input Bias Current	Iinv	-5	0	5	μA	INV1~4,6,7,7I,NON5=7.0V	
INV Threshold	VINV	0.79	0.80	0.81	V	CH1～4,CH6,7V	
NON5 Threshold	VINV5	-12	0	12	mV	CH5	
INV7I Threshold	VINV7I	380	400	420	mV	CH7I	
【 PWM Comparator 】							
MAX DUTY1, 2,3,4	Dmax2	86	92	97	%		
MAX DUTY5, 6,7	Dmax4	77	85	93	%		

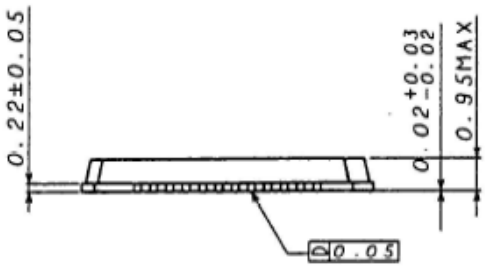
◎This product is not designed for normal operation within a radioactive environment.

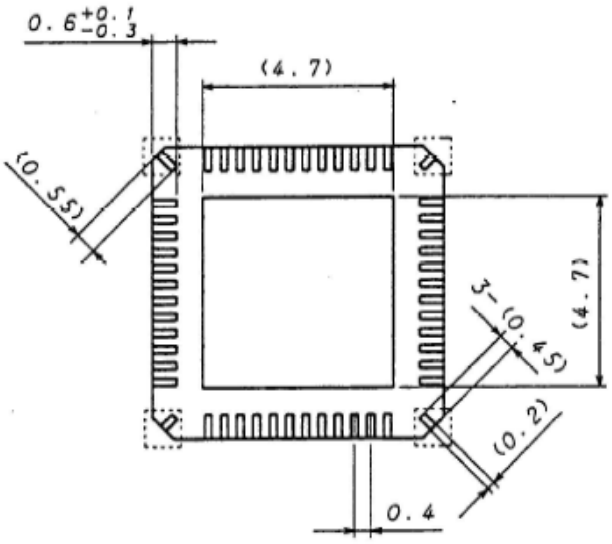
○Electrical characteristics（Ta=25℃, VBAT=3V, VCC=5V, RT=62kohm, STB1～7=3V）

Parameter		Symbol	Spec.			Units	Conditions	Test Circuit
			Min	Typ.	Max.			
【 Output Circuit 】								
CH1,2,3,4 Pch FET ON Resistor		Ronlp	-	250	350	mΩ	Hx=5V	
CH1 Nch FET ON Resistor		Ron1n	-	80	120	mΩ	PVCC=5V	
CH2,3,4 Nch FET ON Resistor		Ron2n	-	130	200	mΩ	PVCC=5V	
CH6,7 Load SW ON Resistor		Ronl	-	250	350	mΩ	HS6, 7H=5V	
CH6 Nch FET ON Resistor		Ronh	-	450	700	mΩ	PVCC=5V	
OUT5 High-level Output Voltage ON Driving		VOUT5H	PVCC5 -1.0	PVCC5 -0.5	-	V	PVCC5=5V,IOUT5=50mA NON5=0.2V	
OUT5 Low-level Output Voltage ON Driving		VOUT5H	-	0.5	1.0	V	PVCC5=5V,IOUT5= - 50mA NON5=-0.2V	
OUT7 High-level Output Voltage ON Driving		VOUT7H	PVCC -1.0	PVCC -0.5	-	V	PVCC=5V,IOUT7=50mA INV7I=0V,INV7=0.4V	
OUT7 Low-level Output Voltage ON Driving		VOUT7H	-	0.5	1.0	V	PVCC=5V,IOUT7= - 50mA INV7I=0.6V,INV7=1.2V	
【 Step-up / down Selection 】								
UDSEL12, UDSEL3 Control Voltage	Step down	VUDDO	VBAT × 0.7	-	VBAT	V		
	Step up	VUDUP	0	-	VBAT ×0.3	V		
【STB1～7】								
STBControl Voltage	ON	VSTBH1	1.5	-	5.5	V		
	OFF	VSTBL1	-0.3	-	0.3	V		
STB Pull-down Resistor		RSTB1	250	400	700	KΩ		
【 Circuit Current 】								
Stand by Current	VBAT	ISTB1	-	-	5	μA		
	VCC, PVCC	ISTB2	-	-	5	μA		
	Hx	ISTB3	-	-	5	μA	Step-down UDSEL1, 2,4=VBAT	
	Lx	ISTB4	-	-	5	μA	Step-up UDSEL1, 2,4=0V	
Start up Current (VBAT Sink Current)		IST	-	300	1000	μA	VBAT=1.5V	
Circuit Current on Driving 1 (VBAT Sink Current)		Icc1	-	200	400	μA	VBAT=3.0V	
Circuit Current on Driving 2 （VCC,PVCC Sink Current）		Icc2	-	4.8	8.5	mA	STB1～7=3V INV=2.5V	

◎This product is not designed for normal operation within a radioactive environment.







(UNIT:mm)

Notice : Do not use the dotted line area
For soldering

Fig. 1 PACKAGE
Fig. 2 PIN ASSIGNMENT

OPIN DESCRIPTION

PIN No.	NAME	I/O	Description	NOTES
22	VBAT	−	Power supply for the start-up circuit	Drive over 1.5V
31	VCC	−	Power supply	Drive over 2.5V
21	PVCC	−	Power supply for Nch Driver	Drive over 2.5V
2	PVCC5	−	Power supply for CH5 Pch Driver.	
33	GND	−	Ground	
17−18,6−7,43	PGND12,34,567	−	Power Ground for the Built-in FET.	
30	VREGA	O	Output of REGA	Output Voltage=2.5V
34	VREF	O	Output of CH5 Reference.	Output Voltage=1.0V
1	OUT5	O	Connect to the Gate of CH5 external Pch FET.	
42	OUT7	O	Connect to the Gate of CH7 external Nch FET.	
14,20,9,4	Hx1,2,3,4	O	Power supply for Built-in Pch FET.	
15−16,19,8,5,44	Lx1,2,3,4,6	O	Connect to the inductor.	
46,40	HS6H, HS7H	I	Power supply for Built-in High side-SW.	
45,41	HS6L, HS7L	O	Output of Built-in High side-SW.	
26,25,27,28,36,38	INV1,2,3,4,6,7	I	Error AMP inverted input.	
35	NON5	I	Error AMP non-inverted input.	
37	INV7I	I	Error AMP inverted input.	For Current Feed Back
29	RT	−	A resistor is placed to set the OSC frequency.	Output Voltage=1.0V CLK frequency 1.2MHz connecting 62kΩ to GND.
32	SCP	−	Connect to a capacitor to set up the delay time of the SCP.	Charge up current 4μA until 1.0V.
23,24,3	UDSEL1,2,4	I	Step-up/down switching mode selection H: step-down L: step-up	
13,12,11,10,48,47,39	STB1,2,3,4,5,6,7	I	ON/OFF SW H: Operating Over 1.5V	All Low; Stand-by

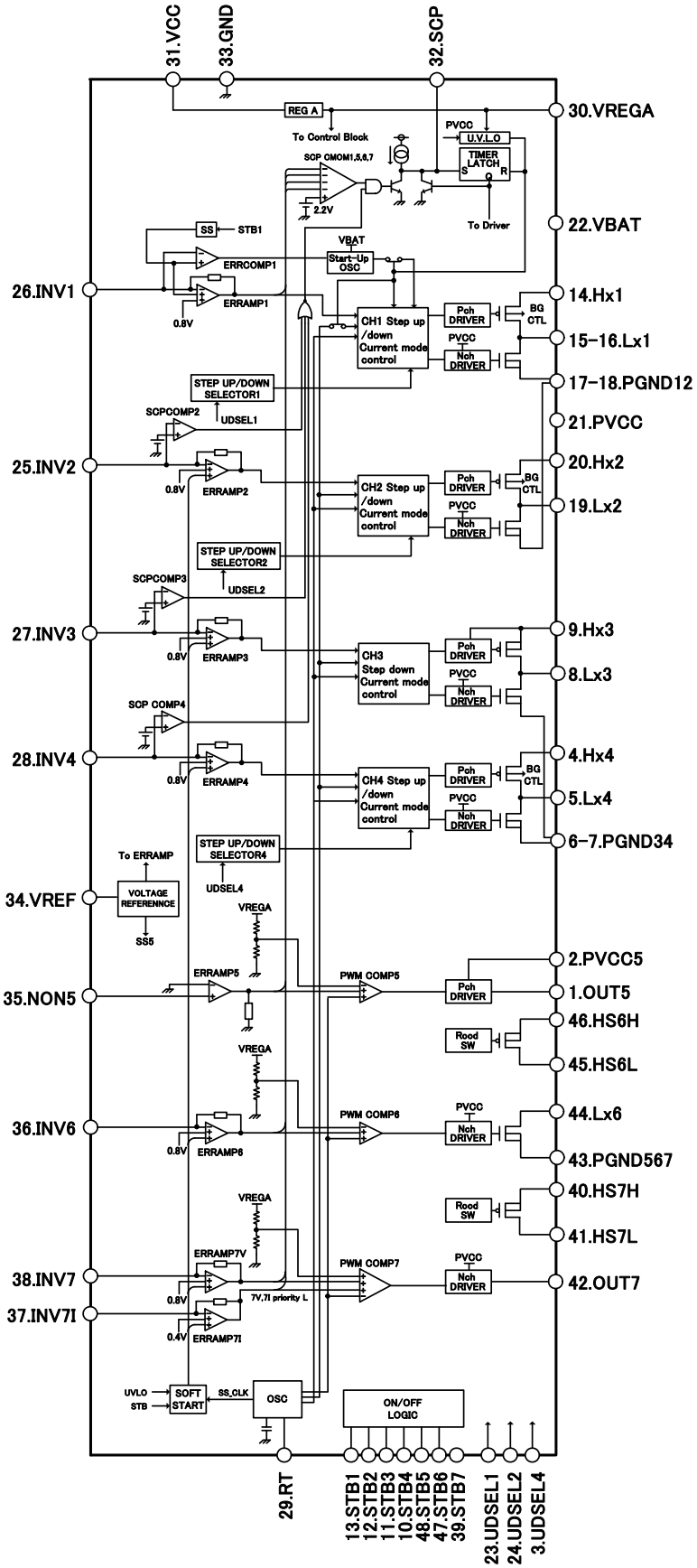


Fig. 3 Block diagram

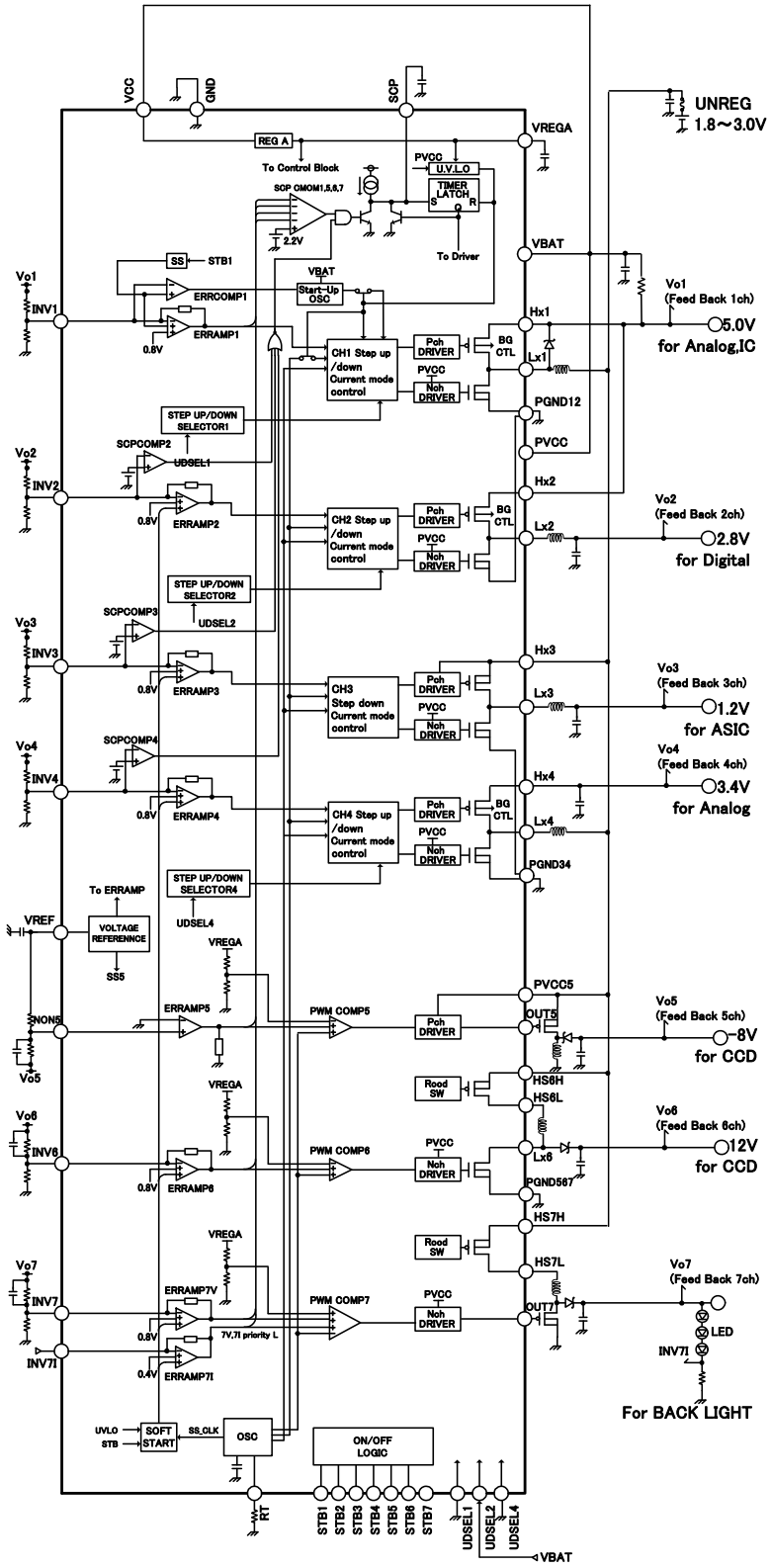


Fig. 4（1） Application Circuit for NiH_2 2cell

※ Note

The following application circuit is recommended. Make sure to confirm its characteristics.
When making changes to the external components, make sure to leave adequate margin
such as static and transitional characteristics, as well as dispersion of the IC.

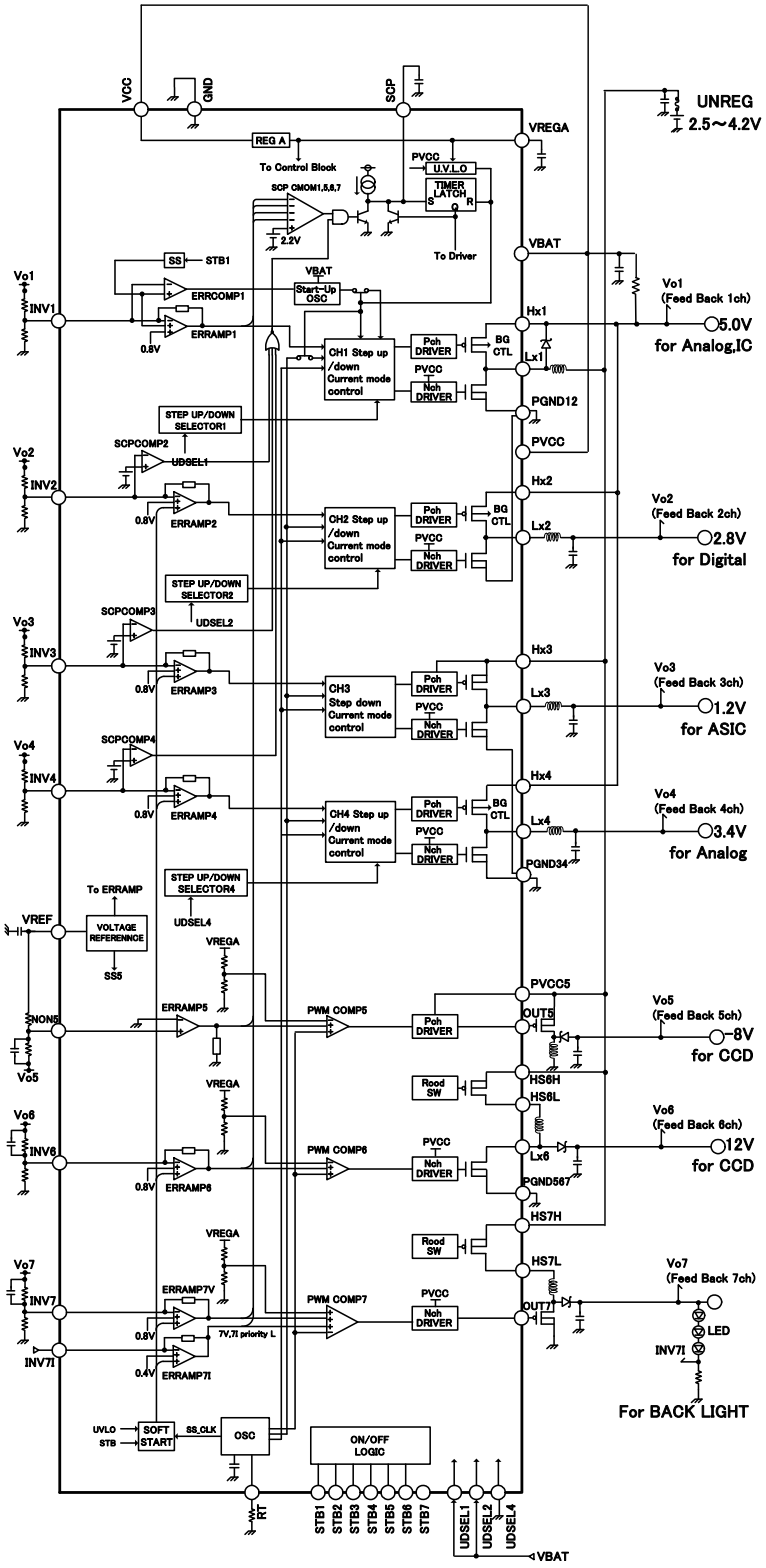
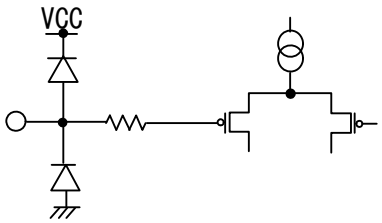
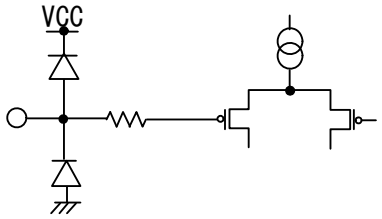
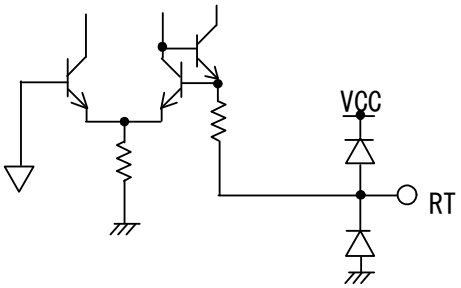
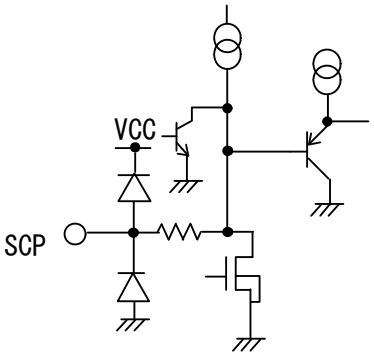


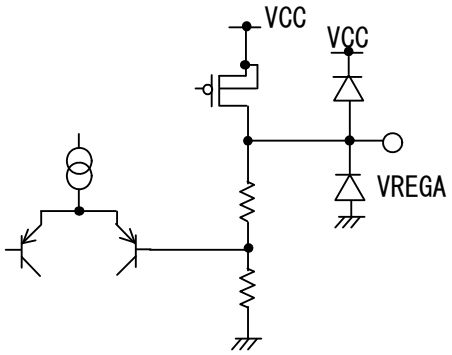
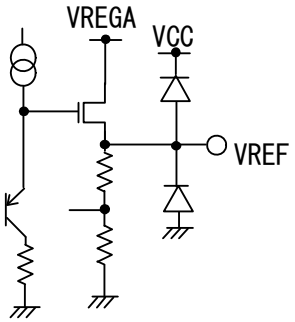
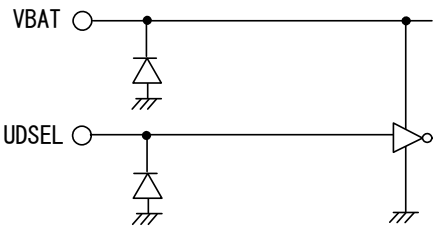
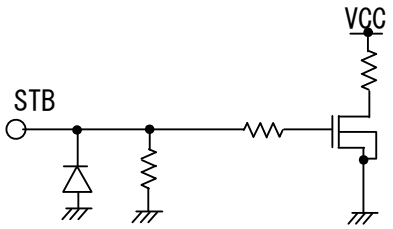
Fig. 4（2） Application Circuit for Li battery 1cell

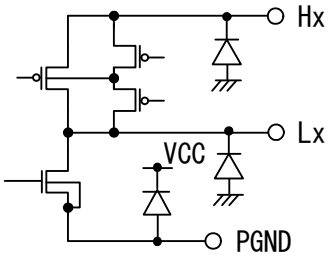
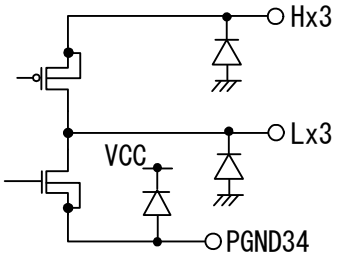
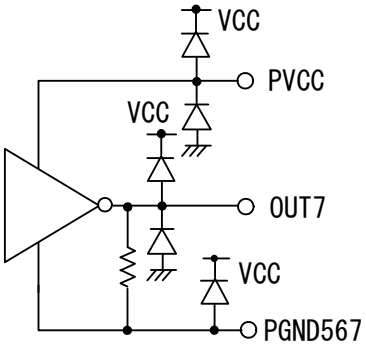
※ Note

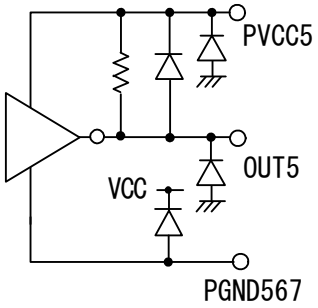
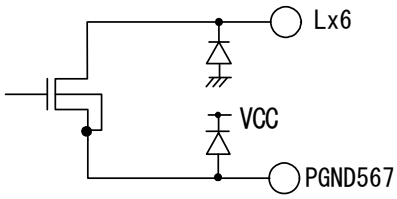
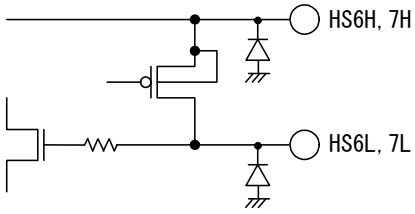
The following application circuit is recommended. Make sure to confirm its characteristics.
When making changes to the external components, make sure to leave adequate margin
such as static and transitional characteristics, as well as dispersion of the IC.

○ I/O Equivalent Circuit Diagrams

Pin. No	Pin Name	Input/ Output	Description	Pin circuit	Note
26 25 27 28 36 38 37	INV1 INV2 INV3 INV4 INV6 INV7 INV7I	I I I I I I I	Error amp inverting input pin.		
35	NON5	I	Error amp non-inverting input pin.		
29	RT	—	Connect to resistor to set up the OSC frequency.		
32	SCP	—	Connect to capacitor to set up the delay time for the timer-latch.		

Pin. No	Pin Name	Input/ Output	Description	Pin circuit	Note
30	VREGA	O	REGA output voltage		
34	VREF	O	Reference voltage for CH5.		
23 24 3 22	UDSEL1 UDSEL2 UDSEL4 VBAT	I I I –	Step-up/down switching mode selection H= Step-down L= Step-up Battery input.		
13 12 11 10 48 47 39	STB1 STB2 STB3 STB4 STB5 STB6 STB7	I I I I I I I	CH1～7 ON/OFF Switches, High = Operating		

Pin. No	Pin Name	Input/ Output	Description	Pin circuit	Note
14,20,4 15, −16,19,5 17−18,6−7	Hx1, 2,4 Lx1, 2,4 PGND12, 34	O O −	Pch FET source. Nch, Pch FET Drain. Ground.		
9 8	Hx3 Lx3	O O	Pch FET source Nch, Pch FET Drain		
21 42 43	PVCC OUT7 PGND567	− O − 	Power supply for Nch Driver. Connect to the gate of CH7 external Nch FET. Ground.		

Pin. No	Pin Name	Input/ Output	Description	Pin circuit	Note
2 1 43	PVCC5 OUT5 PGND567	– O –	Power supply for Driver. Connect to the gate of CH5 external Pch FET. Ground.		
44 45	Lx6 PGND567	O –	Nch FET Drain.		
46,40 45,41	HS6H, 7H HS6L, 7L	I O	Input of PMOS High-side SW. Output of PMOS High-side SW.		

○ BLOCK DESCRIPTION

1. REGA

This is an internal regulator that generates a 2.5V regulated output voltage.
REGA supplies power for all the remaining circuit blocks.
The output voltage can be supplied to external devices from VREGA (30pin).
To prevent any oscillations at the output, a 1μF external capacitor is recommended.

2. Short Circuit Protect, Timer Latch

When Error Amp's output of CH1,5～7 voltages rise beyond 2.2 V, or INV pin voltage of CH2,3,4 fall under 80% of reference, the timer circuit is activated. This will charge up the capacitor connected to SCP (32pin) by approximately 4μA current.
When the voltage reaches 1.0 V, the latch circuit is activated. While this protection circuit is activated, the entire channel's output is turned OFF.
In order to reset the latch circuit, two methods can be used: 1) disable the STB pin before enabling it.
2) Removing or refreshing the power supply voltage.

3. U.V.L.O

This circuit protects the IC from a transient surge at power-on or a momentary drop of the power supply voltage. Under voltage lockout is activated when the VCC pin voltage falls below 2.4V.
During activation, the output drive pins for all Channels is turned OFF.

4. VOLTAGE REFERENCE (VREF)

The reference voltage circuit for CH5 generates a 1.0V output voltage. The reference voltage can be supplied from VREF (34pin).
This reference voltage is used to set the output voltage of CH5. When STB5 is enable, the reference is ramping to 1V. Inverting voltage of CH5 is following this reference.
To prevent any oscillations at the output, a 1μF external capacitor is recommended.

5. OSC

The BD9745EKN include a triangular waveform oscillator for voltage-mode PWM controllers, and slope oscillator for current-mode PWM controllers.
To set the oscillator frequency, connect a timing resistor to the RT (29 pin).
When the resistor is 62kΩ, it is set 1.2MHz(CH1～4), 600kHz(CH5～7).

6. SOFT START , SS1

The circuit prevents inrush current in startup by ramping DC/DC output voltage.
The soft-start time of each channel is designed below.

a. CH1・・・・・・・Typical IC Design's output startup time is 4.2msec. Only CH1, the startup time doesn't depend on OSC frequency.

b. CH5・・・・・・・The soft start function of CH5 is accomplished by ramping the VREF pin (30pin) from 0V to 1V over period of about 10000 SLOPE cycle(7.7msec at 1.2MHz).

c. CH2,3,4,6,7・・・The soft start function of these channel is accomplished by internal reference over period of about 10000 SLOPE cycle(8.5msec at 1.2MHz).

7. ERRAMP 1～7

This amplifier monitors the output voltage of the switching regulator channels and outputs a PWM controlled signal accordingly.
ERRAMP1, 2,3,4,6,7's reference voltage is set by applying voltage of 0.8V. ERRAMP5's reference voltage connected to GND, ERRAMP7I's reference voltage is set to 0.4V.
And all channels have the R-C component for internal compensation.

8. ERRCOMP , Start Up OSC

The Error Comparator monitors the output voltage of the switching regulator and outputs a PFM controlled signal accordingly. The Start Up OSC operates when power supply voltage reaches 1.5V, and is switched ON/OFF by output of ERRCOMP. This OSC oscillates at around 300kHz.
When VCC voltage is above 2.6V, or CH1 soft-start time is over, this circuit stops to oscillate.

9. Current mode control block

DC/DC converter of CH1～4 operates on current-mode PWM. In current-mode PWM controller, Main FET turn on to detect CLK edge, and turn off to detect a peak current of inductor.
Using UDSEL pins, DC/DC converter of CH1～4 is switched to Step-up converter or Step-down converter.

10. PWM COMP

The PWM comparators are voltage - pulse width converters that control the output pulse on time according to the input voltage. The circuit supplies a pulse width controlled signal to the driver, by comparing the triangular wave oscillator with the error amplifier's output voltage.
The maximum on-duty is established internally at approximately 85%.

11. Nch DRIVER

This CMOS inverting output circuit is a Driver block with built-in and external Nch FET. PVCC pin voltage for DRIVER must have same voltage with VCC pin voltage for main block.

12. Pch DRIVER

This CMOS inverting output circuit is a Driver block with built-in and external Pch FET.

13. Road SW

This circuit controls high-side load switch with CH6, 7. HS6H, 7H (40,46pin) is input, and HS6L, 7L (41,45) is output. This circuit controls by ramping the HS6L, 7L voltage on startup to decrease in-rush current.

14. Back gate Control

This circuit controls to switch back-gate voltage of Built-in Pch-FET. (CH1, 2,4) In monolithic IC of P-Sub, the parasitic diode remains between back-gate (cathode), and source, drain (anode). This circuit cut current pass through the parasitic diode in step-up situation on STB OFF.

15. ON/OFF LOGIC

The output of each channel can be turned on and off by the input voltage applied on the STB pin.
The channel is “ON” when the voltage of the STB pin is above 1.5 V.
The channel is “OFF” when the voltage applied at STB pin is 0 V or the pin is left open.
When all channels are “OFF”, the device is at Stand-by State.
Each logic pin is connected to GND via a 400kΩpull-down resistor.

16. UDSEL LOGIC

The output of CH1, 2, 4 can be switched step-down/up by input voltage applied on the UDSEL pin.
The output is at step-up mode when UDSEL is GND, and step-down mode when UDSEL is VBAT.
UDSEL pin must be connected to GND or VBAT to prevent unstable logic state, due to this logic is CMOS inverter powered VBAT.

OAPPLICATION INFORMATION

1.) CH1 Start up sequence.

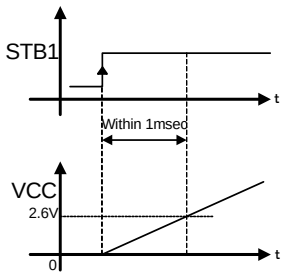
Using step up function in CH1, please take below measure to prevent operation faults and destruction on start-up.

a : CH1 output input to VCC

It must be put schottky Di between Lx1 and Hx1 to clamp Lx1 voltage the input of VBAT pin must short to VCC line and input through C-R filter. (Ref Fig-7)

b : A battery input to VCC, or external power supply input to VCC.（Fig－5）

The ERRCOMP circuit that adjust CH1 output voltage on UVLO condition, switches Lx1 NMOS ON/OFF to compare INV1 and soft-start output. In this circuit, if it is late to switch from start up OSC to main current mode control, it is possible that the output voltage is overshot (Ref, Fig－6) As a rule, VCC voltage is applied before applying STB voltage, or applied at the same time. At the worst, when VCC voltage is applied late from STB, UVLO function must be canceled within 1msec from applying STB voltage.



Fig－5

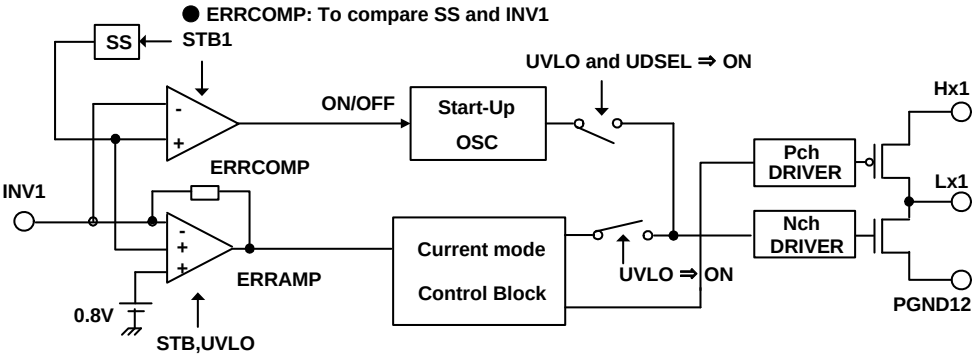
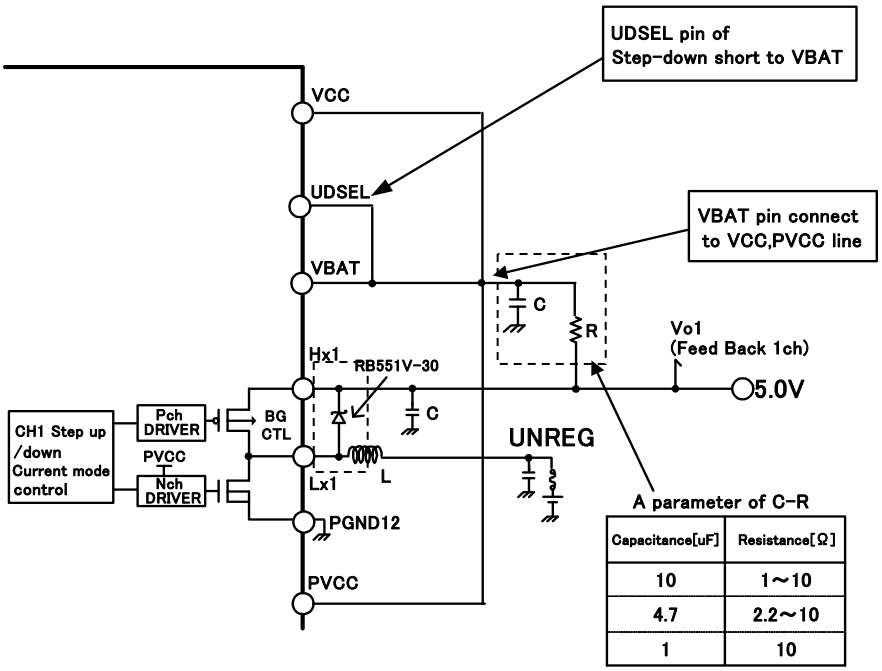


Fig - 6 CH1 Block diagram: Start up circuit



Capacitance[uF]	Resistance[Ω]
10	1～10
4.7	2.2～10
1	10

Fig－7. Recommended application circuit of CH1

2.) Applying condition of VBAT voltage.

The up/down selector UDSEL1,2,4 is constructed by inverter circuit whose power is VBAT, therefore it is possible that operation faults is happen to apply STB voltage without applying VBAT voltage.

As a rule, VBAT voltage is applied before applying STB voltage, or applied at the same time.

At the worst, when VBAT voltage is applied late from STB, VBAT voltage must be applied within 50 μsec from applying STB voltage.

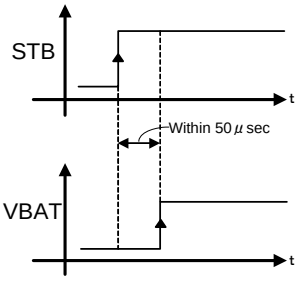


Fig-8

3.) Recommended operating condition of using back-gate control.

The DC/DC converters of CH1,2,4 have back-gate control to cut the current pass of pmos parasitic diode. Using the back-gate control, it is limited by the ability of pmos parasitic diode and pmos switching back-gate position.

When synchronous rectifying FET is OFF in normal operation and STB OFF, the inductor current flows to Hx through pmos parasitic diode (D2) and pmos switching back-gate position (M2). As a result, the voltage of Lx increase to "output voltage + D2 forward voltage Vf + voltage drop of M2". When Hx voltage is set to 5V, this voltage exceed absolute maximum voltage of Lx by increasing input current to about 1.2A. So that it is possible to break built-in FET.

Fig-10 shows recommended operating area of using back-gate control. When the relation between output voltage and input current is out of range, it must be added schottky barrier diode between Lx and Hx. Using schottky barrier diode, back-gate control can be used not to exceed absolute maximum voltage of Lx.

The DC/DC converter of CH1 must be added schottky barrier diode as it is explained in item 1).

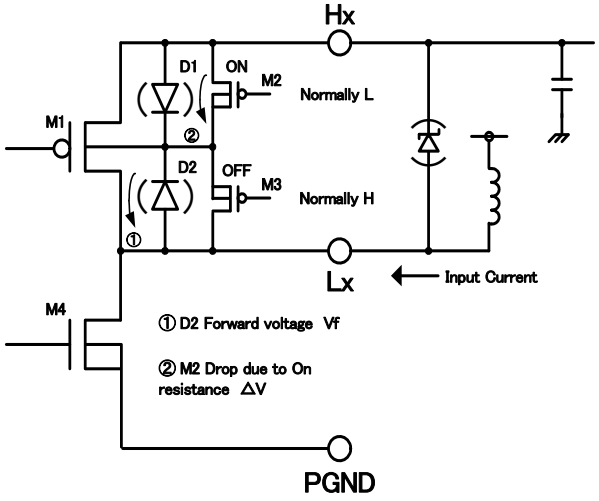


Fig - 9 Back gate control

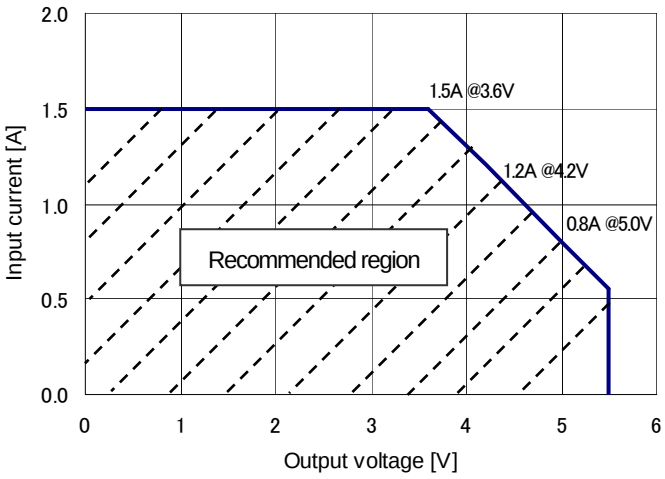


Fig - 10 Recommended operating area of using back-gate

4.) Setting the detection time for the short-circuit-protector (SCP).

The detection time for the SCP is user-adjustable by varying the capacitor connected at SCP (pin32).

The detection time [sec] = Cscp × Vtsc / Iscp

(Cscp : The capacitance、Vtsc : The Threshold voltage SCP、Iscp :The SCP output current)

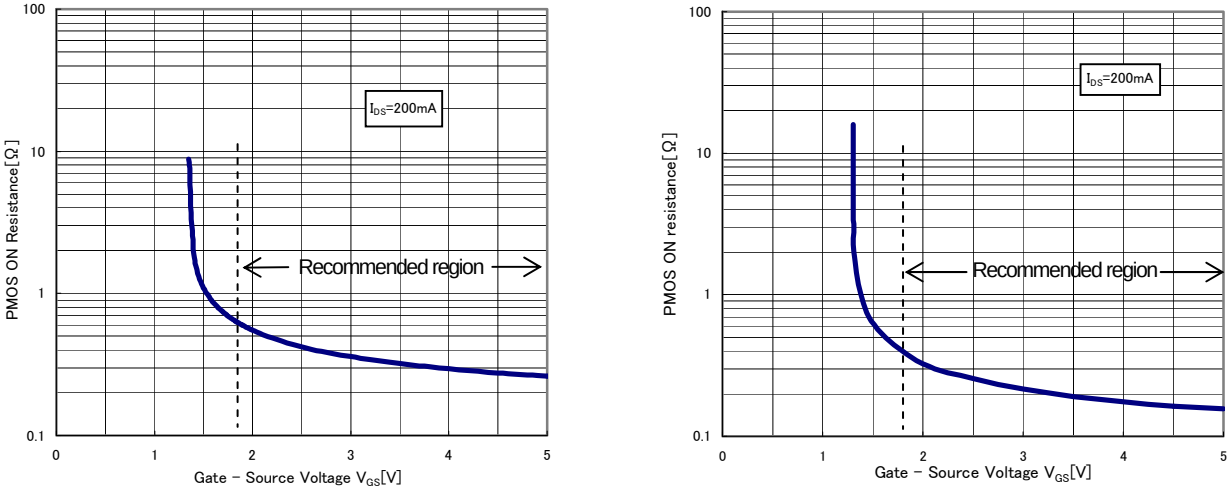
Ex) Cscp = 0.1 μF

The detection time $= 0.1 \times 10^{-6} \times 1 / \{4 \times 10^{-6}\} = 25$msec

As the built-in FET breaks by heat in shorting output, it is recommended that the SCP capacitor is used below 0.47 μF.

5.) Built-in Pch FET(CH1～4,CH67),the drop of current ability in low battery voltage situation

The ON resistance of the built-in Pch FET increase because the FET operates in the saturation region below VGS=1.3V.
Therefore when CH6, 7 step-up converter or step-down channel from a battery is used below 1.8V, the drop is must be considered.
If operating condition below 1.8V should be anticipated, it is recommended that the converter is formed from other channel's output and is not used high side switch.



a. CH4

b. CH7 Highside Switch

Fig - 11 Built-in PMOS ON resistance - V_{GS}

6.) Setting the oscillator frequency.

The oscillator frequency is user-adjustable by varying the resistor connected to RT (29pin). The CH1～4 frequency is set 1.2MHz to connect 62kΩ,and the RT value is inverse proportional relation to the frequency.
The CH5～7 frequency is set half value of the CH1～4 frequency.
Fig.12 shows the relation the RT value and the frequency.

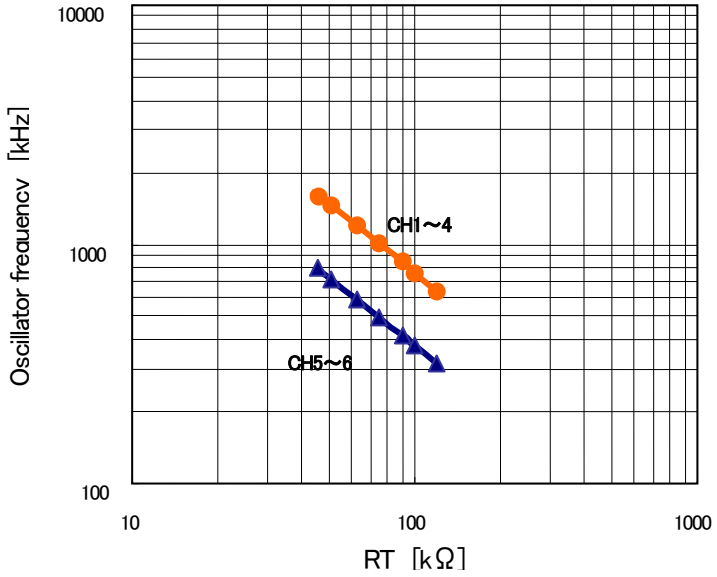


Fig -12 Oscillator frequency – RT resister (EX)

7.) Setting the output voltage.

a. Setting for positive to negative converter (CH5).

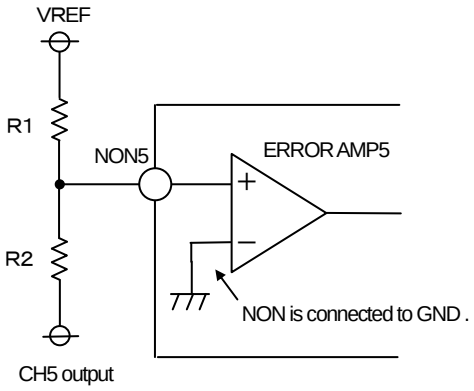


Fig-13 setting for CH5 feed back resistor

The reference of CH5 Error AMP is internally connected to ground. So the high accuracy regulator can be formed up to set up a resistor divider to Fig.13, It is recommended that R1 resistance is over 20kΩ, because current ability of VREF is about 100μA.

$$\text{CH5 output} = -\frac{R2}{R1} \times \text{VREF}\ (=1\text{V}) = -\frac{R2}{R1}$$

(Example)
R1 = 20kΩ, R2 = 160kΩ
CH5 output = -8.0V

b. Setting the feed back of CH7

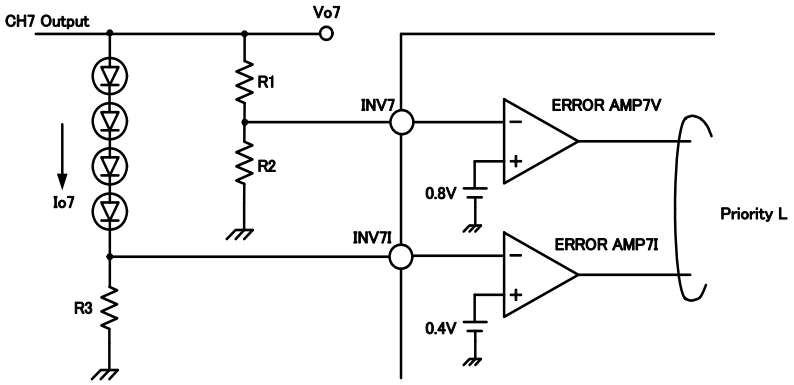


Fig -14 Setting for Voltage and current of CH7.

CH7 has two ERRORAMP whose reference is different. ERROR AMP 7I controls constant current feed back for LED Back light, and ERRORAMP7V controls over voltage feed back and constant voltage feedback.
Each ERRORAMP setting shows below formula.

$$\text{CH7 output current} = \frac{0.4\text{V}}{R3} \quad (\text{Example } R3 = 20\Omega \Rightarrow Io7 = 20\text{mA})$$

$$\text{CH7 output voltage} = \frac{R1+R2}{R2} \times 0.8\text{V} \quad (\text{Example } R1 = 180\text{k}\Omega, R2 = 15\text{k}\Omega \Rightarrow Vo7 = 13\text{V})$$

The lower output of two ERRAMP controls the DC/DC output. There fore, if it is used only one ERRORAMP, other ERRORAMP input must be shorted to GND.

○Operation Notes

1.) Absolute maximum ratings

This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential

Make sure GND is connected at lowest potential. All pins except NON5, must not have voltage below GND. Also, NON5 pin must not have voltage below - 0.3V on start up.

3.) Setting of heat

Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting

Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field

Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance

Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Voltage of STB pin

The threshold voltages of STB pin are 0.3V and 1.5V. STB state is set below 0.3V while action state is set beyond 1.5V.

The region between 0.3V and 1.5V is not recommended and may cause improper operation.

The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01μF.

8.) Thermal shutdown circuit (TSD circuit)

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.)IC Terminal Input

This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed.
For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.15):

○ When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.

Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

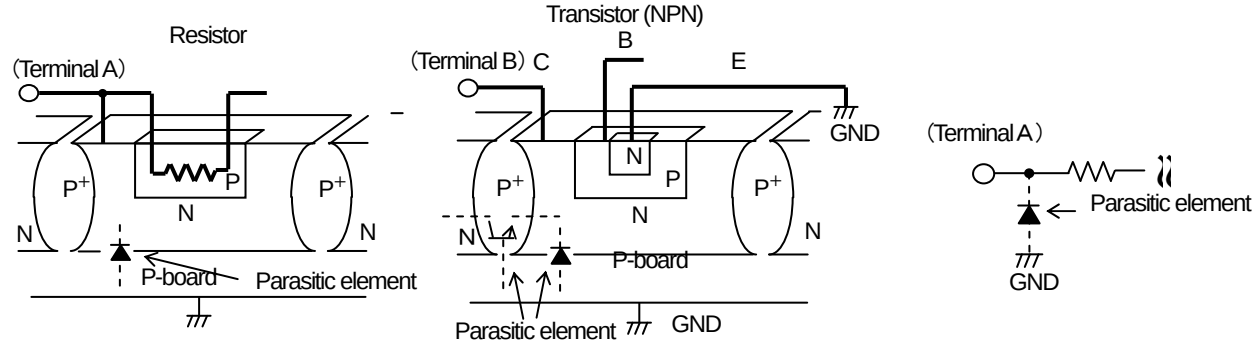


Fig - 15 Simplified structure of a Bipolar IC

Notes

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