



8-Mbit (1024 K × 8) Static RAM

Features

- Very high speed: 45 ns
 - □ Wide voltage range: 2.20 V-3.60 V
- Pin compatible with CY62158DV30
- Ultra low standby power
 - Typical standby current: 2 μA
 - Maximum standby current: 8 μA
- Ultra low active power
 - □ Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

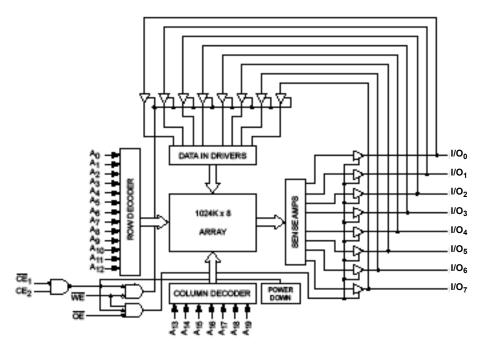
Functional Description

The CY62158EV30 is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life $^{\rm TM}$ (MoBL $^{\rm S}$) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ($\overline{\rm CE}_1$ HIGH or CE $_2$ LOW). The eight input and output pins (I/O $_0$ through I/O $_7$) are placed in a high impedance state when the device is deselected ($\overline{\rm CE}_1$ HIGH or CE $_2$ LOW), the outputs are disabled ($\overline{\rm OE}$ HIGH), or a write operation is in progress ($\overline{\rm CE}_1$ LOW and CE $_2$ HIGH and $\overline{\rm WE}$ LOW).

To write to the device, take Chip Enables ($\overline{\text{CE}}_1$ LOW and CE₂ HIGH) and Write Enable ($\overline{\text{WE}}$) input LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables ($\overline{\text{CE}}_1\text{LOW}$ and CE_2HIGH) and $\overline{\text{OE}}$ LOW while forcing the $\overline{\text{WE}}$ HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See Truth Table on page 10 for a complete description of read and write modes.

Logic Block Diagram



Cypress Semiconductor Corporation
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CY62158EV30 MoBL®



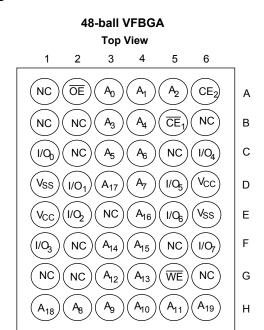
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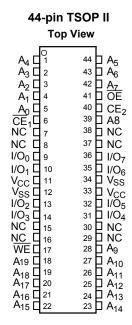
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Pin Configurations [1]





Product Portfolio

							Power Di	ssipation		
Product	V _{CC} Range (V)		Speed	Operating I _{CC} (mA)			Standby L. (uA)			
Product				(ns)	f = 1 MHz f = f _{max}		: max	Standby, I _{SB2} (μA)		
	Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62158EV30LL	2.2	3.0	3.6	45	1.8	3	18	25	2	8

NC pins are not connected on the die.

^{2.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested. Storage Temperature-65 °C to +150 °C Ambient Temperature with Power Applied–55 °C to +125 °C Supply Voltage to Ground Potential–0.3 V to V_{CC(max)} + 0.3 V

DC Input Voltage ^[3, 4] 0.3 V	to V _{CC(max)} + 0.3 V
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage(MIL-STD-883, Method 3015)	> 2001 V
Latch up Current	> 200 mA

Operating Range

Product	Range	Ambient Temperature (T _A)	V cc ^[5]
CY62158EV30LL	Industrial	–40 °C to +85 °C	2.2 V-3.6 V

Electrical Characteristics

Over the Operating Range

D	Dan animation	Tant 0 a	Took Conditions			45 ns			
Parameter	Description	Test Conditions		Min	Typ ^[6]	Max	Unit		
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA		2.0	_	_	V		
		$I_{OH} = -1.0 \text{ mA}, V_{CO}$	₅ ≥ 2.70 V	2.4	_	_	V		
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA		_	_	0.4	V		
		I _{OL} = 2.1 mA, V _{CC} 2	≥ 2.70 V	_	_	0.4	V		
V _{IH}	Input HIGH Voltage	V_{CC} = 2.2 V to 2.7 V	V	1.8	_	V _{CC} + 0.3 V	V		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	V	2.2	_	V _{CC} + 0.3 V	V		
V _{IIL}	Input LOW Voltage	V _{CC} = 2.2 V to 2.7 V		-0.3	_	0.6	V		
		V _{CC} = 2.7 V to 3.6 V		-0.3	_	0.8	V		
I _{IX}	Input Leakage Current	$GND \le V_1 \le V_{CC}$		-1	_	+1	μА		
I _{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, (Output Disabled	-1	_	+1	μА		
I _{CC}	V _{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$	_	18	25	mA		
		f = 1 MHz	I _{OUT} = 0 mA CMOS levels	_	1.8	3	mA		
I _{SB1}	Automatic CE Power down Current — CMOS Inputs	$\begin{array}{l} \overline{\text{CE}}_1 \geq \text{V}_{\text{CC}} - 0.2 \text{ V}, \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V}, \\ \text{f} = \text{f}_{\text{max}} \text{ (Address ar} \\ \text{f} = 0 \text{ (OE and WE)}, \\ \end{array}$	V _{IN} ≤ 0.2 V, nd Data Only),	-	2	8	μА		
I _{SB2} ^[7]	Automatic CE Power down Current — CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$ $f = 0, V_{CC} = 3.60 \text{ V}$		_	2	8	μА		

- Notes
 3. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
 4. V_{IH(max)}= V_{CC} + 0.75 V for pulse duration less than 20 ns.
 5. Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
 7. Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



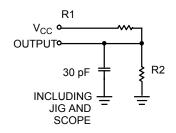
Capacitance

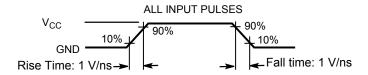
Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	48-ball BGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	76.88	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		8.86	13.52	°C/W

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.

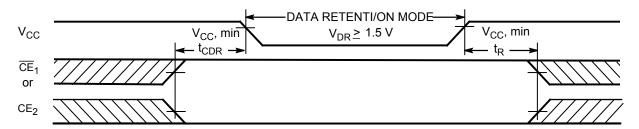


Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V_{DR}	V _{CC} for Data Retention		1.5	_	_	V
I _{CCDR} ^[10]	Data Retention Current	$V_{CC} = 1.5 \text{ V}, \overline{CE}_1 \ge V_{CC} - 0.2 \text{ V}$ or $CE_2 \le 0.2 \text{ V}, V_{IN} \ge V_{CC} - 0.2 \text{ V}$ or $V_{IN} \le 0.2 \text{ V}$	_	2	5	μА
t _{CDR} ^[11]	Chip Deselect to Data Retention Time		0	_	_	ns
t _R ^[12]	Operation Recovery Time		45	_	_	ns

Data Retention Waveform



^{9.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

10. Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

11. Tested initially and after any design or process changes that may affect these parameters.

12. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.



Switching Characteristics

Over the Operating Range

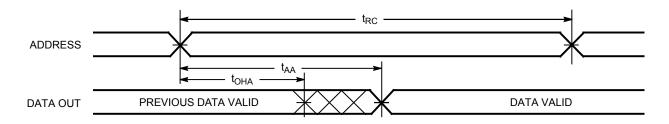
Parameter ^[13]	Description		ns	11!4
Parameter	Description	Min	Max	Unit
Read Cycle			•	
t _{RC}	Read Cycle Time	45	_	ns
t _{AA}	Address to Data Valid	_	45	ns
t _{OHA}	Data Hold from Address Change	10	_	ns
t _{ACE}	CE₁ LOW and CE₂ HIGH to Data Valid	-	45	ns
t _{DOE}	OE LOW to Data Valid	-	22	ns
t _{LZOE}	OE LOW to Low Z ^[14]	5	-	ns
t _{HZOE}	OE HIGH to High Z ^[14, 15]	_	18	ns
t _{LZCE}	$\overline{\text{CE}}_1$ LOW and CE_2 HIGH to Low $Z^{[14]}$	10	_	ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High Z ^[14, 15]	-	18	ns
t _{PU}	CE₁ LOW and CE₂ HIGH to Power Up	0	_	ns
t _{PD}	CE₁ HIGH or CE₂ LOW to Power Down	_	45	ns
Write Cycle ^[1]	6]	,	•	
t _{WC}	Write Cycle Time	45	_	ns
t _{SCE}	CE₁ LOW and CE₂ HIGH to Write End	35	_	ns
t _{AW}	Address Setup to Write End	35	_	ns
t _{HA}	Address Hold from Write End	0	_	ns
t _{SA}	Address Setup to Write Start	0	_	ns
t _{PWE}	WE Pulse Width	35	_	ns
t _{SD}	Data Setup to Write End	25	_	ns
t _{HD}	Data Hold from Write End	0	_	ns
t _{HZWE}	WE LOW to High Z ^[14, 15]	_	18	ns
t _{LZWE}	WE HIGH to Low Z ^[14]	10	_	ns

^{13.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms on page 5.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZCE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

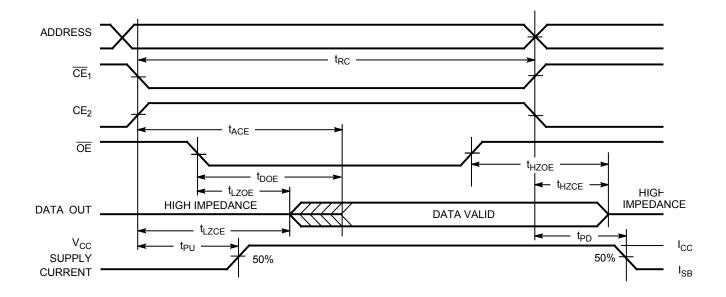


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) $^{[17,\ 18]}$



Read Cycle No. 2 (OE Controlled)[18, 19]



^{17.} Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

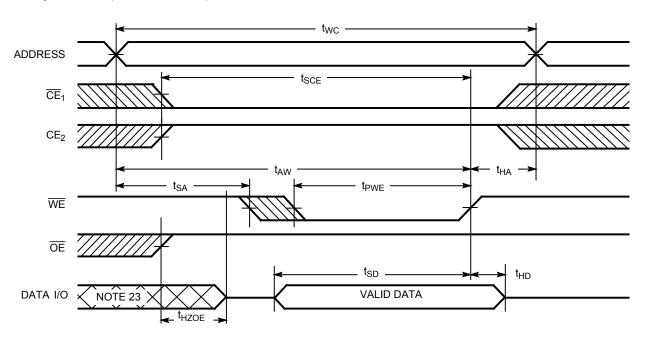
^{18.} WE is HIGH for read cycle.

19. Address valid before or similar to $\overline{\text{CE}}_1$ transition LOW and CE_2 transition HIGH.

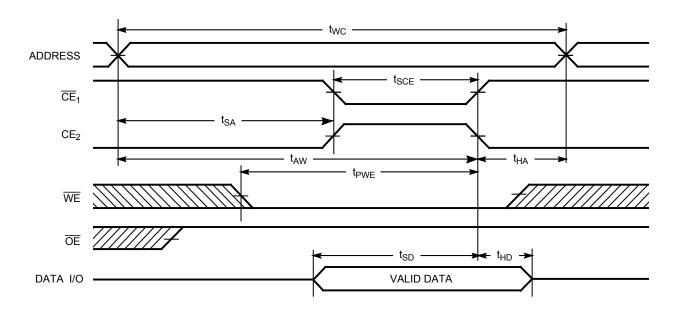


Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)^[20, 21, 22]



Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE_2 Controlled)[20, 21, 22]

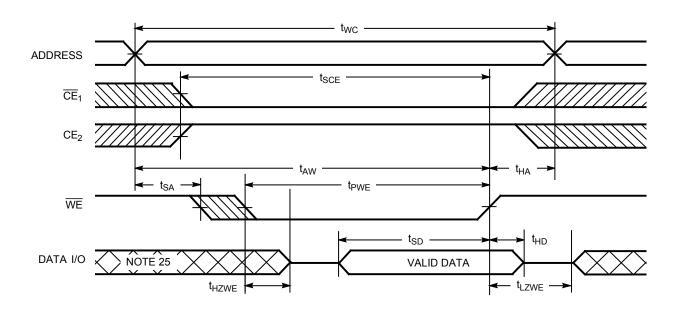


- 20. The internal write time of the memory is defined by the overlap of WE, $\overline{CE}_1 = V_{\parallel}$, and $CE_2 = V_{\parallel}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write. 21. Data I/O is high impedance if $\overline{OE} = V_{\parallel}$. 22. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state. 23. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[24]



Truth Table

Œ ₁	CE ₂	WE	ŌĒ	Inputs/Outputs	Mode	Power
Н	X ^[26]	Х	Х	High Z	Deselect/Power down	Standby (I _{SB})
X ^[26]	L	Х	Х	High Z	Deselect/Power down	Standby (I _{SB})
L	Н	Н	L	Data Out	Read	Active (I _{CC})
L	Н	L	Х	Data In	Write	Active (I _{CC})
L	Н	Н	Н	High Z	Selected, Outputs Disabled	Active (I _{CC})

^{24.} If CE₁ goes HIGH or CE₂ goes LOW simultaneously with WE HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.
26. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

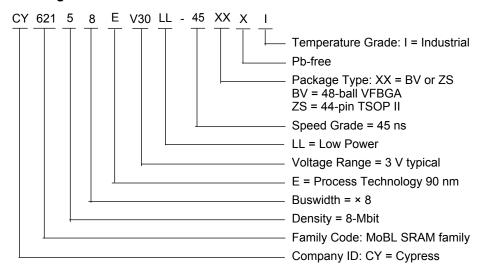


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158EV30LL-45BVXI	51-85150	48-ball Very Fine-Pitch Ball Grid Array (Pb-free)	Industrial
	CY62158EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

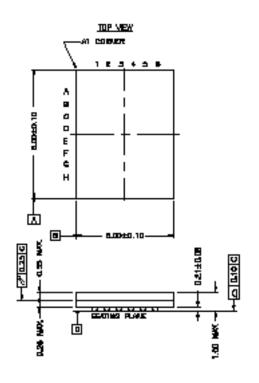
Ordering Code Definitions

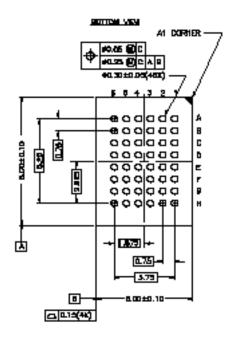




Package Diagrams

Figure 1. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48, 51-85150



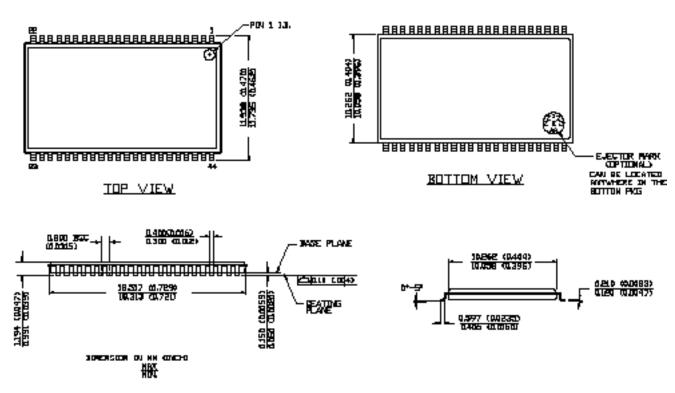


51-85150 *F



Package Diagrams (continued)

Figure 2. 44-pin TSOP Z44-II, 51-85087



51-85087 *C



Acronyms

Acronym	Description			
CE	chip enable			
CMOS	complementary metal oxide semiconductor			
I/O	input/output			
ŌĒ	output enable			
RAM	random access memory			
SRAM	static random access memory			
TTL	transistor-transistor logic			
TSOP	thin small outline package			
VFBGA	very fine-pitch ball grid array			
WE	write enable			

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celcius			
MHz	Mega Hertz			
μΑ	micro Amperes			
μs	micro seconds			
mA	milli Amperes			
mm	milli meter			
ns	nano seconds			
Ω	ohms			
%	percent			
pF	pico Farad			
V	Volts			
W	Watts			



Document History Page

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	270329	See ECN	PCI	New Data Sheet
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed I _{CCDR} from 4 to 4.5 μA
*B	444306	See ECN	NXR	Converted from Preliminary to Final. Removed 35 ns speed bin Removed "L" bin. Removed 44 pin TSOP II package Included 48 pin TSOP I package Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} max value from 28 m to 25 mA for test condition $f = fax = 1/t_{RC}$. Changed the I_{CC} max value from 2.3 mA to 3 mA for test condition $f = 1$ MHz. Changed the I_{SB1} and I_{SB2} max value from 4.5 μ A to 8 μ A and Typ value from 0 μ A to 2 μ A respectively. Updated Thermal Resistance table Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ value for I_{CCDR} . Changed the I_{CCDR} max value from 4.5 μ A to 5 μ A corrected I_{R} in Data Retention Characteristics from 100 I_{R} to I_{R} to 5 changed I_{R} to 10 Changed I_{R} from 3 to 5 changed I_{R} from 22 to 18 changed I_{R} from 22 to 25 changed I_{R} from 6 to 10 Updated the ordering Information and replaced the Package Name column with Package Diagram.
*C	467052	See ECN	NXR	Included 44 pin TSOP II package in Product Offering. Removed TSOP I package; Added reference to CY62157EV30 TSOP I Updated the ordering Information table
*D	1015643	See ECN	VKN	Added footnote #8 related to I _{SB2} and I _{CCDR}
*E	2934396	06/03/10	VKN	Added footnote #21 related to chip enable Updated package diagrams Updated template
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram and Package Diagram. Added Ordering Code Definitions.
*G	3269641	05/30/2011	RAME	Updated Features. Removed the note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com." and i reference in Functional Description. Updated Data Retention Characteristics. Added Acronyms and Units of Measure. Updated in new template.



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