Product Specification Type Number : M T M 9 8 1 4 0 0 [B] B F *1	Prepared by	Checked by	Applied by	Established by
	S.Miyata	M.Fujisawa	H.Shidooka	K.Komichi

Type	Silicon Field Effect Transistors
Application	Switching
Structure	P-Channel MOS Type
Outline	SO8-F1-B
Marking	BA

Absolute Maximum Ratings	VDSS	VGSS	ID	IDp	PD*2	Tch	Tstg
	-40	±20	-7	-28	2	150	-55 to +150
	(V)	(V)	(A)	(A)	(W)	(°C)	(°C)

Electrical characteristics (Ta = 25 °C ±3 °C)

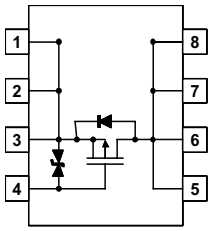
Item	Symbol	Measuring condition	Limit min.	Limit typ.	Limit max.	Unit
Drain-Source Voltage	VDSS	ID = -1 mA, VGS = 0 V	-40			V
Drain-Source Cutoff Current	IDSS	VDS = -40 V, VGS = 0 V			-10	μA
Gate-Source Cutoff Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10.0 V	-1.0		-2.5	V
*3 Drain Resistance (ON)	RDS(ON)	ID = -7 A, VGS = -10 V		19	25	mΩ
*3 Drain Resistance (ON)	RDS(ON)	ID = -3.5A, VGS = -4.5V		28	45	mΩ
*3 Forward Transfer Admittance	|Yfs|	ID = -7 A, VDS = -10 V	10			S
Small-Signal Short-Circuit Imput Capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1MHz		2700		pF
Small-Signal Short-Circuit Output Capacitance	Coss	VDS = -10V, VGS = 0V, f = 1MHz		190		pF
Small-Signal Reverse Transfer Capacitance	Crss	VDS = -10 V, VGS = 0 V, f = 1 MHz		175		pF
*3,4 Turn-on Delay Time	td(on)	VDD = -25 V, VGS = 0 to -10 V, ID = -3.5 A		18		ns
*3,4 Rise Time	tr	VDD = -25 V, VGS = 0 to -10 V, ID = -3.5 A		15		ns
*3,4 Turn-off Delay Time	td(off)	VDD = -25 V, VGS = -10 to 0 V, ID = -3.5 A		230		ns
*3,4 Fall Time	tf	VDD = -25 V, VGS = -10 to 0 V, ID = -3.5 A		70		ns

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Packing
Embossed type (thermo-compressioon sealing)
*2 Measuring on ceramic board at 50×50×1.0mm.
*3 Pulse test
*4 See test circuit

Internally connected circuit

1.Source
2.Source
3.Source
4.Gate
5.Drain
6.Drain
7.Drain
8.Drain



2008.01.31	
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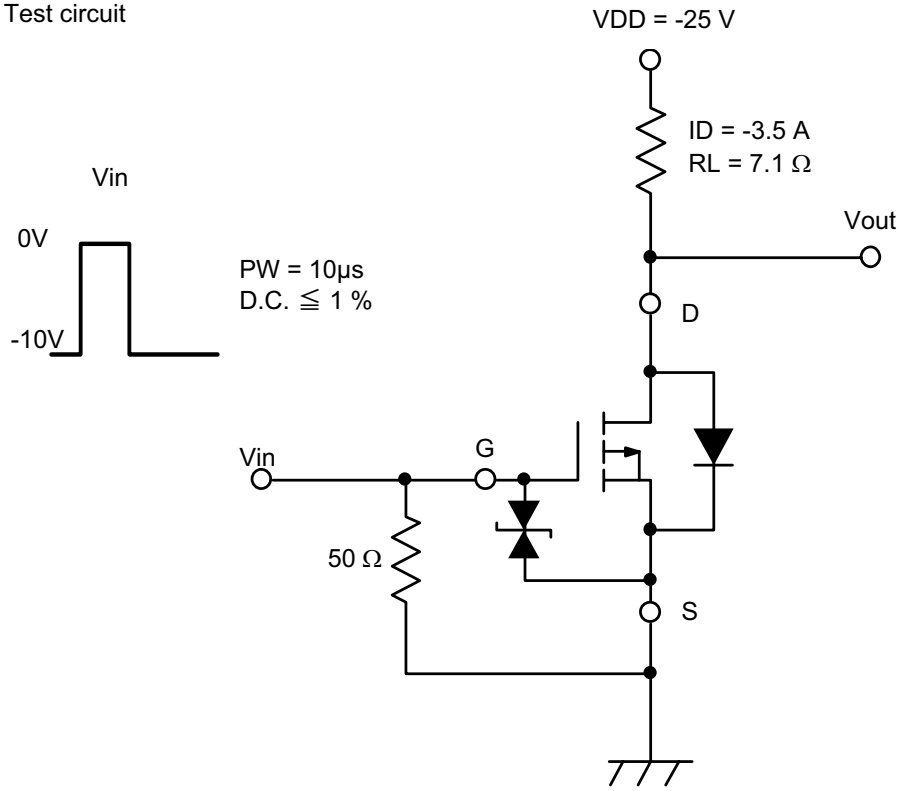
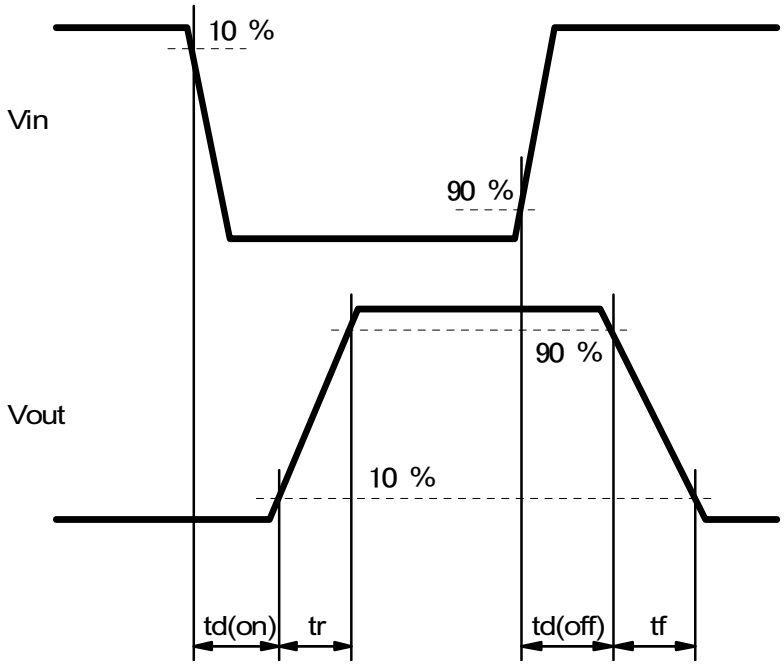
Product Specification
Type Number : M T M 9 8 1 4 0 0 B B F
*1

Test circuit





2008.01.31	
Established	Revised

Panasonic Semiconductor Discrete Devices Co., Ltd.

Regulations No. : SC3S1512	Total Pages	Page
	3	1

PACKAGE STANDARDS

Package Code	SO8-F1-B

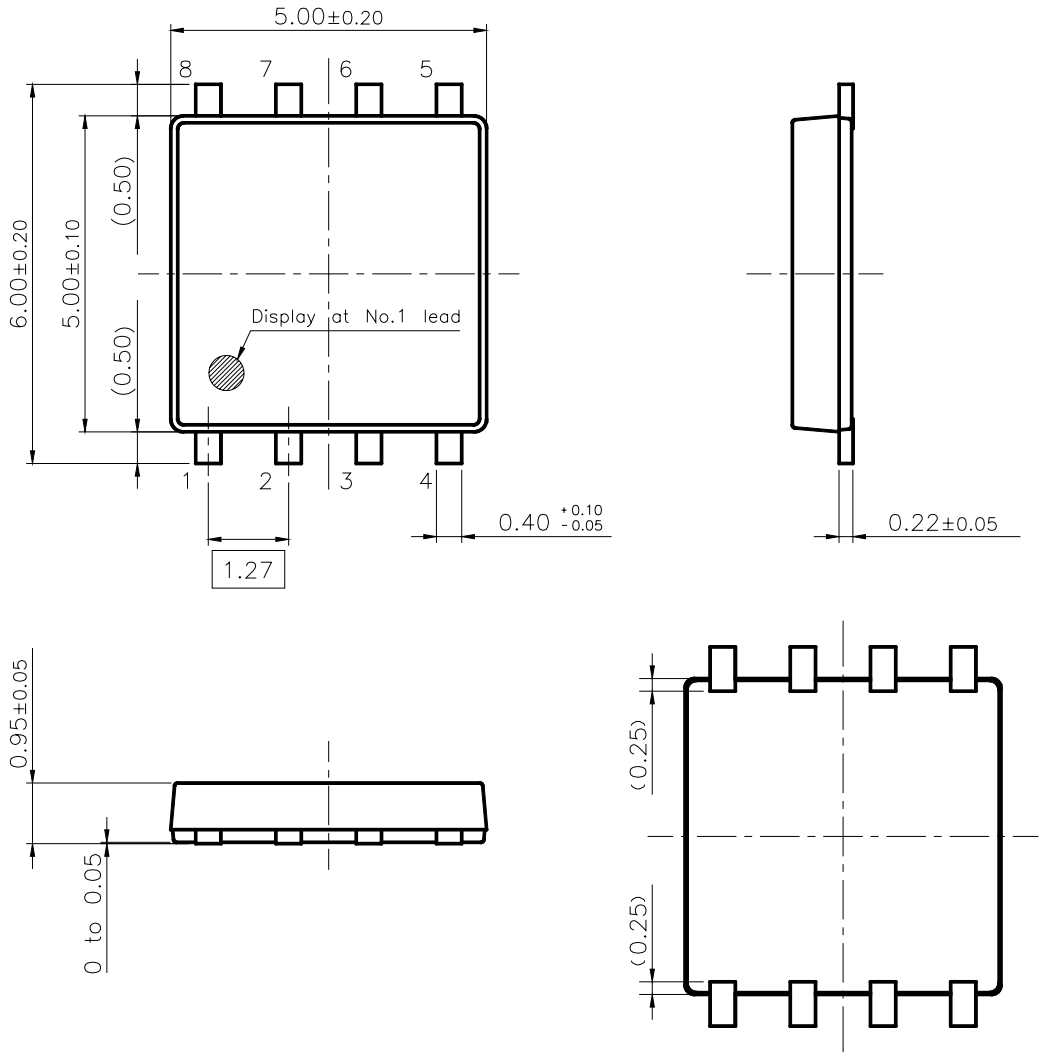
Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Kametaka

Established: 2007-01-18
Revised : 2009-01-23

1. Outline Drawing

Unit:mm

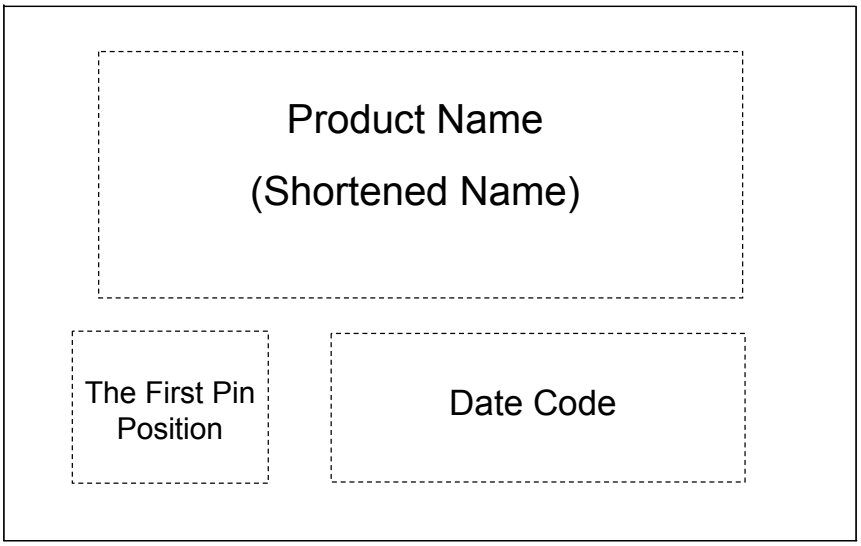


Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	SnBi Plating

Semiconductor Company, Panasonic Corporation

Established: 2007-01-18
Revised : 2009-01-23

3. Mark Drawing



Established: 2007-01-18
Revised : 2009-01-23