LM5071 Evaluation Board

National Semiconductor
Application Note 1430
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April 2006

Introduction

The LM5071 evaluation board is designed to provide a low cost, fully IEEE 802.3af compliant Power over Ethernet (PoE) power supply, capable of operating with both PoE and auxiliary (AUX) power sources. The evaluation board features the LM5071 PoE Powered Device (PD) interface and controller integrated circuit (IC) configured in the versatile flyback topology.

Features of the LM5071 Evaluation Board:

- Single Isolated 3.3V output
- Dual Isolated 5V and 3.3V outputs supported (see Figure 12)
- Maximum output current 3.3A
- Input voltage range (full power):
  - With the installed wide-voltage-range EP13 transformer
    - PoE input voltage range: 38 to 60V
    - AUX input voltage range: 14 to 60V
  - With the optional, efficiency-optimized EP13 transformer
    - PoE input voltage range: 38 to 60V
    - AUX input voltage range: 24 to 60V
- Measured maximum efficiency:
  - With the installed wide-voltage-range EP13 transformer
    - DC to DC converter efficiency: 81% at 3A
    - Overall efficiency (including diode bridge): 78.5% at 3A
  - With the optional, efficiency-optimized EP13 transformer
    - DC to DC converter efficiency: 84% at 3A
    - Overall efficiency (including diode bridge): 81.5% at 3A
- Board Size: 2.75 x 2.00 x 0.66 inches
- Operating frequency: 250 kHz
- Programmed PoE input under-voltage lockout (UVLO) release: 39V Nominal
- Programmed PoE input UVLO hysteresis: 5.9V

This application note focuses on the evaluation board. Please refer to the datasheet for detailed information about the complete functions and features of the LM5071 IC.

A Note about Input Potentials

The LM5071 is designed for PoE applications that are typically -48V systems, in which the notations GND and -48V normally refer to the high and low input potentials, respectively. However, for easy readability, the LM5071 datasheet was written in the positive voltage convention with positive input potentials referenced to the VEE pin of the LM5071. Therefore, when testing the evaluation board with a bench power supply, the negative terminal of the power supply is equivalent to the PoE system's -48V potential, and the positive terminal is equivalent to the PoE system ground. To prevent confusion between the datasheet and this application note, the same positive voltage convention is used herein.

Schematic of the Evaluation Board

Figure 1 shows the schematic of the LM5071 evaluation board. See the Appendix for the Bill of Materials (BOM).

Schematic of the Evaluation Board (Continued)

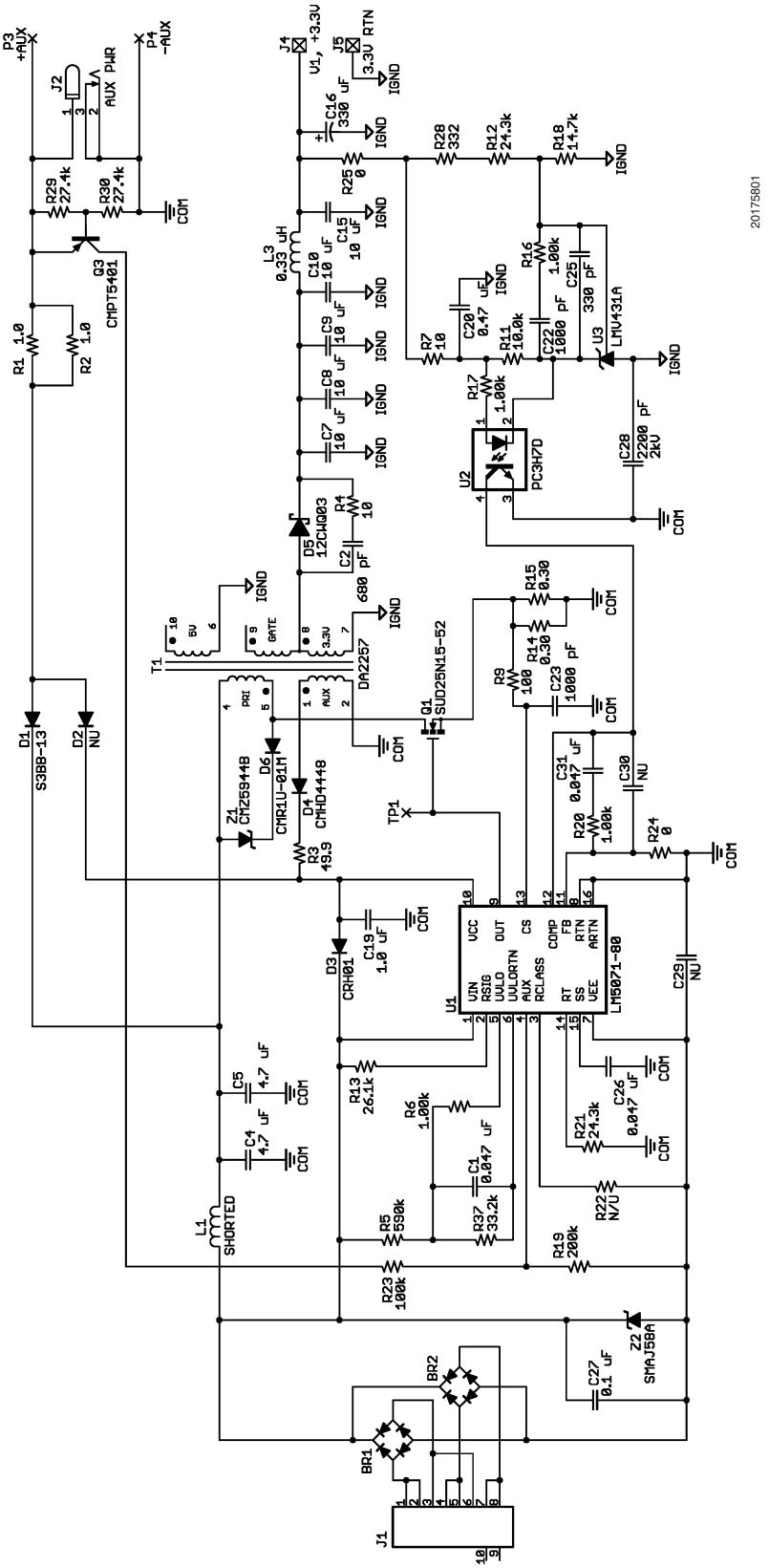

FIGURE 1. Schematic of the LM5071 Evaluation Board

Connection and Proper Test Methods

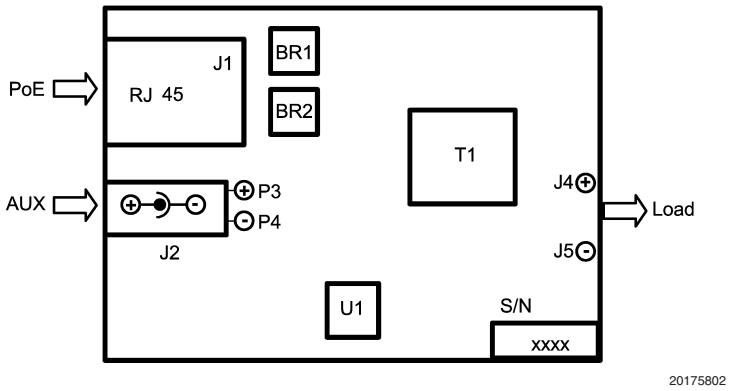

FIGURE 2. LM5071 Evaluation Board Connections

Figure 2 shows the connections for the LM5071 evaluation board.

The LM5071 evaluation board has three ports for connections. The RJ45 receptacle connector is for PoE input, the PJ102A power jack for AUX input (also accessible with posts P3 and P4 located right behind the jack), and the 3.3V output port accessible with posts J4 and J5.

For the PoE input, two diode bridges BR1 and BR2 steer the current to the positive and negative supply pins of the LM5071. For the AUX input, the high potential of the AUX input voltage should feed into the center pin of the PJ102A jack.

For the output connection, the load can be either a passive resistor or active electronic load. Attention should be paid to the output polarity when connecting an electronic load. Use of additional filter capacitors greater than 20 µF total across the output port is not recommended unless the feedback loop compensation is adjusted accordingly.

Sufficiently large wire size not smaller than AWG #18 is required when connecting the source supply and load. Also, monitor the current into and out of the unit under test. Monitor the voltages directly at the board terminals, as resistive voltage drops along the connecting wires may decrease measurement accuracy. Never rely on the lab supply voltmeter if accurate efficiency measurements are needed.

When measuring the dc-dc converter efficiency, the converter input voltage should be measured across C4 or C5, as this is the input of the converter stage. When measuring the evaluation board overall efficiency, both input and output voltage should be read from the terminals of the evaluation board.

Source Power

To fully test the LM5071 evaluation board, a DC power supply capable of at least 60V and 1A is required for the PoE input. For the AUX source power, use a DC power supply capable of 1.5A. Use the output over-voltage and over-current limit features of the bench power supplies to protect the board against damage by errant connections.

Loading / Current Limiting Behavior

A resistive load is optimal, but an appropriate electronic load specified for operation down to 2.0V is acceptable. The maximum load current is 3.3A. Exceeding this current at low input voltage may cause oscillatory behavior as the part will go into current limit mode. Current limit mode is triggered whenever the current through the PoE connector exceeds 390mA (nominal). If current limit is triggered, the switching regulator is automatically disabled by discharging the soft-start capacitor C26 through the SS pin. The module is then allowed to restart, but the unit will operate in an automatic re-try (hiccup) mode as long as the over-current condition remains.

Power Up

It is suggested to apply PoE power first. During the first power up, the load should be kept reasonably low. Verify the supply current during signature and classification modes before applying full power. During signature mode, the module should have the I-V characteristics of a 25 kΩ resistor in series with two diodes. During classification mode, current draw should be about 600 µA at 15V as the RCLASS pin is left open, defaulting to class 0. If the proper response is not observed during both signature and classification modes, check the connections closely. If no current is flowing it is likely that the set of conductors feeding the PoE power have been incorrectly installed.

Once the proper setup has been established, full power can be applied. A voltmeter across the output terminals J4 (+3.3V) and J5 (3.3V RTN), will allow direct measurement of the 3.3V output line. Because the output voltage is isolated, it should not be measured by a meter referenced to the bench power supply ground. If the 3.3V output voltage is not observed within a few seconds, turn the power supply off and review connections.

A final check of efficiency is the best way to confirm that the unit is operating properly. Efficiency significantly lower than 80% at full load indicates a problem.

After the PoE operation is verified, apply the AUX power. It is recommended that the application of the AUX power follow the same precautions as that of the PoE. If no output voltage

Power Up (Continued)

is observed, it is likely that the AUX power feed polarity is reversed. After successful operation is observed, full power testing can begin.

PD Interface Operating Modes

When connecting into the PoE system, the evaluation board's Powered Device interface will go through the following operating modes in sequence: PD signature detection, power level classification (optional), and application of full power. Refer to the LM5071 datasheet and IEEE 802.3af for detailed information about these operating modes.

Signature Detection

On the evaluation board, the PD signature is implemented with R13. The use of a 26.1 kΩ resistor for R13 yields an equivalent signature impedance of 25.1kΩ, which is in the valid PD signature range of 23.75 kΩ to 26.25 kΩ per IEEE 803.2af.

It should be noted that when the AUX power is present, it will not allow the PoE's power sourcing equipment (PSE) to identify the PD as a valid device, because the AUX voltage will cause the front-end current steering diode bridges to be reverse biased during detection mode. This prevents the PSE from applying power, and the evaluation board only draws current from the AUX source.

Classification

PD classification is implemented with R22. The evaluation board is set to the default Class 0 by leaving the RCLASS pin open (R22 position not populated). To activate a specific class instead of Class 0, install R22 according to the following table.

Class	P_{MIN}	P_{MAX}	I_{CLASS}(MIN)	I_{CLASS}(MAX)	R22 Selection
0	0.44W	12.95W	0mA	4mA	Open
1	0.44W	3.84W	9mA	12mA	150Ω
2	3.84W	6.49W	17mA	20mA	82.5Ω
3	6.49W	12.95W	26mA	30mA	53.6Ω
4	Reserved	Reserved	36mA	44mA	38.3Ω

Input UVLO and UVLO Hysteresis

The input UVLO threshold and UVLO hysteresis can be independently programmed by selecting R5 and R37. The UVLO release threshold level is mainly determined by the ratio of R37 and R5, as governed by the following equation,

$$UVLO\_release = \left(1 + \frac{R5}{R37}\right) x\ 2V + 2 x\ V_F$$

where V_F stands for the forward voltage drop of a single diode of the input current steering bridge. The UVLO hysteresis is determined by the following equation:

$$UVLO\_hysteresis = 10\mu A x\ R5$$

The evaluation board uses 33.2 kΩ for R37 and 590 kΩ for R5, setting the UVLO release threshold at about 39V and a UVLO hysteresis of 5.9V. The use of C1 helps filter out input voltage transients, thus preventing faulty activation or release of the input UVLO.

AUX Power Option

For AUX power option, the circuitry tied to the AUX pin forces the UVLO to release in order to allow operation at an AUX voltage as low as 10.5V (9.5V seen by the VIN pin of the LM5071 IC). Note that the AUX pin references VEE while the auxiliary supply references RTN, which will be different by one diode drop until the internal hot swap MOSFET is engaged.

It is required that D2 be installed when the AUX input is lower than 14V. This will bypass the internal startup regulator and directly supply the bias voltage to the LM5071 IC for startup. Use CMHD4448 or equivalent for D2. When the switching circuit establishes stable operation, Vcc will be provided by a transformer winding with a level up to 16V. This voltage may damage the internal startup regulator by back feeding to the lower potential VIN line. To solve this problem, D3 is introduced to protect the IC by bypassing the back feed path and clamping the VCC pin. On the evaluation board, D3 has already been installed. However, for applications where the input voltage is always higher than 18V, D3 can be removed to save the BOM cost.

Small value resistors in series with the auxiliary input limit the inrush current from the auxiliary supply. They should be made as large as is practical given the design constraints.

Special attention should be paid to the selection of D1, D2, D3, D4 and Q3. They all should be low leakage current devices. Otherwise the leakage current during PoE operation will create a false signal at the AUX pin of the IC as if the circuit is powered from the AUX source. Most diode and transistor datasheets provide information on the maximum leakage current at both 25˚C and 125˚C, although the data for the intermediate temperatures are not often given. It can be approximated that the leakage current doubles for every 10˚C temperature rise.

The junction temperature of these devices should not reach 125˚C because the only dissipation inside these devices is due to the leakage current. Therefore it is not necessary to select the devices based on the maximum leakage current specified at 125˚C. The evaluation board design considered 55˚C as the maximum junction temperature of these devices, which is true for most PoE applications. At 55˚C, the selection of S3BB-13 for D1, CRH01 for D3, CMHD4448 for D4 and CMPT5401 for Q3, will not cause a false signal at AUX pin.

When designing a PD for the higher temperature requirement of some particular application, the values of R19, R23, R29 and R30 should be chosen such that the voltage created across R19 does not exceed 0.5V during PoE operation.

The AUX pin is not reverse protected, and an additional reverse blocking diode will be required for complete auxiliary input reverse protection.

Flyback Converter Topology

The dc-dc converter stage of the LM5071 evaluation board features the flyback topology, which employs the minimum number of power components to implement an isolated power supply at the lowest possible cost.

A unique characteristic of the flyback topology is its power transformer. Unlike an ordinary power transformer that simultaneously transfers the power from the primary to the secondary, the flyback transformer first stores the energy in the transformer core every switching cycle when the main switch is turned on; and then releases the stored energy to the load during the rest of the cycle. When the stored energy is not completely released before the main switch is turned on again, it is said that the flyback converter operates in continuous conduction mode (CCM). Otherwise, it is in discontinuous conduction mode (DCM).

Major advantages of CCM over DCM include (i) lower ripple current and ripple voltage, requiring smaller input and output filter capacitors; and (ii) lower rms current, thus reducing the conduction losses. To keep the flyback converter in CCM at light load, the transformer's primary inductance should be designed as large as is practical.

Major drawbacks of CCM, as compared to DCM, are (i) the presence of the Right-Half-Plane Zero which may limit the achievable bandwidth of the feedback loop; and (ii) the need for slope compensation to stabilize the feedback loop at duty cycles greater than 50%. The flyback topology can have multiple secondary windings for multi output channels. One or more of these secondary channels are normally utilized internally by the converter itself to provide necessary bias voltages for the controller and other devices.

The evaluation board uses a small power transformer having a primary inductance of 32 µH. This is a compromise made to allow the small transformer to operate over a wide input voltage range from 14V to 60V. However, with this transformer, the flyback converter runs in CCM at full load for input voltages lower than 42V, and in DCM for higher input voltages or light loads. The LM5071's built-in slope compensation helps stabilize the feedback loop when the duty cycle exceeds 50% in the low input voltage range.

A transformer winding is used to provide the bias voltage (V_{CC}) to the LM5071 IC. Although the LM5071 controller includes an internal startup regulator which can support the bias requirement indefinitely, the transformer winding produces a V_{CC} about 2V higher than the startup regulator output, thus shutting off the startup regulator and reducing the power dissipation inside the IC.

The Factors Limiting the Minimum Operating Input Voltage

The LM5071 is capable of operating with an AUX power source of as low as 10.5V (after the AUX input OR-ing-diode drop, the VIN pin sees 9.5V). However, the minimum operating AUX input voltage of the evaluation board at full load is mainly determined by two factors; the flyback power transformer design and the values of the current sense resistors R14 and R15.

The installed EP13 type power transformer (DA2257-AL or DCT13EP-U12S005) is a low cost solution to operate with a wide AUX input voltage range. However, the small cross-sectional area of the EP13 magnetic core limits the maximum flux it can handle. To use such a small transformer from 14V to 60V under the full load condition, a compromise between the minimum operating input voltage and maximum inductance of the transformer must be made such that the peak current at 14V input will not cause the peak flux density to exceed 3000 Gauss. A drawback of this low cost solution is that the rms currents flowing through the dc-dc converter stage are increased and the efficiency of the dc-dc converter is reduced by about 3%.

Replacing the originally installed transformer with the optional power transformer DA2383-AL from Coilcraft improves the efficiency, but the minimum operating input voltage will be limited to 24V. To use this optional transformer for lower input voltage, the load level should be scaled down accordingly, as shown in *Figure 3*.

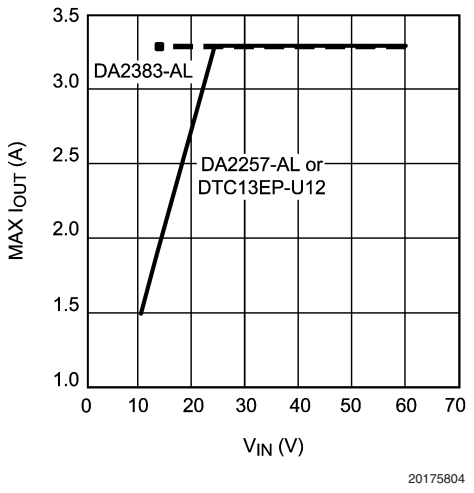

FIGURE 3. Maximum Load Current vs. Minimum Input Voltage as Limited by Different EP13 Type Power Transformers

To optimize efficiency over the maximum input voltage range of 9.5V to 60V, a larger magnetic core like the EFD20 should be used. The EFD20 core has adequate cross-sectional area to handle the peak currents at 9.5V input.

The effects of the current sense resistors R14 and R15 also limit the minimum AUX input operating voltage. The LM5071's internal slope compensation stabilizes the feedback loop of the dc-dc converter when the duty cycle exceeds 50% for input voltages lower than 22V. However, the relative magnitude of the slope compensation is inversely proportional to the values of R14 and R15. The maximum values of R14 and R15 are governed by the following relation:

$$\frac{R14 \times R15}{R14 + R15} < \frac{1.8 \times D_{max}}{2 \times D_{max} - 1} \times \frac{f_{SW} \times L_m}{k_t \times (V_O + V_F)}$$

where

D_{max} is the duty cycle at the minimum AUX input voltage

f_{sw} the switching frequency, in kHz

L_m the flyback transformer primary inductance, in µH

k_t the transformer's primary to secondary turns ratio

V_o the output voltage, in volts

V_F the forward drop of the output diode D5, in volts

Selecting 0.30Ω for both R14 and R15 will allow a minimum operating voltage of 14V. For lower AUX input voltage, Dmax is greater and hence R14 and R15 must be reduced accordingly. However, the smaller resistors increase the slope compensation. Increasing the slope compensating makes the feedback loop appear more like voltage mode than current mode which requires the use of a low ESR capacitor for C16 rather than the low cost capacitor initially installed on the evaluation board.

In summary, the 14V minimum operating AUX input voltage of the evaluation board is limited by the low cost solution. In order to use the evaluation board with a lower AUX source, the power transformer T1, the output capacitor C16, R14 and R15 should be all modified in addition to the installation of D2.

Performance Characteristics

POWER UP SEQUENCE

The high level of integration designed into the LM5071 allows all power sequencing communications to occur within the IC. Very little system management design is required by the user. The power up sequence is as follows. Note that the RTN pin (IC pin 8) is isolated from the +3.3V RTN output pin of the board:

1. Before power up, all nodes in the non-isolated section of the power supply remain at high potential until UVLO is released and the drain of the internal hot swap MOSFET is pulled down to VEE (IC pin 7).
2. Once the RTN pin of the IC drops below 1.5V (referenced to VEE), the V_{CC} regulator is released and allowed to start. This signals the assertion of the internal "Power Good" signal. The V_{CC} regulator ramps at a rate equal to its current limit, typically 20 mA, divided by the V_{CC} load capacitance, C19.
3. Once the V_{CC} regulator is within minimum regulation, about 7.6V referenced to RTN, the soft-start pin is released. The soft-start pin will rise at a rate equal to the soft-start current source, typically 10µA, divided by the soft-start pin capacitance, C26.
4. As the switching regulator achieves regulation, the auxiliary winding will raise the V_{CC} voltage to about 10V, thus shutting down the internal regulator and increasing efficiency.

Figure 4 shows the voltages at RTN, VCC, and SS (Soft-start) IC pins, all referenced to the VEE pin, during a normal startup sequence. A more detailed scope plot of the V_{CC} regulator starting up is given in *Figure 5*. The auxiliary winding starts to supply a higher voltage as the switching regulator output voltage rises.

Performance Characteristics

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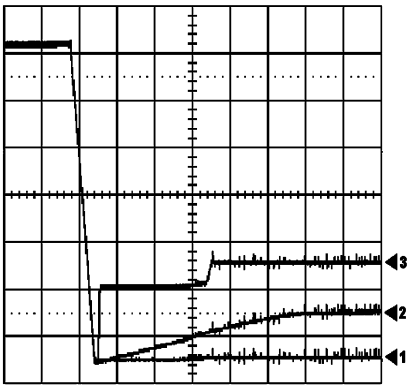

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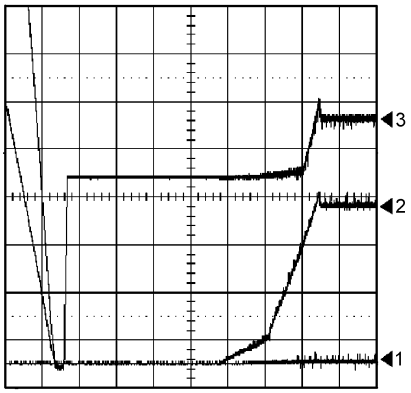
Horizontal Resolution: 5 ms/Div.

Trace 1: RTN pin, elevated until UVLO release. 5V/Div.

Trace 2: SS pin, starts when VCC achieves minimum regulation. 5V/Div.

Trace 3: VCC, starts when RTN<1.5V, elevated by auxiliary winding. 5V/Div.

FIGURE 4. Normal Startup Sequence



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Horizontal Resolution: 2 ms/Div.

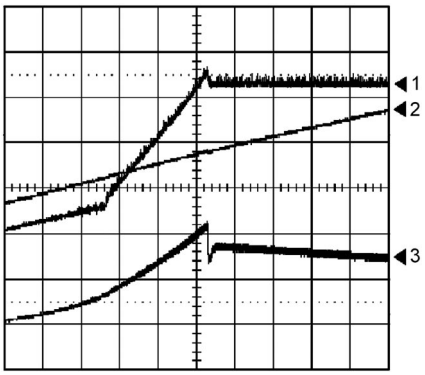
Trace 1: RTN pin, elevated until UVLO release. 5V/Div.

Trace 2: Vout, cross-regulate VCC after output regulation is established. 1V/Div.

Trace 3: VCC, starts when RTN<1.5V, elevated by auxiliary winding. 2V/Div.

FIGURE 5. VCC Startup Detail

Figure 6 shows a normal 3.3V line startup, along with the softstart pin for reference.



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Horizontal Resolution: 1 ms/Div.

Trace 1: +3.3V output voltage, 1V/Div.

Trace 2: Softstart pin, 1V/Div.

Trace 3: Input current (AC coupled), 200 mA/Div.

FIGURE 6. Regulator Output (+3.3V) Startup Detail

OUTPUT DEAD SHORT FAULT RESPONSE

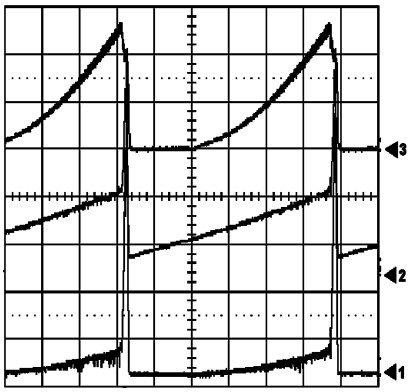
The evaluation board survives the output dead short condition by running into a re-try mode (hiccups). Applying a dead short to the +3.3V line causes a number of protection mechanisms to occur sequentially. They are:

1. Feedback raises duty cycle in an attempt to maintain the output voltage. This initiates cycle-by-cycle over-current limiting which turns off the main switch when the current sense (CS) pin exceeds the current limit threshold.
2. The average current in the internal PD interface MOSFET rises until it is current limited around 390 mA. Some overshoot in the current will be observed, as it takes time for the current limit amplifier to react and change the operating mode of the MOSFET.
3. Because linear current limit is accomplished by driving the MOSFET into the saturation region, the drain voltage (RTN pin) rises. When it reaches 2.5V with respect to VEE, the internal power good signal is de-asserted.
4. The de-assertion of power good causes the discharge of the soft-start capacitor, which disables all switching action in the dc-dc converter.
5. Once the switching stops, the current in the internal MOSFET will decrease and the drain voltage will fall back below 1.5V with respect to VEE. When power good is re-asserted, the dc-dc converter will automatically restart with a new soft-start sequence.

The re-try mode due to a shorted output condition can be observed in Figure 7. The soft-start pin is observed to rise quickly as the LM5071 reacts to the fault. This is because it references RTN, while all scope measurements reference VEE.

Performance Characteristics

(Continued)



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Horizontal Resolution: 2 ms/Div.

Trace 1: RTN pin of the LM5071 IC, 1V/Div.

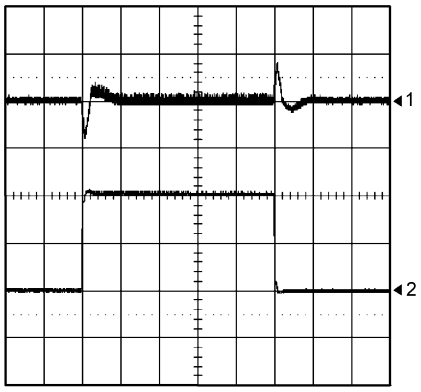
Trace 2: Softstart pin, 2V/Div.

Trace 3: Test board input current, 200 mA/Div.

FIGURE 7. Shorted Output Fault Condition / Automatic Re-try

STEP RESPONSE

Figure 8 shows the step load response at V_{IN} = 48V.



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Horizontal Resolution: 200 µs/Div.

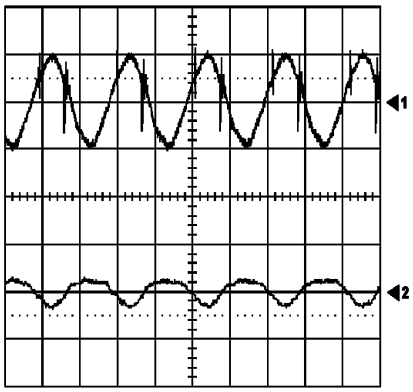
Trace 1: Output voltage (AC coupled), 200 mV/Div.

Trace 2: Output current (DC coupled), 0.5A/Div.

FIGURE 8. Regulator Response to Step Load

RIPPLE VOLTAGE/CURRENT

Figure 9 shows the output ripple voltage and input ripple current for 48V input voltage and 3.3A output.



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Horizontal Resolution: 0.2 ms/Div.

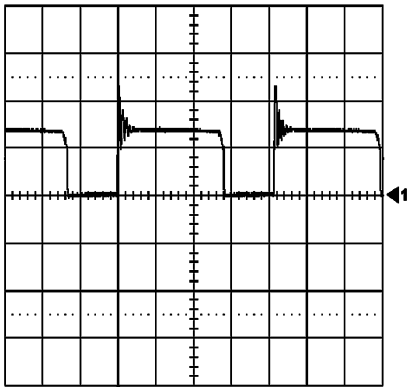
Trace 1: Output voltage (AC coupled), 20 mV/Div.

Trace 2: Input current (AC coupled), 50 mA/Div.

FIGURE 9. Ripple Currents and Voltages

FLYBACK TRANSFORMER WAVEFORMS

Figure 10 and *Figure 11* show the typical drain to source voltage of the main switch Q1 and the reverse voltage of rectifier diode D5, respectively, at 48V input voltage and 3.3A output.



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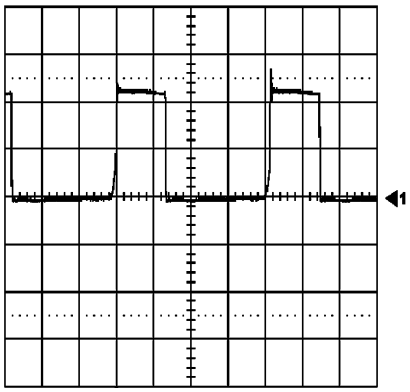
Horizontal Resolution: 1 µs/Div.

Trace 1: Drain to source voltge of main switch Q1, 50V/Div.

FIGURE 10. Flyback Main Switch Drain Voltage Waveform

Performance Characteristics

(Continued)



Horizontal Resolution: 1 µs/Div.

Trace 1: Reverse voltage across output rectifier diode D5, 5V/Div.

FIGURE 11. Output Rectifier Reverse Voltage Waveform

Reconfiguration Of The Evaluation Board For 3.3V And 5V Dual Outputs

The standard evaluation circuit can be easily reconfigured into a 2A 3.3V and 0.6A 5.5V, dual output power supply. The reconfiguration needs to populate the components for the 5.5V output rail, as shown in *Figure 12*. These components are listed in the additional BOM list in the Appendix.

Reconfiguration Of The Evaluation Board for Non-Isolated Output Applications

For applications where output isolation is not required, the non-isolated version of the evaluation board can be used to reduce the BOM cost. Reconfiguration of the circuit board to the non-isolated version can be accomplished in the following four steps (refer to Figure 1 if not indicated otherwise):

1. Delete the unused parts from the circuit board as well as the BOM: C20, C22, C25, C28, R7, R11, R16, R17, R24, U2 and U3.
2. Connect test points P5 and P6 with a bus wire of AWG 26 (refer to Figure 13).
3. Short C28 pads by installing a 0Ω resistor of R2010 size, or by soldering a piece of AWG 26 bus wire.
4. Change C30 to 3.3 nF, C31 to 1.0 nF and R20 to 10 kΩ.

Figure 13 shows the schematic of non-isolated circuit for a single 3.3V output. Similar changes also apply to the dual output version.

Enhancing Input Filter Performance

The evaluation board employs two 4.7 µF ceramic capacitors (C4 and C5) as the input filter of the DC-DC converter stage. The configuration is adequate to meet the IEEE 802.3af specifications, though it may be required to further enhance the input filter performance for EMI / EMC considerations. To do so, an inductor of 10 µH such as the Coilcraft DO3308P-103MLD can be added. The inductor should be installed in the L1 location on the top side of the PC Board, a location originally shorted with a bus wire. Also, install a 22 µF aluminum electrolytic capacitor such as the Panasonic EEV-HA2A220P in the C6 location right beside L1 on the top side of the PC Board in order to protect the LM5072 IC by absorbing the inductor energy during shutdown. A jumper wire of AWG #28 or thicker with insulation sleeve should be soldered to connect the junction of L1 / BR1 with the junction of C6 / R27. By doing so, the 22 µF capacitor is placed in front of L1 and directly across the VIN and RTN pins of the LM5072. As a cost consideration, ceramic capacitor C5 (4.7 µF) can be deleted from the PCB, and L1 and C4 will be adequate to attenuate the input ripple current below 2 mA peak to peak .

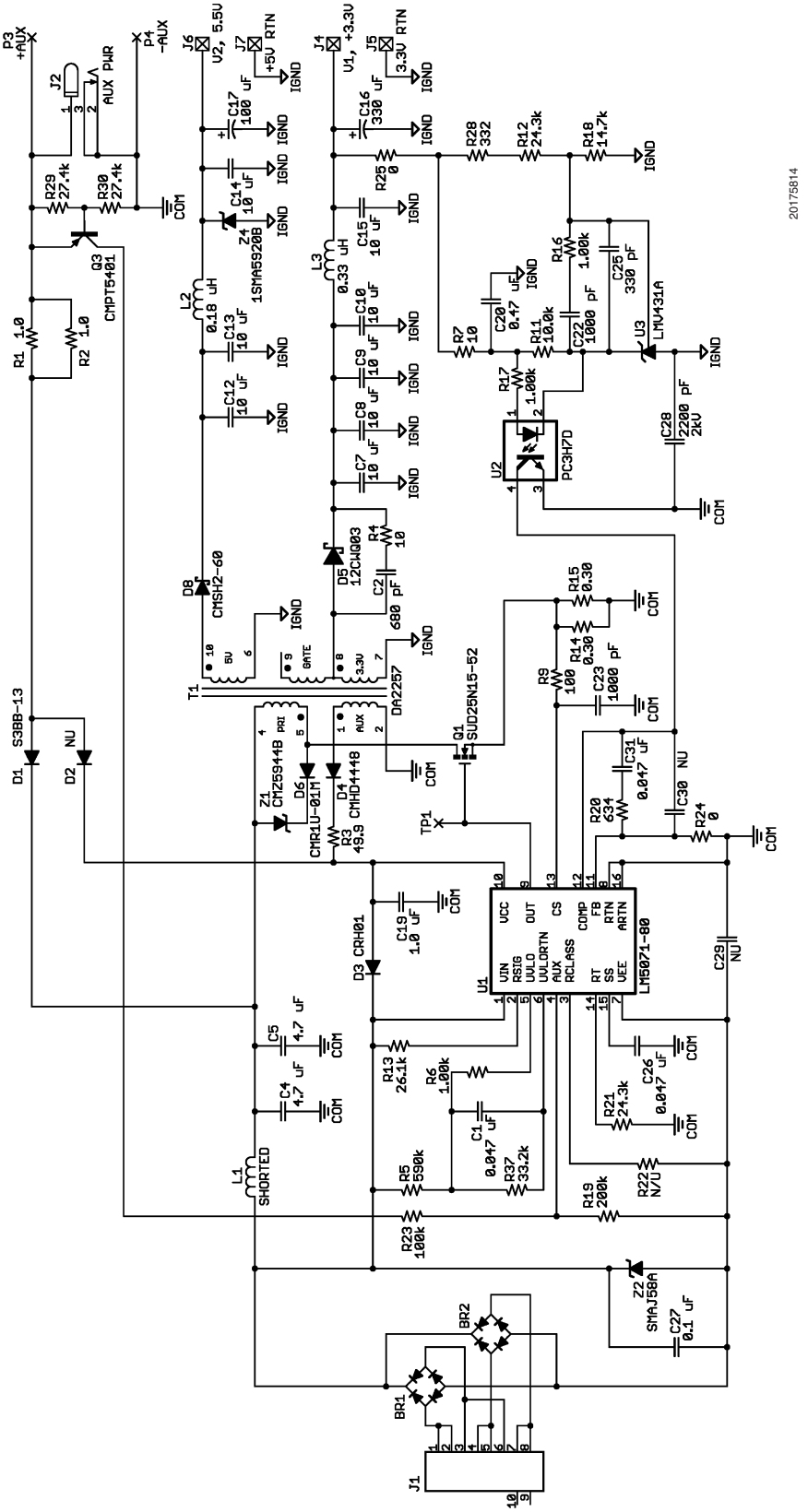


FIGURE 12. The Schematic for Dual Outputs

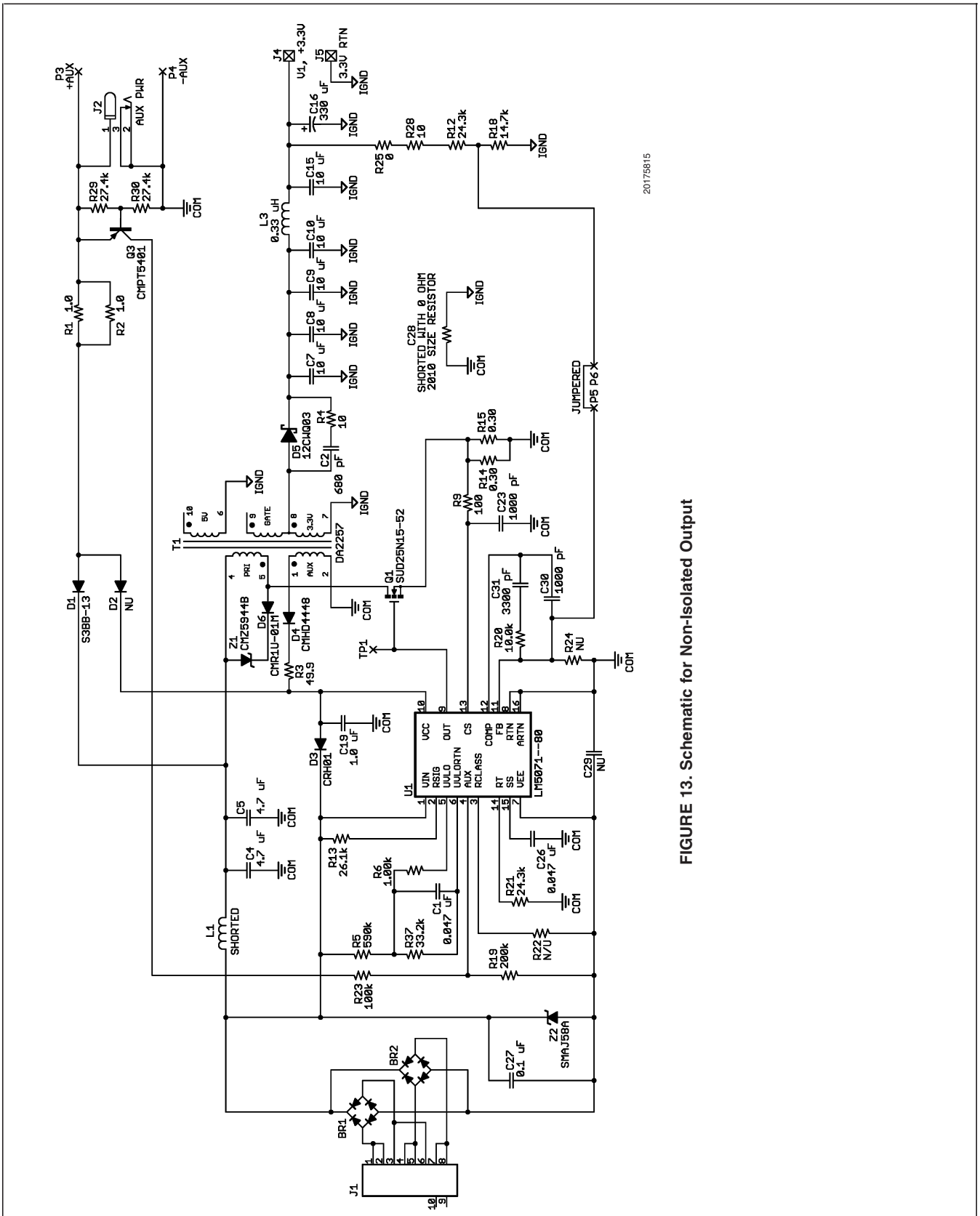


FIGURE 13. Schematic for Non-Isolated Output

A Note For Using The Efficiency Optimized EP13 Power Transformer DA2383

Please note that the DA2383 is a single output transformer. When using a DA2383 to obtain better efficiency (See Figure 3 for the applicable load and AUX input voltage levels), D5 should be removed and installed onto the Q2 pads on the top side of the evaluation board. This is because the secondary winding of DA2382 uses Pins 6 through 9 of the transformer bobbin, unlike DA2257 that only uses of Pins 7 and 8 for the secondary winding. The maximum converter stage efficiency at 3.3A will be expected to be greater than 84%.

A Few More Hints On Improving The Efficiency

Since the evaluation board is designed as a low cost solution, upgrading the following components with slightly more expensive devices will increase the efficiency.

(i) Use SUD15N15-95 for Q1; a faster device than the installed SUD25N15-52, to improve the dc-dc converter efficiency by 1%

(ii) Use DFLS1100 for D1; a 100V 1A high voltage Schottky barrier rectifier with low leakage current, to increase the AUX operation's end-to-end efficiency by at least 1%. This is suitable for an AUX input voltage greater than 15V.

Appendix: LM5071 Evaluation Board Bill of Materials

ITEM	PART NUMBER	DESCRIPTION	VALUE
BR1	CBRHD-01	DIODE BRIDGE, SMDIP, CENTRAL	0.5A, 100V
BR2	CBRHD-01	DIODE BRIDGE, SMDIP, CENTRAL	0.5A, 100V
C1	C0805C473K5RAC	CAP, CER, CC0805, KEMET	47nF, 50V
C2	C0805C681K5RAC	CAP, CER, CC0805, KEMET	680p, 50V
C4	C5750X7R2A475M	CAPACITOR, CER, CC2220, TDK	4.7µF, 100V
C5	C5750X7R2A475M	CAPACITOR, CER, CC2220, TDK	4.7µF, 100V
C7	C3216X5R0J106M	CAPACITOR, CER, CC1206, TDK	10µF, 6.3V
C8	C3216X5R0J106M	CAPACITOR, CER, CC1206, TDK	10µF, 6.3V
C9	C3216X5R0J106M	CAPACITOR, CER, CC1206, TDK	10µF, 6.3V
C10	C3216X5R0J106M	CAPACITOR, CER, CC1206, TDK	10µF, 6.3V
C15	C3216X5R0J106M	CAPACITOR, CER, CC1206, TDK	10µF, 6.3V
C16	EMVY6R3ADA331MF80G	CAPACITOR, AL ELEC, CHEMI-ON	330µF, 6.3V
C19	C2012X7R1E105K	CAPACITOR, CER, CC0805, TDK	1.0µF, 25V
C20	C2012X7R1E474K	CAPACITOR, CER, CC0805, TDK	0.47µF, 25V
C22	C0805C102K5RAC	CAP, CER, CC0805, KEMET	1nF, 50V
C23	C0805C102K5RAC	CAP, CER, CC0805, KEMET	1nF, 50V
C25	C0805C331K5RAC	CAP, CER, CC0805, KEMET	330pF, 50V
C26	C0805C473K5RAC	CAP, CER, CC0805, KEMET	47nF, 50V
C27	C2012X7R2A104K	CAPACITOR, CER, CC0805, TDK	100nF, 100V
C28	C4532X7R3D222k	CAPACITOR, CER, CC1812, TDK	2.2nF, 2 kV
C31	C0805C473K5RAC	CAP, CER, CC0805, KEMET	47nF, 50V
D1	S3BB-13	SCHOTTKY, SMB, DIODE INC	3A, 100V
D2	NU	ONLY INSTALL FOR AUX<14V	
D3	CRH01	SCHOTTKY, DO123, TOSHIBA	1A, 200V
D4	CMHD4448	DIODE, DO123, CENTRAL	125mA, 75V
D5	12CWQ03FN	SCHOTTKY, TO252, IR	12A, 30V
D6	CMR1U-01M	ULTRAFAST DIODE, CENTRAL	1A, 100V
J1	RJ-45-8N-B	RJ-45 CONNECTOR	
J2	PJ-102A	POWER JACK	
J4	3104-2-00-01-00-00-080	POST, MILL MAX	
J5	3104-2-00-01-00-00-080	POST, MILL MAX	
L1	bus-wire short	AWG #22 BUS WIRE	
L3	DO1813P-331MLD	SM INDUCTOR, COILCRAFT	0.33µH
P3	5012K-ND	TEST POINT, KEYSTONE	
P4	5012K-ND	TEST POINT, KEYSTONE	
Q1	SUD25N15-52	MOSFET, N-CH, TO252, VISHAY	150V, 25A
Q3	CMPT5401	BIPOLAR, PNP, SOT23, CENTRAL	150V, 1A

Appendix: LM5071 Evaluation Board Bill of Materials (Continued)

ITEM	PART NUMBER	DESCRIPTION	VALUE
R1	CRCW2512100J	RESISTOR	1Ω
R2	CRCW2512100J	RESISTOR	1Ω
R3	CRCW120649R9F	RESISTOR	49.9 Ω
R4	CRCW 120610R0F	RESISTOR	10 Ω
R5	CRCW08055903F	RESISTOR	590 kΩ
R6	CRCW08051001F	RESISTOR	1kΩ
R7	CRCW080510R0F	RESISTOR	10Ω
R9	CRCW08051000F	RESISTOR	100Ω
R11	CRCW08051002F	RESISTOR	10kΩ
R12	CRCW08052432F	RESISTOR	24.3kΩ
R13	CRCW08052612F	RESISTOR	26.1kΩ
R14	CRCW12060R301F	RESISTOR	0.301Ω
R15	CRCW12060R301F	RESISTOR	0.301Ω
R16	CRCW08051001F	RESISTOR	1kΩ
R17	CRCW08051001F	RESISTOR	1kΩ
R18	CRCW08051472F	RESISTOR	14.7kΩ
R19	CRCW08052003F	RESISTOR	200kΩ
R20	CRCW08056340F	RESISTOR	634Ω
R21	CRCW08052432F	RESISTOR	24.3kΩ
R22	NU	OPTIONAL FOR PD CLASS	
R23	CRCW08051003F	RESISTOR	100kΩ
R24	CRCW08050R0J	RESISTOR	0Ω
R25	CRCW08050R0J	RESISTOR	0Ω
R28	CRCW08053320F	RESISTOR	332Ω
R29	CRCW08052742F	RESISTOR	27.4kΩ
R30	CRCW08052742F	RESISTOR	27.4kΩ
R37	CRCW08053322F	RESISTOR	33.2kΩ
T1A	DA2257-AL	XFMR, DUAL OUTPUT FLYBACK, EP13, COILCRAFT	
T1B	DCT13EP-U12S005	XFMR, DUAL OUTPUT FLYBACK, EP13, TDK	
U1	LM5071-80		
U2A	PC3H7D	OPTO-COUPLER, SHARP	
U2B	PS2801-1-L	OPTIO-COUPLER, NEC	
U3	LMV431A		
Z1	CMZ5499B	ZENER, 62V, CENTRAL	
Z2	SMAJ58A	AVS, 58V, DIODE INC	

Additional BOM to Add An 1A, 5.5V Output Rail

ITEM	PART NUMBER	DESCRIPTION	VALUE
C12	C3216X5R1A106M	CAPACITOR, CER, CC1206, TDK	10µF, 10V
C13	C3216X5R1A106M	CAPACITOR, CER, CC1206, TDK	10µF, 10V
C14	C3216X5R1A106M	CAPACITOR, CER, CC1206, TDK	10µF, 10V
C17	EMVY100ADA101MF55G	CAPACITOR, AL ELEC, CHEMI-ON	100µF, 10V
D8	CMSH2-60	DIODE, SMA, CENTRAL	2A, 60V
J6	3104-2-00-01-00-00-080	POST, MILL MAX	
J7	3104-2-00-01-00-00-080	POST, MILL MAX	
L2	DO1813P-181MLD	SM INDUCTOR, COILCRAFT	0.18µH
Z4	CMZ5920B	ZENER, SMA, CENTRAL	6.2V

Note: The total load of the dual outputs should be limited below 10W maximum.

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