

# **LH28F640BFHE-PBTL70A**

Flash Memory  
64Mbit (4Mbitx16)

(Model Number: LHF64FG8)

Spec. Issue Date: June 1, 2004  
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To: \_\_\_\_\_

## S P E C I F I C A T I O N S

Product Type 64 Mbit Flash Memory

**LH28F640BFHE — PBTL70A**

Model No. (LHF64FG8)

If you have any objections, please contact us before issuing purchasing order.

\* This specifications contains 42 pages including the cover and appendix.

\* Refer to LH28F640BF Series Appendix (FUM00701).

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# LH28F640BFHE-PBTL70A

## 64Mbit (4Mbit×16)

### Page Mode Dual Work Flash MEMORY

- 64M density with 16Bit I/O Interface
- High Performance Reads
  - 70/30ns 8-Word Page Mode
- Configurative 4-Plane Dual Work
  - Flexible Partitioning
  - Read operations during Block Erase or (Page Buffer) Program
  - Status Register for Each Partition
- Low Power Operation
  - 2.7V Read and Write Operations
  - $V_{CCQ}$  for Input/Output Power Supply Isolation
  - Automatic Power Savings Mode Reduces  $I_{CCR}$  in Static Mode
- Enhanced Code + Data Storage
  - 5 $\mu$ s Typical Erase/Program Suspends
- OTP (One Time Program) Block
  - 4-Word Factory-Programmed Area
  - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
  - 16-Word Page Buffer
  - 5 $\mu$ s/Word (Typ.) at 9.5V  $V_{PP}$
- Operating Temperature -40°C to +85°C
- CMOS Process (P-type silicon substrate)
- Flexible Blocking Architecture
  - Eight 4K-word Parameter Blocks
  - One-hundred and twenty-seven 32K-word Main Blocks
  - Bottom Parameter Location
- Enhanced Data Protection Features
  - Individual Block Lock and Block Lock-Down with Zero-Latency
  - All blocks are locked at power-up or device reset.
  - Absolute Protection with  $V_{PP} \leq V_{PPLK}$
  - Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
  - 3.0V Low-Power 11 $\mu$ s/Word (Typ.) Programming
  - 9.5V No Glue Logic 9 $\mu$ s/Word (Typ.) Production Programming and 0.5s Erase (Typ.)
- Cross-Compatible Command Support
  - Basic Command Set
  - Common Flash Interface (CFI)
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- 48-Lead TSOP
- ETOX<sup>TM</sup>\* Flash Technology
- Not designed or rated as radiation hardened

The product, which is 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at  $V_{CC}=2.7V-3.6V$  and  $V_{PP}=1.65V-3.6V$  or  $9.0V-10.0V$ . Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

\* ETOX is a trademark of Intel Corporation.

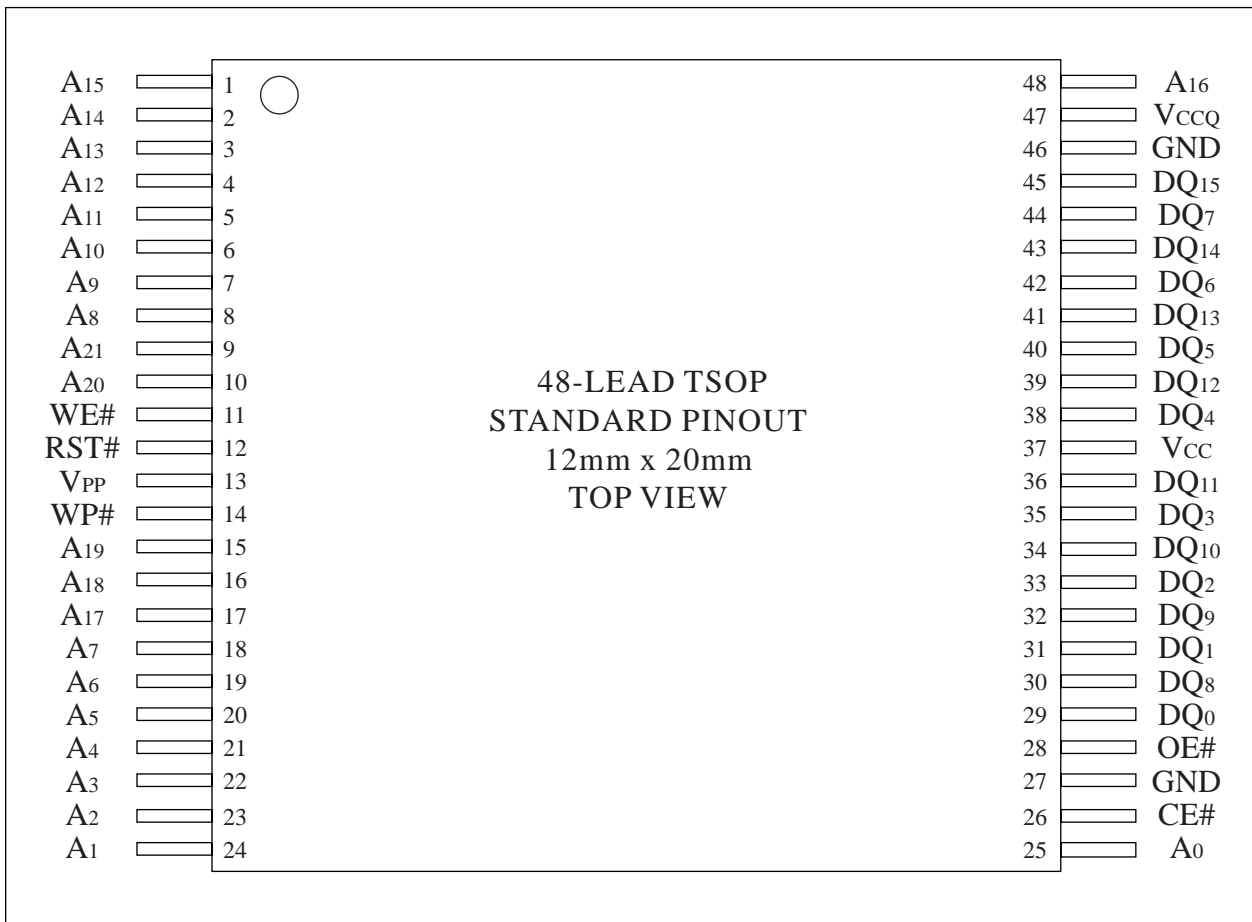


Figure 1. 48-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A <sub>0</sub> -A <sub>21</sub>	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M: A <sub>0</sub> -A <sub>21</sub>
DQ <sub>0</sub> -DQ <sub>15</sub>	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V <sub>IH</sub> ) deselected the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V <sub>IL</sub> ), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V <sub>IH</sub> ) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V <sub>IL</sub> , locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP# is V <sub>IH</sub> , lock-down is disabled.
V <sub>PP</sub>	INPUT/SUPPLY	MONITORING POWER SUPPLY VOLTAGE: V <sub>PP</sub> is not used for power supply pin. With V <sub>PP</sub> ≤ V <sub>PPLK</sub> , block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 9.5V ± 0.5V to V <sub>PP</sub> provides fast erasing or fast programming mode. In this mode, V <sub>PP</sub> is power supply pin. Applying 9.5V ± 0.5V to V <sub>PP</sub> during erase/program can only be done for a maximum of 1,000 cycles on each block. V <sub>PP</sub> may be connected to 9.5V ± 0.5V for a total of 80 hours maximum. Use of this pin at 9.5V beyond these limits may reduce block cycling capability or cause permanent damage.
V <sub>CC</sub>	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With V <sub>CC</sub> ≤ V <sub>LKO</sub> , all write attempts to the flash memory are inhibited. Device operations at invalid V <sub>CC</sub> voltage (see DC Characteristics) produce spurious results and should not be attempted.
V <sub>CCQ</sub>	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.

Table 2. Simultaneous Operation Modes Allowed with Four Planes<sup>(1, 2)</sup>

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:

- "X" denotes the operation available.
- Configurative Partition Dual Work Restrictions:  
 Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing.  
 Commands must be written to an address within the block targeted by that command.



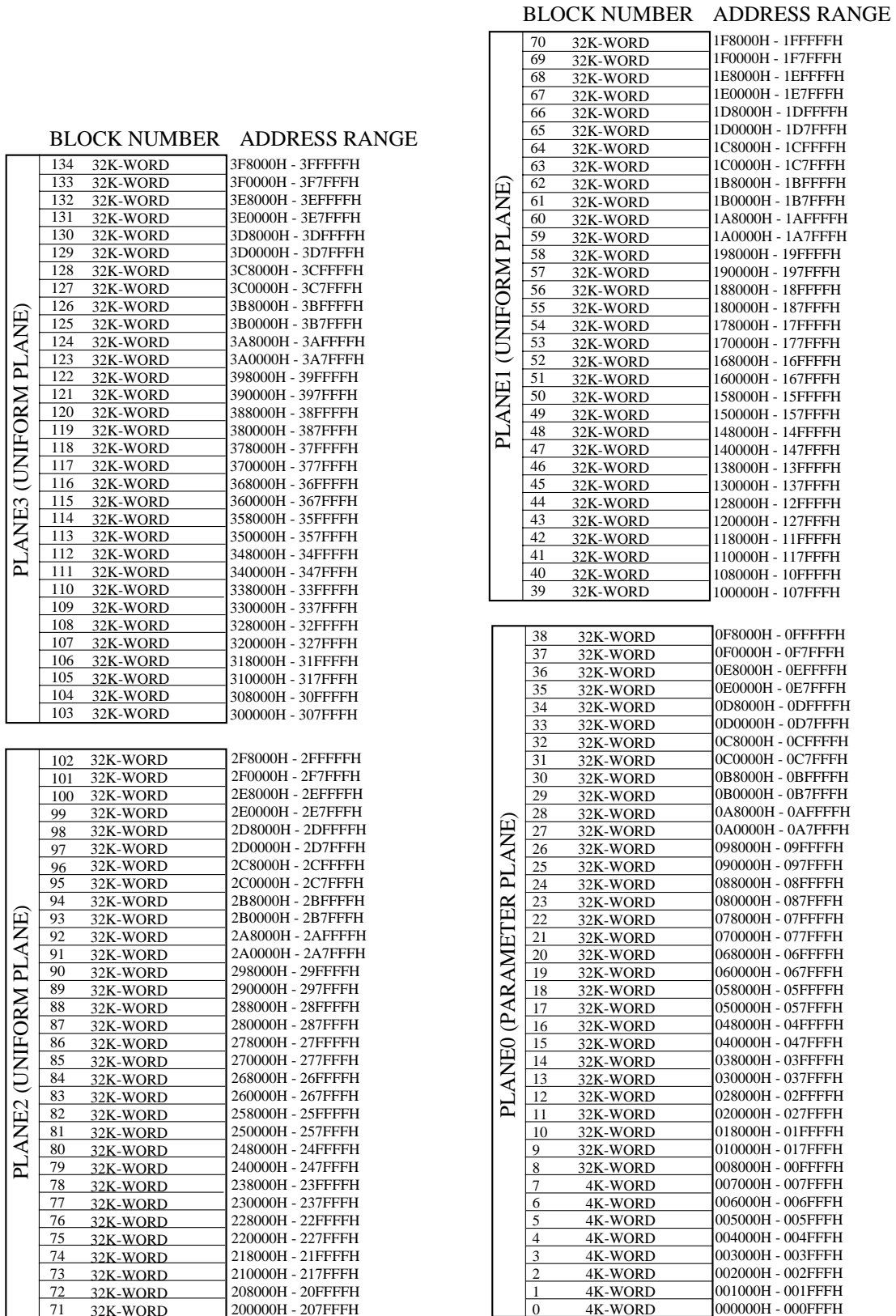


Figure 2. Memory Map (Bottom Parameter)

Table 3. Identifier Codes and OTP Address for Read Operation

	Code	Address [A <sub>15</sub> -A <sub>0</sub> ]	Data [DQ <sub>15</sub> -DQ <sub>0</sub> ]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	1
Device Code	Bottom Parameter Device Code	0001H	00B3H	1, 2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ <sub>0</sub> = 0	3
	Block is Locked		DQ <sub>0</sub> = 1	3
	Block is not Locked-Down		DQ <sub>1</sub> = 0	3
	Block is Locked-Down		DQ <sub>1</sub> = 1	3
Device Configuration Code	Partition Configuration Register	0006H	PCRC	1, 4
OTP	OTP Lock	0080H	OTP-LK	1, 5
	OTP	0081-0088H	OTP	1, 6

NOTES:

1. The address A<sub>21</sub>-A<sub>16</sub> are shown in below table for reading the manufacturer code, device code, device configuration code and OTP data.
2. Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
3. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written.  
DQ<sub>15</sub>-DQ<sub>2</sub> are reserved for future implementation.
4. PCRC=Partition Configuration Register Code.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.

Table 5. Identifier Codes and OTP Address for Read Operation on Partition Configuration<sup>(1)</sup> (64M-bit device)

Partition Configuration Register <sup>(2)</sup>			Address (64M-bit device) [A <sub>21</sub> -A <sub>16</sub> ]
PCR.10	PCR.9	PCR.8	
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

NOTES:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 12 for the partition configuration register.

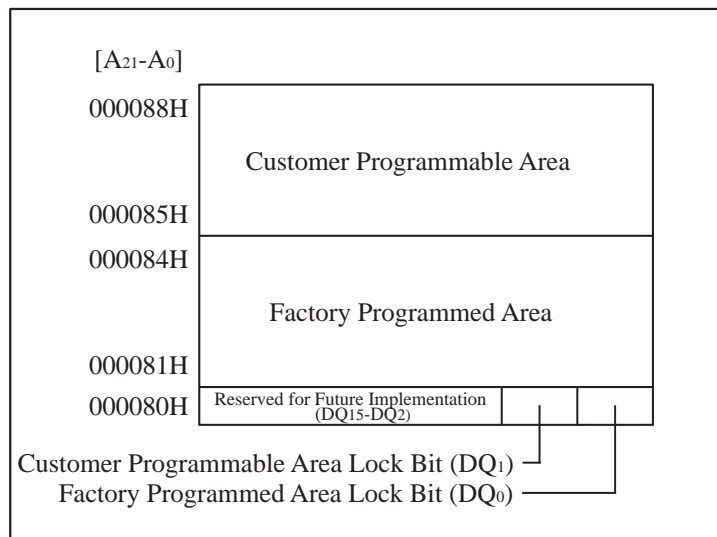


Figure 3. OTP Block Address Map for OTP Program  
(The area outside 80H~88H cannot be used.)

Table 6. Bus Operation<sup>(1, 2)</sup>

Mode	Notes	RST#	CE#	OE#	WE#	Address	V <sub>PP</sub>	DQ <sub>0-15</sub>
Read Array	6	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>
Output Disable		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z
Standby		V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	High Z
Reset	3	V <sub>IL</sub>	X	X	X	X	X	High Z
Read Identifier Codes/OTP	6	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Table 3 and Table 4	X	See Table 3 and Table 4
Read Query	6,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Appendix	X	See Appendix
Write	4,5,6	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	D <sub>IN</sub>

## NOTES:

1. Refer to DC Characteristics. When  $V_{PP} \leq V_{PPLK}$ , memory contents can be read, but cannot be altered.
2. X can be V<sub>IL</sub> or V<sub>IH</sub> for control pins and addresses, and V<sub>PPLK</sub> or V<sub>PPH1/2</sub> for V<sub>PP</sub>. See DC Characteristics for V<sub>PPLK</sub> and V<sub>PPH1/2</sub> voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when  $V_{PP} = V_{PPH1/2}$  and  $V_{CC} = 2.7V - 3.6V$ .
5. Refer to Table 6 for valid D<sub>IN</sub> during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F640BF series for more information about query code.

Table 7. Command Definitions<sup>(11)</sup>

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data	Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3)</sup>
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5,9	Write	X	30H	Write	X	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	C0H	Write	OA	OD
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

## NOTES:

- Bus operations are defined in Table 5.
- All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.  
X=Any valid address within the device.  
PA=Address within the selected partition.  
IA=Identifier codes address (See Table 3 and Table 4).  
QA=Query codes address. Refer to Appendix of LH28F640BF series for details.  
BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.  
WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.  
OA=Address of OTP block to be read or programmed (See Figure 3).  
PCRC=Partition configuration register code presented on the address A<sub>0</sub>-A<sub>15</sub>.
- ID=Data read from identifier codes. (See Table 3 and Table 4).  
QD=Data read from query database. Refer to Appendix of LH28F640BF series for details.  
SRD=Data read from status register. See Table 10 for a description of the status register bits.  
WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.  
OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.  
N-1=N is the number of the words to be loaded into a page buffer.
- Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4).  
The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V<sub>IH</sub>.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Appendix of

LH28F640BF series for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is  $V_{IL}$ . When WP# is  $V_{IH}$ , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 8. Functions of Block Lock<sup>(5)</sup> and Block Lock-Down

Current State					Erase/Program Allowed <sup>(2)</sup>
State	WP#	DQ <sub>1</sub> <sup>(1)</sup>	DQ <sub>0</sub> <sup>(1)</sup>	State Name	
[000]	0	0	0	Unlocked	Yes
[001] <sup>(3)</sup>	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] <sup>(3)</sup>	1	0	1	Locked	No
[110] <sup>(4)</sup>	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

## NOTES:

- DQ<sub>0</sub>=1: a block is locked; DQ<sub>0</sub>=0: a block is unlocked.  
DQ<sub>1</sub>=1: a block is locked-down; DQ<sub>1</sub>=0: a block is not locked-down.
- Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
- At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
- When WP# is driven to V<sub>IL</sub> in [110] state, the state changes to [011] and the blocks are automatically locked.
- OTP (One Time Program) block has the lock function which is different from those described above.

Table 9. Block Locking State Transitions upon Command Write<sup>(4)</sup>

Current State				Result after Lock Command Written (Next State)		
State	WP#	DQ <sub>1</sub>	DQ <sub>0</sub>	Set Lock <sup>(1)</sup>	Clear Lock <sup>(1)</sup>	Set Lock-down <sup>(1)</sup>
[000]	0	0	0	[001]	No Change	[011] <sup>(2)</sup>
[001]	0	0	1	No Change <sup>(3)</sup>	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] <sup>(2)</sup>
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] <sup>(2)</sup>
[111]	1	1	1	No Change	[110]	No Change

## NOTES:

- "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
- When the Set Block Lock-Down Bit command is written to the unlocked block (DQ<sub>0</sub>=0), the corresponding block is locked-down and automatically locked at the same time.
- "No Change" means that the state remains unchanged after the command written.
- In this state transitions table, assumes that WP# is not changed and fixed V<sub>IL</sub> or V<sub>IH</sub>.

Table 10. Block Locking State Transitions upon WP# Transition<sup>(4)</sup>

Previous State	Current State				Result after WP# Transition (Next State)	
	State	WP#	DQ <sub>1</sub>	DQ <sub>0</sub>	WP#=0→1 <sup>(1)</sup>	WP#=1→0 <sup>(1)</sup>
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] <sup>(2)</sup>	[011]	0	1	1	[110]	-
Other than [110] <sup>(2)</sup>					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] <sup>(3)</sup>
-	[111]	1	1	1	-	[011]

## NOTES:

1. "WP#=0→1" means that WP# is driven to V<sub>IH</sub> and "WP#=1→0" means that WP# is driven to V<sub>IL</sub>.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to V<sub>IL</sub> in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.



Table 11. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

<p>SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES) 1 = Error in Block Erase or Full Chip Erase 0 = Successful Block Erase or Full Chip Erase</p> <p>SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS) 1 = Error in (Page Buffer) Program or OTP Program 0 = Successful (Page Buffer) Program or OTP Program</p> <p>SR.3 = V<sub>PP</sub> STATUS (VPPS) 1 = V<sub>PP</sub> LOW Detect, Operation Abort 0 = V<sub>PP</sub> OK</p> <p>SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p>NOTES:</p> <p>Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.</p> <p>Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V<sub>PP</sub> level. The WSM interrogates and indicates the V<sub>PP</sub> level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when V<sub>PP</sub>≠V<sub>PPH1</sub>, V<sub>PPH2</sub> or V<sub>PPLK</sub>.</p> <p>SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.</p> <p>SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.</p>
--	--

Table 12. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

<p>XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>XSR.7 = STATE MACHINE STATUS (SMS)          1 = Page Buffer Program available          0 = Page Buffer Program not available</p> <p>XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p>NOTES:</p> <p>After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.</p> <p>XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.</p>
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Table 13. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

<p>PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>PCR.10-8 = PARTITION CONFIGURATION (PC2-0)</p> <p>000 = No partitioning. Dual Work is not allowed.</p> <p>001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)</p> <p>010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.</p> <p>100 = Plane 0-2 are merged into one partition. (default in a top parameter device)</p> <p>011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p> <p>110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p> <p>101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p>	<p>111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.</p> <p>PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>NOTES:</p> <p>After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.</p> <p>See Figure 4 for the detail on partition configuration.</p> <p>PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.</p>
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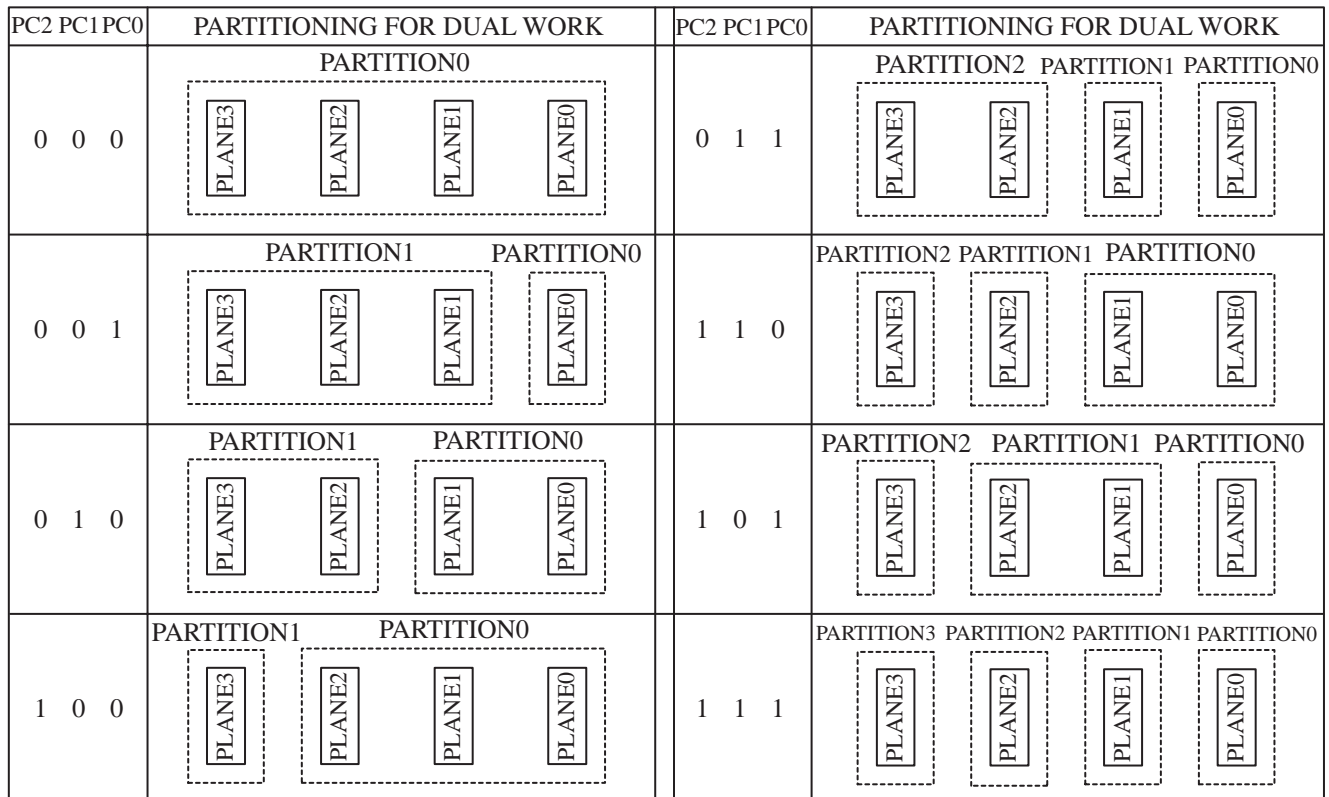


Figure 4. Partition Configuration

## 1 Electrical Specifications

### 1.1 Absolute Maximum Ratings\*

#### Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

#### Storage Temperature

During under Bias..... -40°C to +85°C

During non Bias..... -65°C to +125°C

#### Voltage On Any Pin

(except V<sub>CC</sub> and V<sub>PP</sub>)..... -0.5V to V<sub>CC</sub>+0.5V (2)

V<sub>CC</sub> and V<sub>CCQ</sub> Supply Voltage ..... -0.2V to +3.9V (2)

V<sub>PP</sub> Supply Voltage ..... -0.2V to +10.0V (2, 3, 4)

Output Short Circuit Current ..... 100mA (5)

*\*WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

#### NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V<sub>CC</sub> and V<sub>PP</sub> pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V<sub>CC</sub>+0.5V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.
3. Maximum DC voltage on V<sub>PP</sub> may overshoot to +11.0V for periods <20ns.
4. V<sub>PP</sub> erase/program voltage is normally 2.7V-3.6V. Applying 9.0V-10.0V to V<sub>PP</sub> during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V<sub>PP</sub> may be connected to 9.0V-10.0V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

### 1.2 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T <sub>A</sub>	-40	+25	+85	°C	
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	1
I/O Supply Voltage	V <sub>CCQ</sub>	2.7	3.0	3.6	V	1
V <sub>PP</sub> Voltage when Used as a Logic Control	V <sub>PPH1</sub>	1.65	3.0	3.6	V	1
V <sub>PP</sub> Supply Voltage	V <sub>PPH2</sub>	9.0	9.5	10.0	V	1, 2
Main Block Erase Cycling: V <sub>PP</sub> =V <sub>PPH1</sub>		100,000			Cycles	
Parameter Block Erase Cycling: V <sub>PP</sub> =V <sub>PPH1</sub>		100,000			Cycles	
Main Block Erase Cycling: V <sub>PP</sub> =V <sub>PPH2</sub> , 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: V <sub>PP</sub> =V <sub>PPH2</sub> , 80 hrs.				1,000	Cycles	
Maximum V <sub>PP</sub> hours at V <sub>PPH2</sub>				80	Hours	

#### NOTES:

1. See DC Characteristics tables for voltage range-specific specification.
2. Applying V<sub>PP</sub>=9.0V-10.0V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V<sub>PP</sub>=9.0V-10.0V is not allowed and can cause damage to the device.

### 1.2.1 Capacitance<sup>(1)</sup> ( $T_A=+25^\circ\text{C}$ , $f=1\text{MHz}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN}=0.0\text{V}$		4	7	pF
Output Capacitance	$C_{OUT}$	$V_{OUT}=0.0\text{V}$		6	10	pF

**NOTE:**

1. Sampled, not 100% tested.

### 1.2.2 AC Input/Output Test Conditions

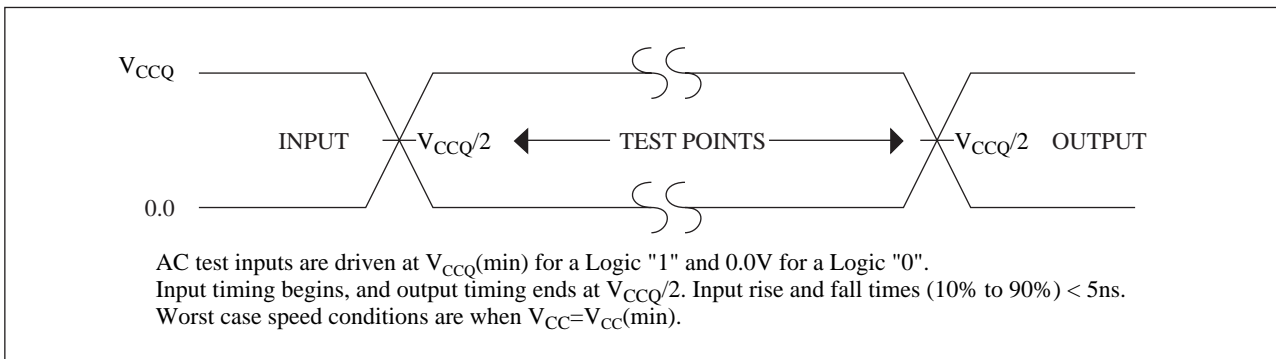


Figure 5. Transient Input/Output Reference Waveform for  $V_{CC}=2.7\text{V}-3.6\text{V}$

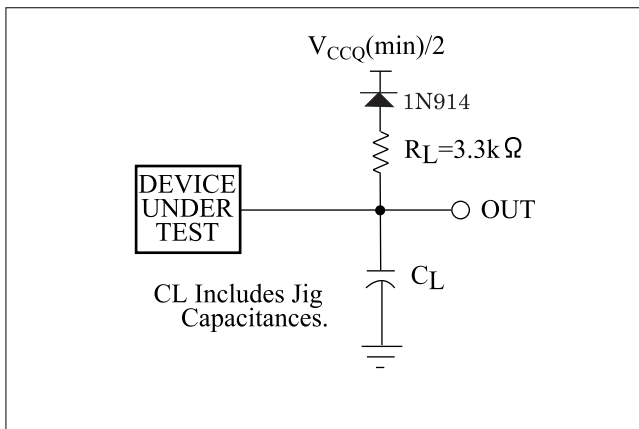


Figure 6. Transient Equivalent Testing Load Circuit

Table 14. Configuration Capacitance Loading Value

Test Configuration	$C_L$ (pF)
$V_{CC}=2.7\text{V}-3.6\text{V}$	70

## 1.2.3 DC Characteristics

$V_{CC}=2.7V-3.6V$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
$I_{LI}$	Input Load Current	1	-1.0		+1.0	$\mu A$	$V_{CC}=V_{CCMax.}$ ,
$I_{LO}$	Output Leakage Current	1	-1.0		+1.0	$\mu A$	$V_{CCQ}=V_{CCQMax.}$ , $V_{IN}/V_{OUT}=V_{CCQ}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,8		4	20	$\mu A$	$V_{CC}=V_{CCMax.}$ , CE#=RST#= $V_{CCQ}\pm 0.2V$ , WP#= $V_{CCQ}$ or GND
$I_{CCAS}$	$V_{CC}$ Automatic Power Savings Current	1,4,8		4	20	$\mu A$	$V_{CC}=V_{CCMax.}$ , CE#=GND $\pm 0.2V$ , WP#= $V_{CCQ}$ or GND
$I_{CCD}$	$V_{CC}$ Reset Current	1,8		4	20	$\mu A$	RST#=GND $\pm 0.2V$
$I_{CCR}$	Average $V_{CC}$ Read Current Normal Mode	1,7,8		15	25	mA	$V_{CC}=V_{CCMax.}$ , CE#= $V_{IL}$ , OE#= $V_{IH}$ , f=5MHz
	Average $V_{CC}$ Read Current Page Mode	8 Word Read	1,7,8	5	10	mA	
$I_{CCW}$	$V_{CC}$ (Page Buffer) Program Current	1,5,7,8		20	60	mA	$V_{PP}=V_{PPH1}$
		1,5,7,8		10	20	mA	$V_{PP}=V_{PPH2}$
$I_{CCE}$	$V_{CC}$ Block Erase, Full Chip Erase Current	1,5,7,8		10	30	mA	$V_{PP}=V_{PPH1}$
		1,5,7,8		4	10	mA	$V_{PP}=V_{PPH2}$
$I_{CCWS}$ $I_{CCES}$	$V_{CC}$ (Page Buffer) Program or Block Erase Suspend Current	1,2,7,8		10	200	$\mu A$	CE#= $V_{IH}$
$I_{PPS}$ $I_{PPR}$	$V_{PP}$ Standby or Read Current	1,6,7,8		2	5	$\mu A$	$V_{PP}\leq V_{CC}$
$I_{PPW}$	$V_{PP}$ (Page Buffer) Program Current	1,5,6,7,8		2	5	$\mu A$	$V_{PP}=V_{PPH1}$
		1,5,6,7,8		10	30	mA	$V_{PP}=V_{PPH2}$
$I_{PPE}$	$V_{PP}$ Block Erase, Full Chip Erase Current	1,5,6,7,8		2	5	$\mu A$	$V_{PP}=V_{PPH1}$
		1,5,6,7,8		5	15	mA	$V_{PP}=V_{PPH2}$
$I_{PPWS}$	$V_{PP}$ (Page Buffer) Program Suspend Current	1,6,7,8		2	5	$\mu A$	$V_{PP}=V_{PPH1}$
		1,6,7,8		10	200	$\mu A$	$V_{PP}=V_{PPH2}$
$I_{PPES}$	$V_{PP}$ Block Erase Suspend Current	1,6,7,8		2	5	$\mu A$	$V_{PP}=V_{PPH1}$
		1,6,7,8		10	200	$\mu A$	$V_{PP}=V_{PPH2}$

## DC Characteristics (Continued)

$V_{CC}=2.7V-3.6V$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	5	-0.4		0.4	V	
$V_{IH}$	Input High Voltage	5	2.4		$V_{CCQ} + 0.4$	V	
$V_{OL}$	Output Low Voltage	5			0.2	V	$V_{CC}=V_{CCMin.}$ , $V_{CCQ}=V_{CCQMin.}$ , $I_{OL}=100\mu A$
$V_{OH}$	Output High Voltage	5	$V_{CCQ} - 0.2$			V	$V_{CC}=V_{CCMin.}$ , $V_{CCQ}=V_{CCQMin.}$ , $I_{OH}=-100\mu A$
$V_{PPLK}$	$V_{PP}$ Lockout during Normal Operations	3,5,6			0.4	V	
$V_{PPH1}$	$V_{PP}$ during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations	6	1.65	3.0	3.6	V	
$V_{PPH2}$	$V_{PP}$ during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations	6	9.0	9.5	10.0	V	
$V_{LKO}$	$V_{CC}$ Lockout Voltage		1.5			V	

## NOTES:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at  $V_{CC}=3.0V$  and  $T_A=+25^\circ C$  unless  $V_{CC}$  is specified.
- $I_{CCWS}$  and  $I_{CCES}$  are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of  $I_{CCES}$  and  $I_{CCR}$  or  $I_{CCW}$ . If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of  $I_{CCWS}$  and  $I_{CCR}$ .
- Block erase, full chip erase, (page buffer) program and OTP program are inhibited when  $V_{PP} \leq V_{PPLK}$ , and not guaranteed in the range between  $V_{PPLK}(max.)$  and  $V_{PPH1}(min.)$ , between  $V_{PPH1}(max.)$  and  $V_{PPH2}(min.)$  and above  $V_{PPH2}(max.)$ .
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ( $t_{AVQV}$ ) provide new data when addresses are changed.
- Sampled, not 100% tested.
- $V_{PP}$  is not used for power supply pin. With  $V_{PP} \leq V_{PPLK}$ , block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.  
Applying  $9.5V \pm 0.5V$  to  $V_{PP}$  provides fast erasing or fast programming mode. In this mode,  $V_{PP}$  is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the  $V_{CC}$  power bus.  
Applying  $9.5V \pm 0.5V$  to  $V_{PP}$  during erase/program can only be done for a maximum of 1,000 cycles on each block.  $V_{PP}$  may be connected to  $9.5V \pm 0.5V$  for a total of 80 hours maximum.
- The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
- For all pins other than those shown in test conditions, input level is  $V_{CCQ}$  or GND.

1.2.4 AC Characteristics - Read-Only Operations<sup>(1)</sup>
 $V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{AVAV}$	Read Cycle Time		70		ns
$t_{AVQV}$	Address to Output Delay			70	ns
$t_{ELQV}$	CE# to Output Delay	3		70	ns
$t_{APA}$	Page Address Access Time			30	ns
$t_{GLQV}$	OE# to Output Delay	3		25	ns
$t_{PHQV}$	RST# High to Output Delay			150	ns
$t_{EHQZ}, t_{GHQZ}$	CE# or OE# to Output in High Z, Whichever Occurs First	2		25	ns
$t_{ELQX}$	CE# to Output in Low Z	2	0		ns
$t_{GLQX}$	OE# to Output in Low Z	2	0		ns
$t_{OH}$	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns
$t_{AVEL}, t_{AVGL}$	Address Setup to CE#, OE# Going Low for Reading Status Register	4, 6	10		ns
$t_{ELAX}, t_{GLAX}$	Address Hold from CE#, OE# Going Low for Reading Status Register	5, 6	30		ns
$t_{EHEL}, t_{GHGL}$	CE#, OE# Pulse Width High for Reading Status Register	6	15		ns

## NOTES:

1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to  $t_{ELQV} - t_{GLQV}$  after the falling edge of CE# without impact to  $t_{ELQV}$ .
4. Address setup time ( $t_{AVEL}, t_{AVGL}$ ) is defined from the falling edge of CE# or OE# (whichever goes low last).
5. Address hold time ( $t_{ELAX}, t_{GLAX}$ ) is defined from the falling edge of CE# or OE# (whichever goes low last).
6. Specifications  $t_{AVEL}, t_{AVGL}, t_{ELAX}, t_{GLAX}$  and  $t_{EHEL}, t_{GHGL}$  for read operations apply to only status register read operations.



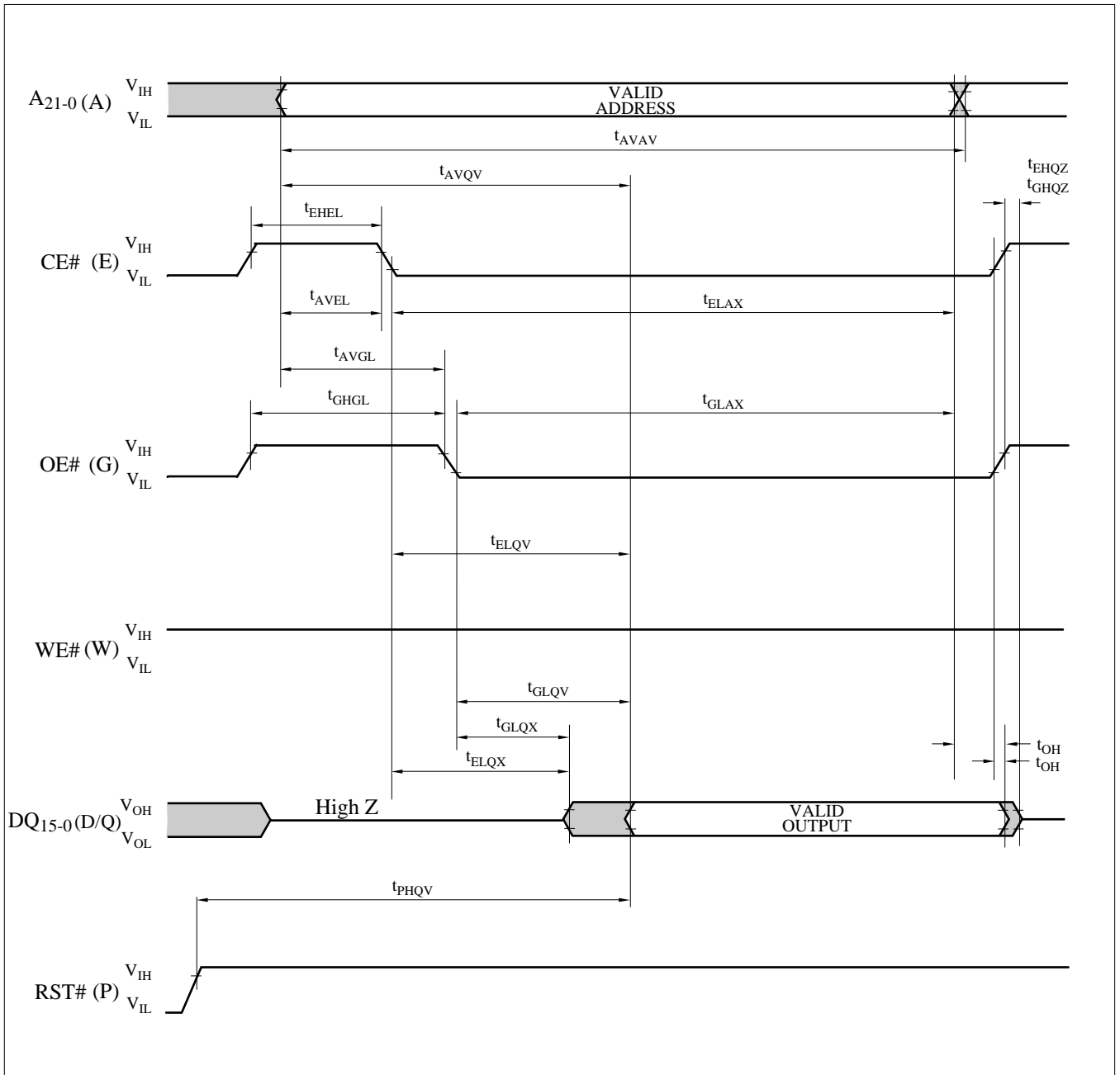


Figure 7. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code

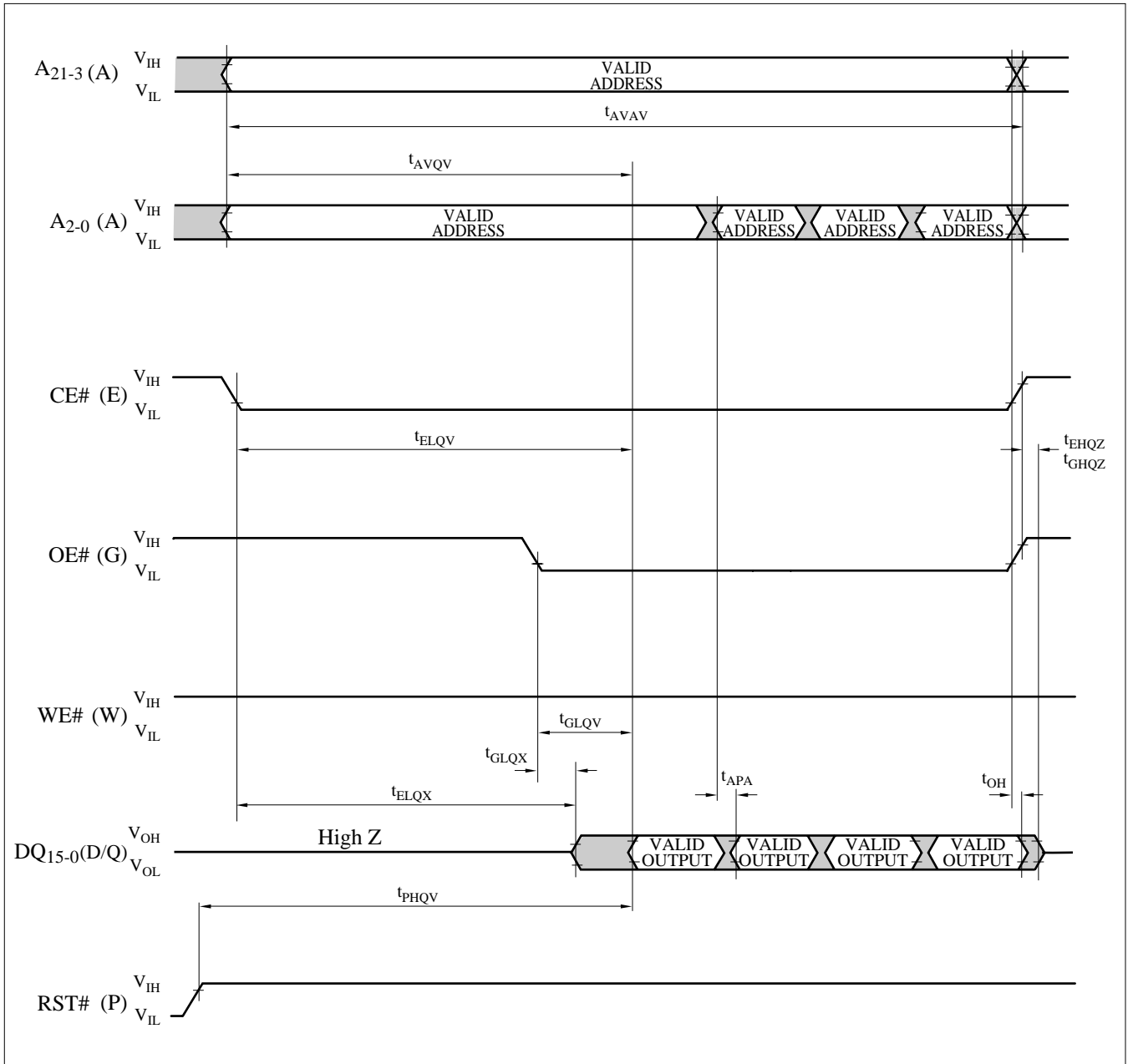


Figure 8. AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks

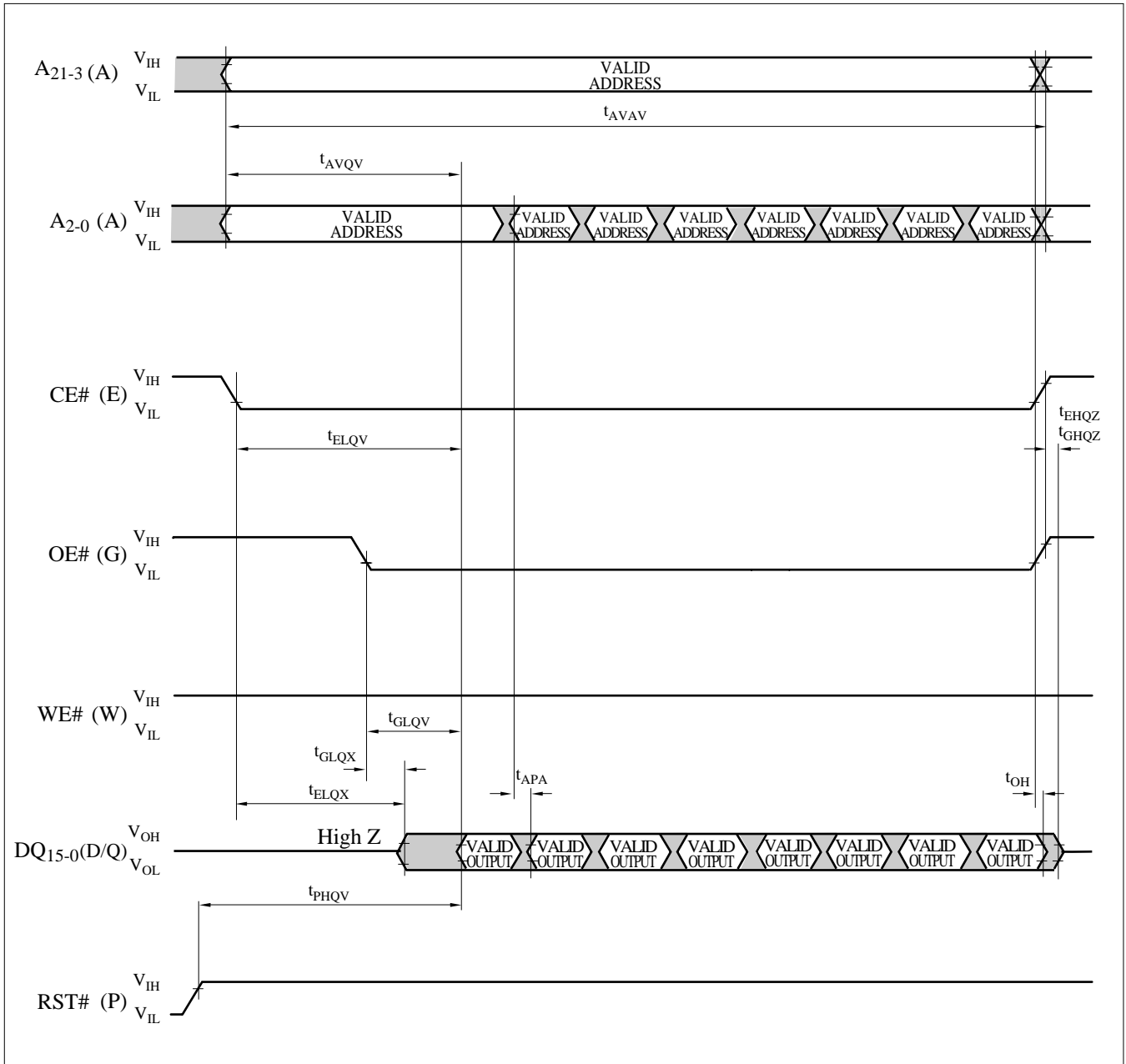


Figure 9. AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks

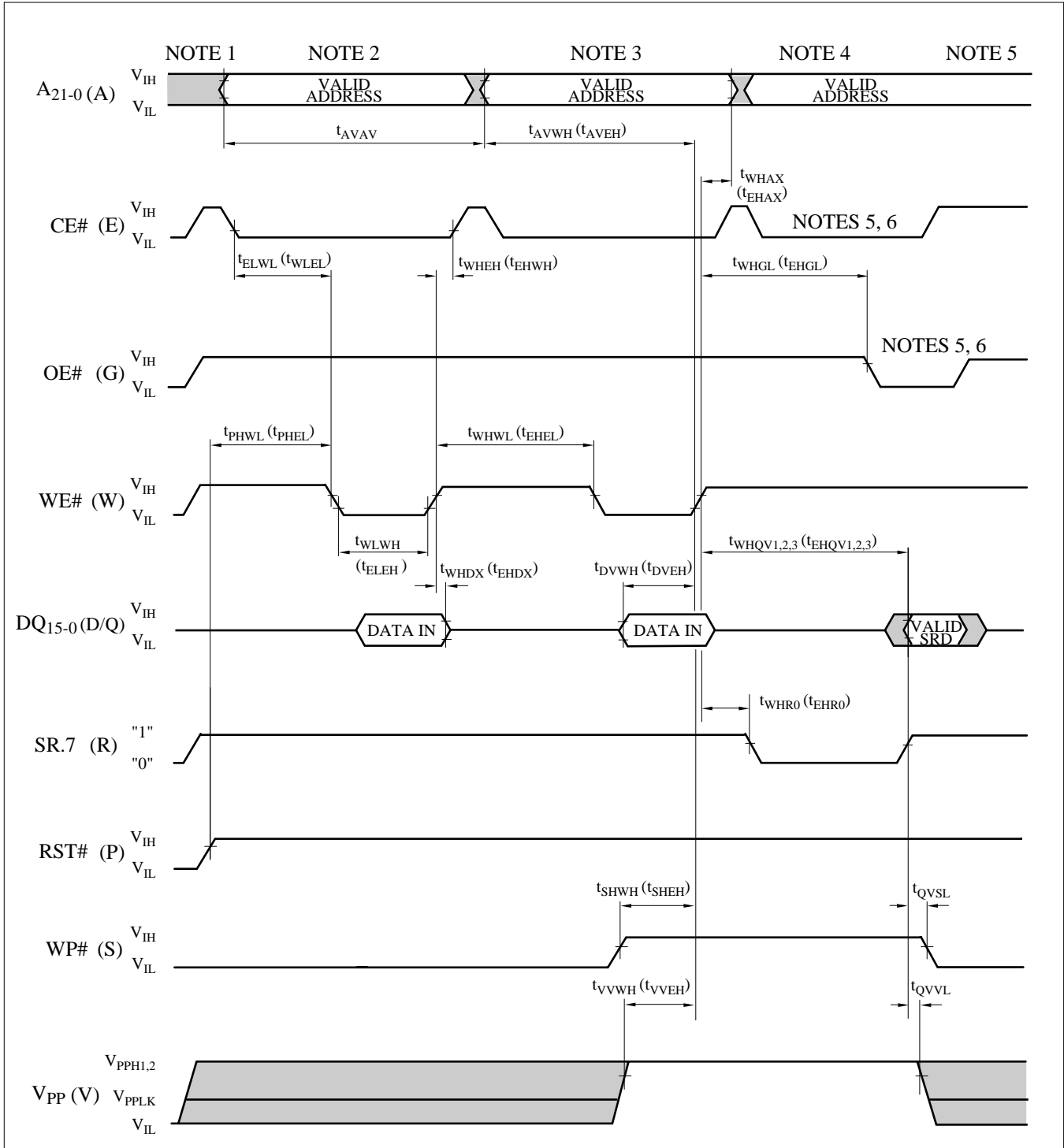
1.2.5 AC Characteristics - Write Operations<sup>(1), (2)</sup>

$$V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{AVAV}$	Write Cycle Time		70		ns
$t_{PHWL}$ ( $t_{PHEL}$ )	RST# High Recovery to WE# (CE#) Going Low	3	150		ns
$t_{ELWL}$ ( $t_{WLEL}$ )	CE# (WE#) Setup to WE# (CE#) Going Low		0		ns
$t_{WLWH}$ ( $t_{ELEH}$ )	WE# (CE#) Pulse Width	4	55		ns
$t_{DVWH}$ ( $t_{DVEH}$ )	Data Setup to WE# (CE#) Going High	8	40		ns
$t_{AVWH}$ ( $t_{AVEH}$ )	Address Setup to WE# (CE#) Going High	8	55		ns
$t_{WHEH}$ ( $t_{EHWH}$ )	CE# (WE#) Hold from WE# (CE#) High		0		ns
$t_{WHDX}$ ( $t_{EHDX}$ )	Data Hold from WE# (CE#) High		0		ns
$t_{WHAX}$ ( $t_{EHAX}$ )	Address Hold from WE# (CE#) High		0		ns
$t_{WHWL}$ ( $t_{EHEL}$ )	WE# (CE#) Pulse Width High	5	15		ns
$t_{SHWH}$ ( $t_{SHEH}$ )	WP# High Setup to WE# (CE#) Going High	3	0		ns
$t_{VVWH}$ ( $t_{VVEH}$ )	$V_{PP}$ Setup to WE# (CE#) Going High	3	200		ns
$t_{WHGL}$ ( $t_{EHGL}$ )	Write Recovery before Read		30		ns
$t_{QVSL}$	WP# High Hold from Valid SRD	3, 6	0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD	3, 6	0		ns
$t_{WHR0}$ ( $t_{EHR0}$ )	WE# (CE#) High to SR.7 Going "0"	3, 7		$t_{AVQV}+$ 50	ns

## NOTES:

- The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- A write operation can be initiated and terminated with either CE# or WE#.
- Sampled, not 100% tested.
- Write pulse width ( $t_{WP}$ ) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence,  $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$ .
- Write pulse width high ( $t_{WPH}$ ) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence,  $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$ .
- $V_{PP}$  should be held at  $V_{PP}=V_{PPH1/2}$  until determination of block erase, full chip erase, (page buffer) program or OTP program success (SR.1/3/4/5=0).
- $t_{WHR0}$  ( $t_{EHR0}$ ) after the Read Query or Read Identifier Codes/OTP command= $t_{AVQV}+100ns$ .
- Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.



- NOTES:
1.  $V_{CC}$  power-up and standby.
  2. Write each first cycle command.
  3. Write each second cycle command or valid address and data.
  4. Automated erase or program delay.
  5. Read status register data.
  6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 10. AC Waveform for Write Operations

## 1.2.6 Reset Operations

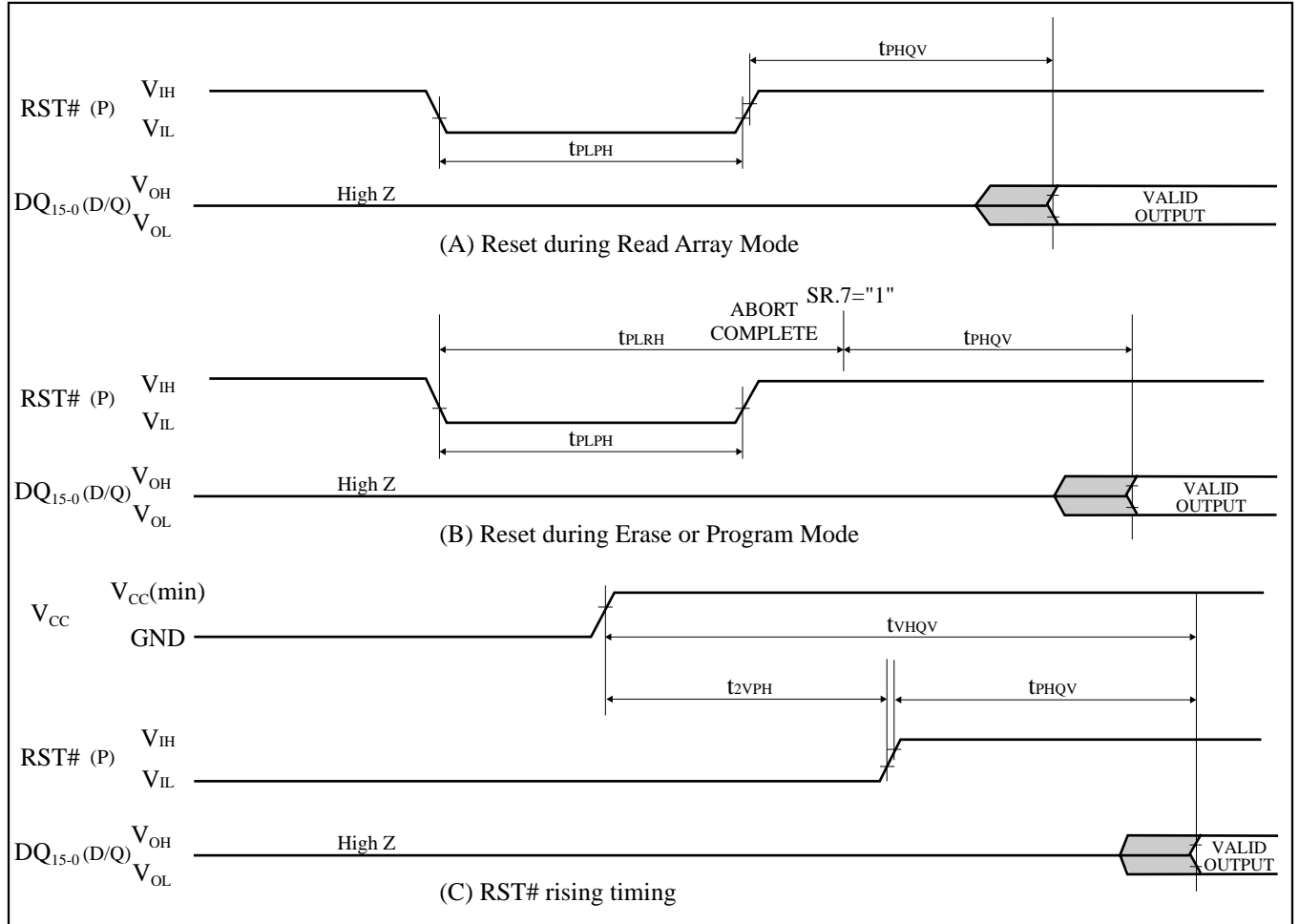


Figure 11. AC Waveform for Reset Operations

Reset AC Specifications ( $V_{CC}=2.7V-3.6V$ ,  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{PLPH}$	RST# Low to Reset during Read (RST# should be low during power-up.)	1, 2, 3	100		ns
$t_{PLRH}$	RST# Low to Reset during Erase or Program	1, 3, 4		22	$\mu s$
$t_{2VPH}$	$V_{CC}$ 2.7V to RST# High	1, 3, 5	100		ns
$t_{VHQV}$	$V_{CC}$ 2.7V to Output Delay	3		1	ms

NOTES:

1. A reset time,  $t_{PHQV}$ , is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for  $t_{PHQV}$ .
2.  $t_{PLPH}$  is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after  $V_{CC}$  has been in predefined range and also has been in stable there.

1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance<sup>(3)</sup>

$$V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	$V_{PP}=V_{PPH1}$ (In System)			$V_{PP}=V_{PPH2}$ (In Manufacturing)			Unit
				Min.	Typ. <sup>(1)</sup>	Max. <sup>(2)</sup>	Min.	Typ. <sup>(1)</sup>	Max. <sup>(2)</sup>	
$t_{WPB}$	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3		0.04	0.12	s
		2	Used		0.03	0.12		0.02	0.06	s
$t_{WMB}$	32K-Word Main Block Program Time	2	Not Used		0.38	2.4		0.31	1.0	s
		2	Used		0.24	1.0		0.17	0.5	s
$t_{WHQV1}/$ $t_{EHQV1}$	Word Program Time	2	Not Used		11	200		9	185	$\mu$ s
		2	Used		7	100		5	90	$\mu$ s
$t_{WHOV1}/$ $t_{EHOV1}$	OTP Program Time	2	Not Used		36	400		27	185	$\mu$ s
$t_{WHQV2}/$ $t_{EHQV2}$	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
$t_{WHQV3}/$ $t_{EHQV3}$	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
	Full Chip Erase Time	2			80	700		65	700	s
$t_{WHRH1}/$ $t_{EHRH1}$	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	$\mu$ s
$t_{WHRH2}/$ $t_{EHRH2}$	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	$\mu$ s
$t_{ERES}$	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			$\mu$ s

## NOTES:

1. Typical values measured at  $V_{CC}=3.0V$ ,  $V_{PP}=3.0V$  or  $9.5V$ , and  $T_A=+25^{\circ}C$ . Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than  $t_{ERES}$  and its sequence is repeated, the block erase operation may not be finished.

## 2 Related Document Information<sup>(1)</sup>

Document No.	Document Name
FUM00701	LH28F640BF series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.



## 3 Package and packing specification

## [Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

## 1. Storage Conditions.

## 1-1. Storage conditions required before opening the dry packing.

- Normal temperature : 5~40°C
- Normal humidity : 80%( Relative humidity) max.
- "Humidity" means "Relative humidity"

## 1-2. Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

- (1) Storage conditions for one-time soldering. (Convection reflow<sup>\*1</sup>, IR/Convection reflow.<sup>\*1</sup>, or Manual soldering. )
  - Temperature : 5~25°C
  - Humidity : 60% max.
  - Period : 72 hours max. after opening.
- (2) Storage conditions for two-time soldering. (Convection reflow<sup>\*1</sup>, IR/Convection reflow.<sup>\*1</sup>)
  - a. Storage conditions following opening and prior to performing the 1st reflow.
    - Temperature : 5~25°C
    - Humidity : 60% max.
    - Period : 72 hours max. after opening.
  - b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.
    - Temperature : 5~25°C
    - Humidity : 60% max.
    - Period : 72 hours max. after completion of the 1st reflow.

<sup>\*1</sup>: Air or nitrogen environment.

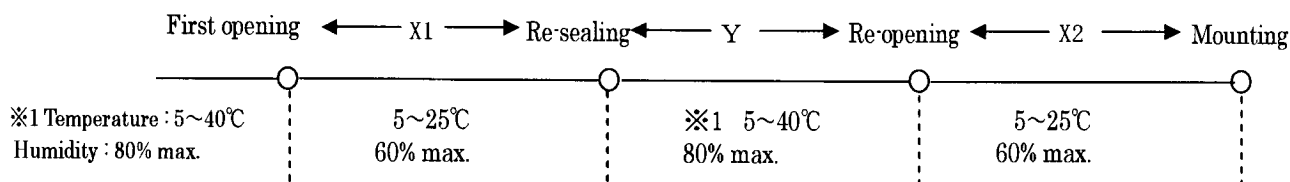
## 1-3. Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

## (1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



## (2) Storage period.

- X1 + X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

## 2. Baking Condition.

### (1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.  
( Also for re-opening.)

### (2) Recommended baking conditions.

- Baking temperature and period :  
120°C for 16~24 hours.
- The above baking conditions apply since the trays are heat-resistant.

### (3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

## 3. Surface mount conditions.

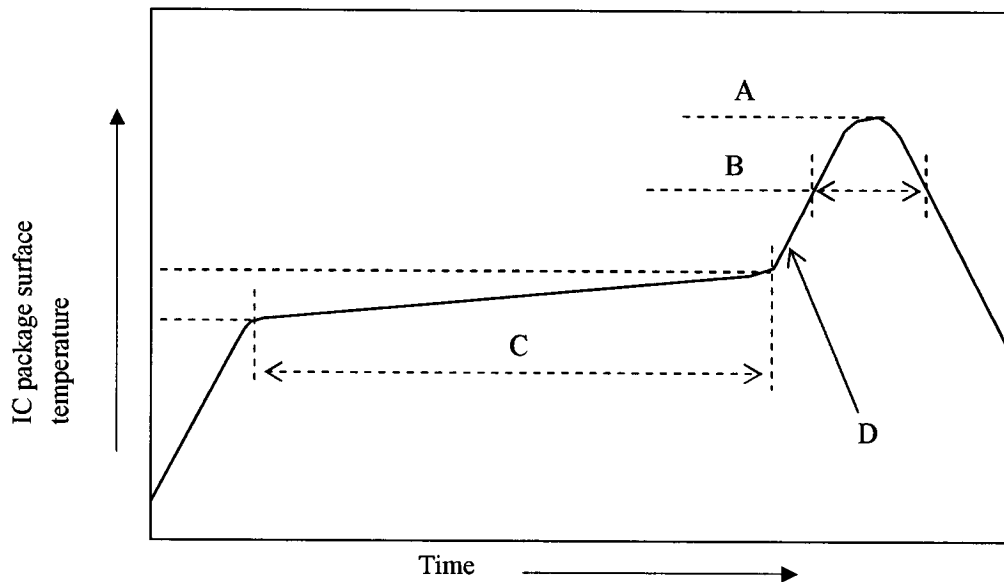
The following soldering condition are recommended to ensure device quality.

### 3-1. Soldering.

#### (1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :

A) Peak temperature.	250°C max.
B) Heating temperature.	40 to 60 seconds as 220°C
C) Preheat temperature.	It is 150 to 200°C, and is 120±30 seconds
D) Temperature increase rate.	It is 1 to 3°C/seconds
- Measuring point : IC package surface.
- Temperature profile:



(2) Manual soldering ( soldering iron ) ( one-time soldering only )

Soldering iron should only touch the IC's outer leads.

- Temperature and period :  
350°C max. for 3 seconds / pin max.  
(Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.

- (1) Ultrasonic washing power : 25 watts / liter max.
- (2) Washing time : Total 1 minute max.
- (3) Solvent temperature : 15~40°C

5. Package outline specification.

Refer to the attached drawing.

(Plastic body dimensions do not include burr of resin.)

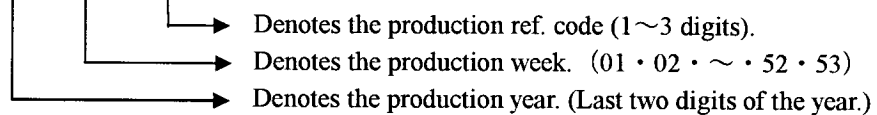
The contents of LEAD-FREE TYPE application of the specifications. (\*2)

6. Markings.

6-1. Marking details. (The information on the package should be given as follows.)

- (1) Product name : LH28F640BFHE-PBTL70A
- (2) Company name : SHARP
- (3) Date code

(Example) YY WW XXX



- (4) "JAPAN" indicates the country of origin.

6-2. Marking layout.

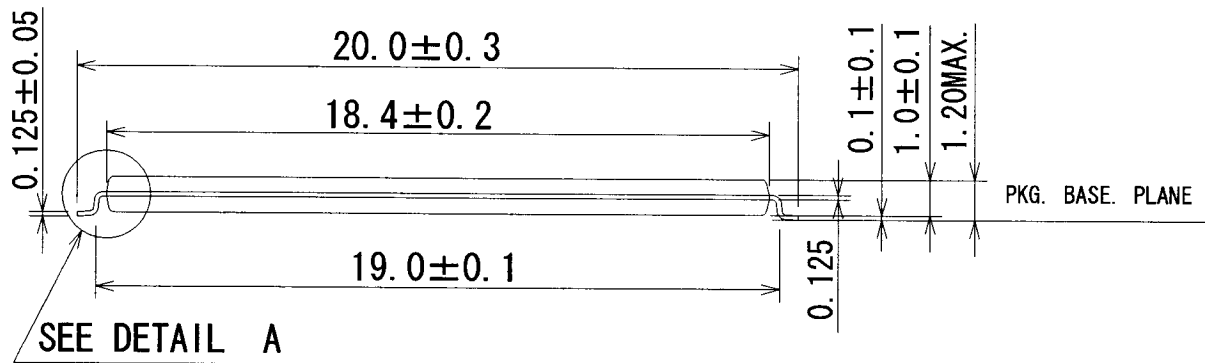
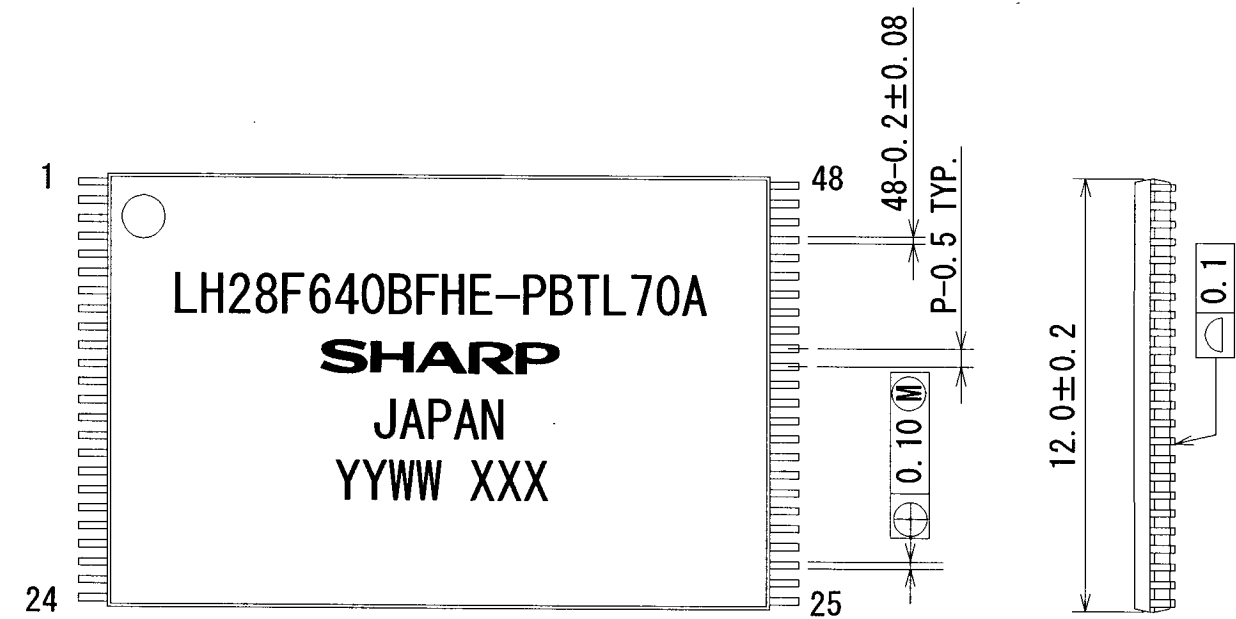
The layout is shown in the attached drawing.

(However, this layout does not specify the size of the marking character and marking position.)

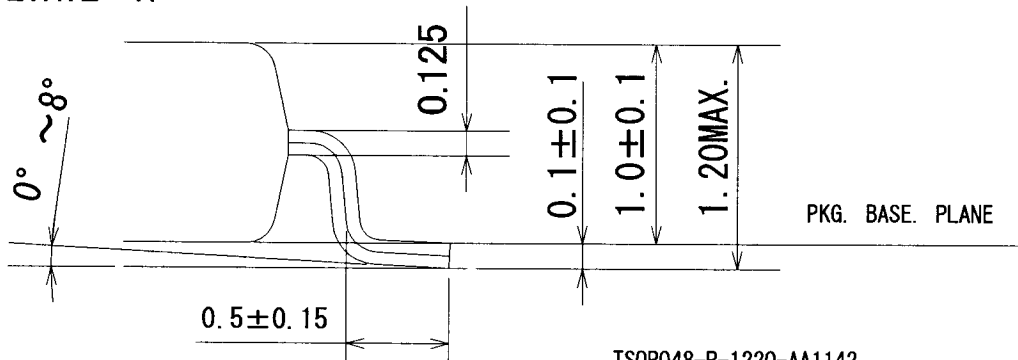
\*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline under YYWW XXX
The word of " LEAD FREE" is printed on the packing label	Printed

(Note) It is those with an underline printing in a date code because of a LEAD-FREE type.



DETAIL A



TSOP048-P-1220-AA1142

LEAD TYPE	LEAD FINISH		LEAD MATERIAL	
	Sn-Bi PLATING		42Alloy	
NAME	TSOP048-P-1220			NOTE : Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1142	UNIT	mm	

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (960 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (96 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton )	Securing the devices.
Outer carton	Cardboard (3840 devices / outer carton max.)	Outer packing.

( Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

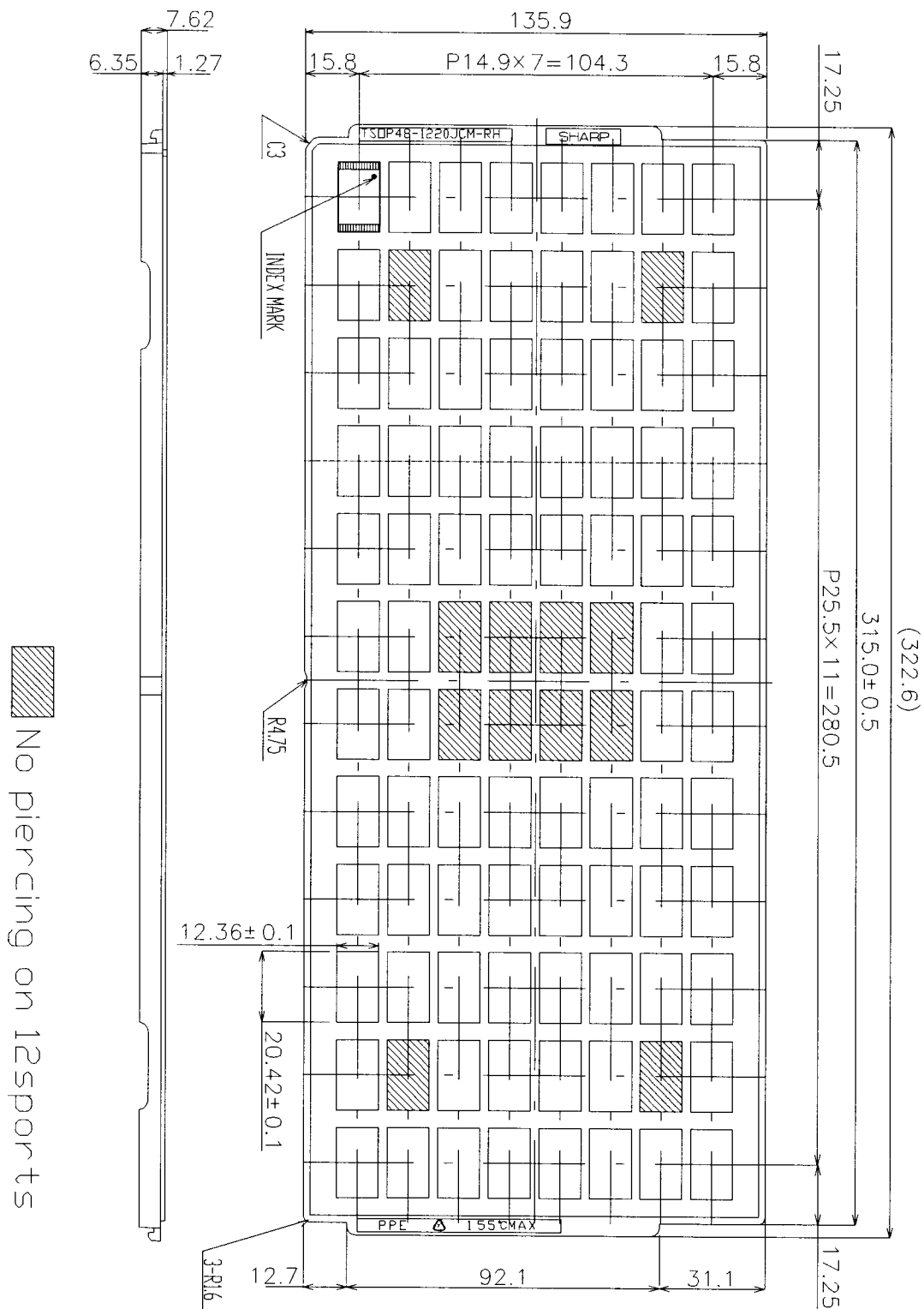
7-3.Outline dimension of carton.

Refer to the attached drawing.

TYPE-A and TYPE-B exist as a packing-case.

8. Precautions for use.

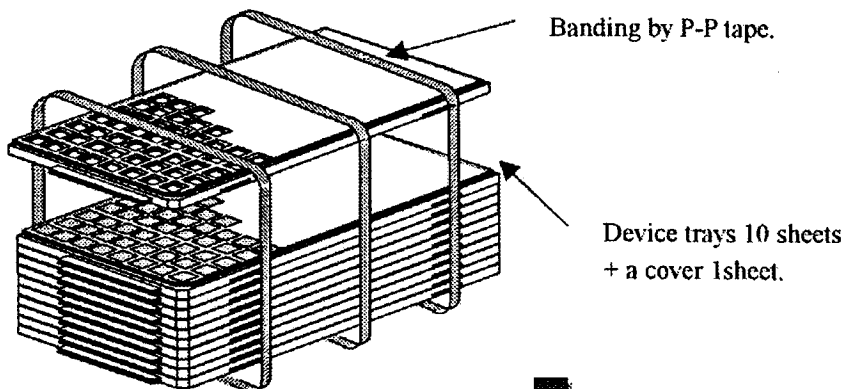
- (1) Opening must be done on an anti-ESD treated workbench.  
All workers must also have undergone anti-ESD treatment.
- (2) The trays have undergone either conductive or anti-ESD treatment.  
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.
- (3) The devices should be mounted the devices within one year of the date of delivery.



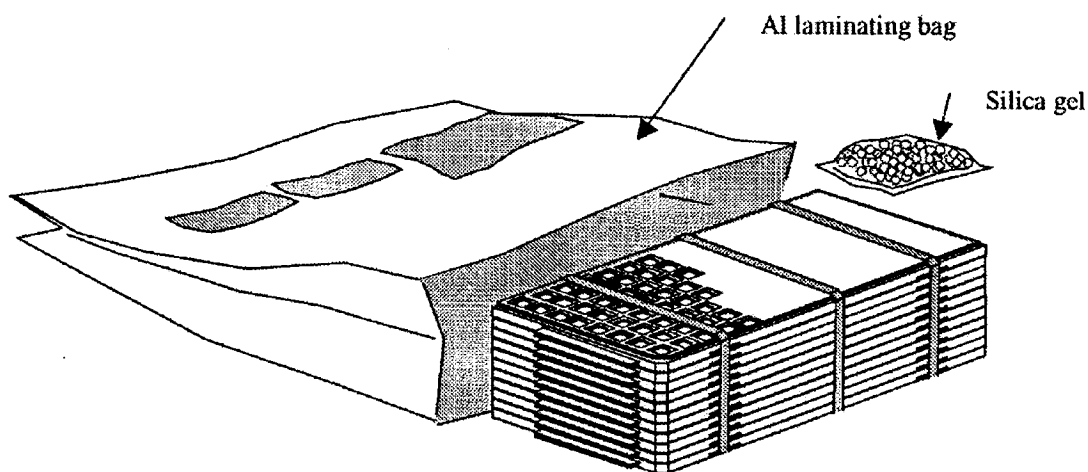
名称 NAME	TSOP48-1220JCM-RH-N		備考 NOTE
DRAWING NO.	CV911	单位 UNIT	

TYPE-A

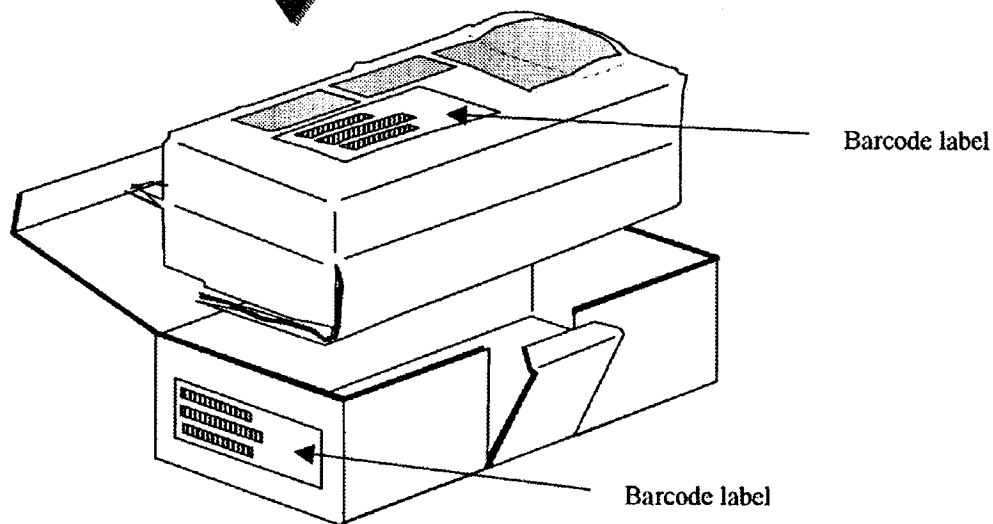
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.



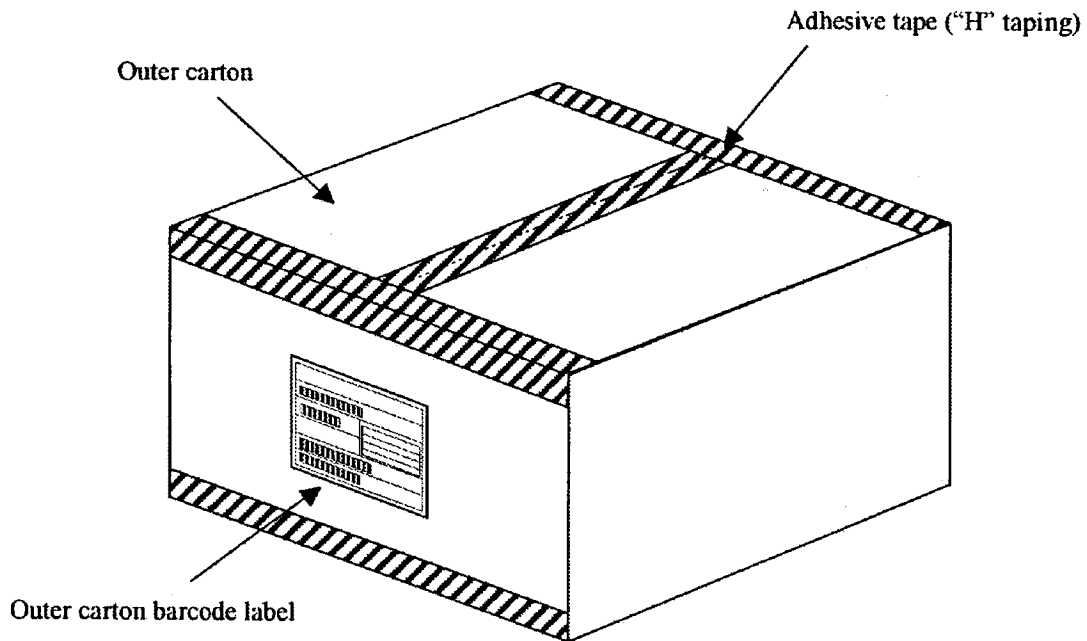
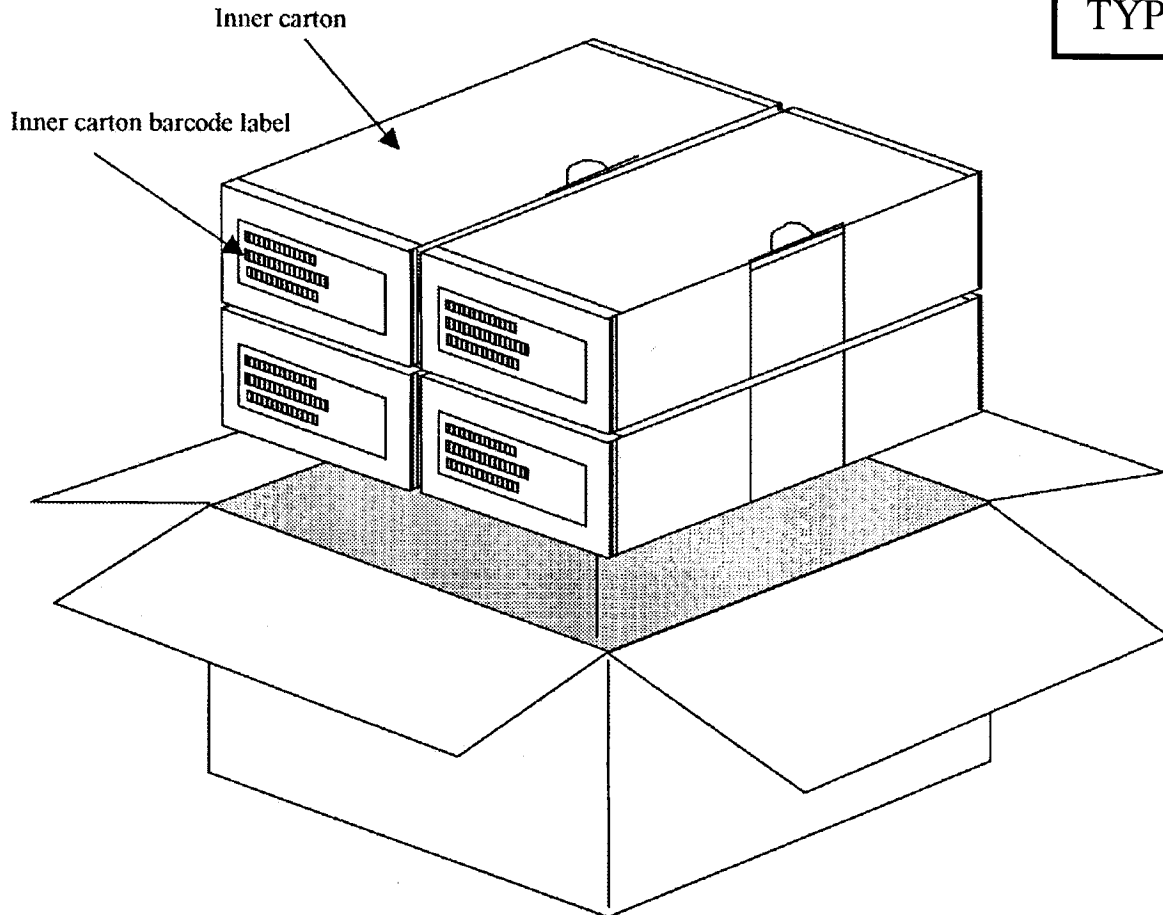
(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433a	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

TYPE-A



L × W × H

Inner carton - Outer dimensions : 335 × 150 × 80

Outer carton - Outer dimensions : 340 × 310 × 175

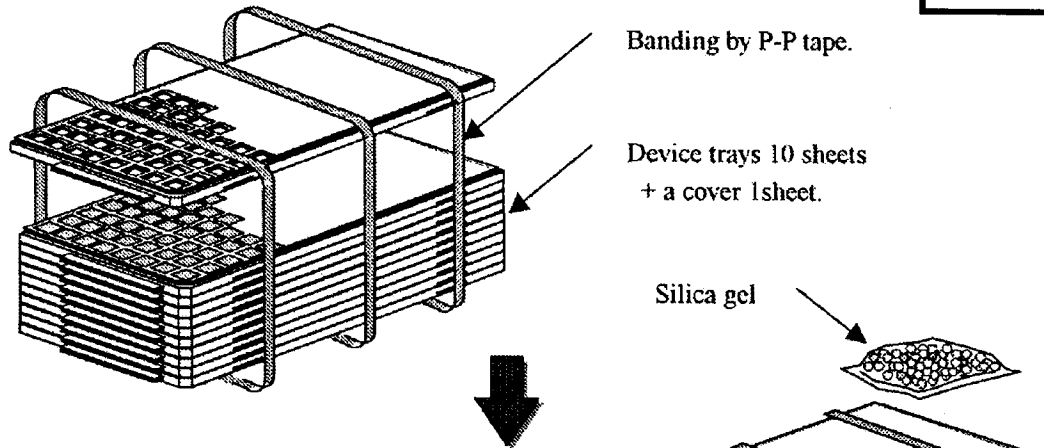
NOTE There is a possibility different from this specification when the number of shipments is fractions.

NAME	Packing specifications		
DRAWING NO.	BJ433b	UNIT	mm

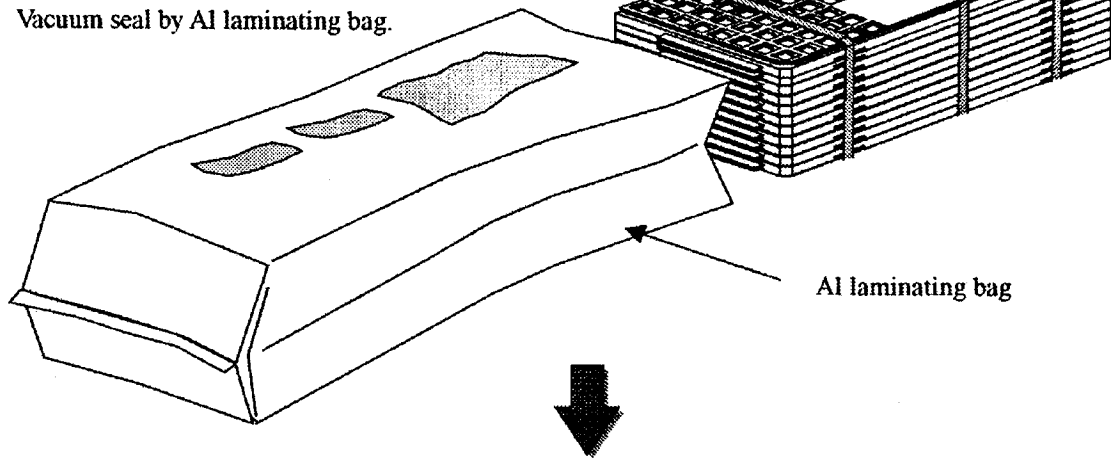


TYPE-B

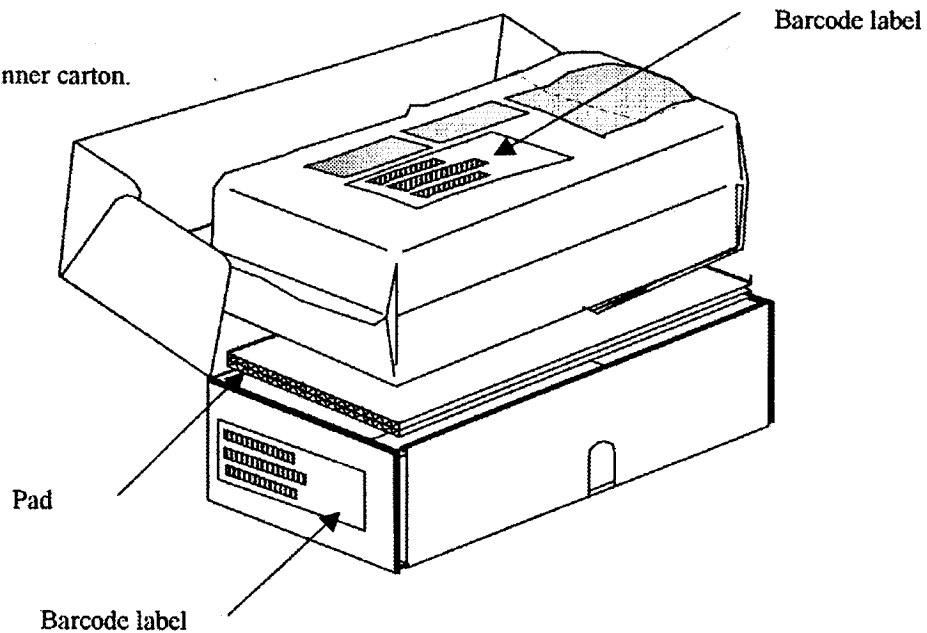
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.



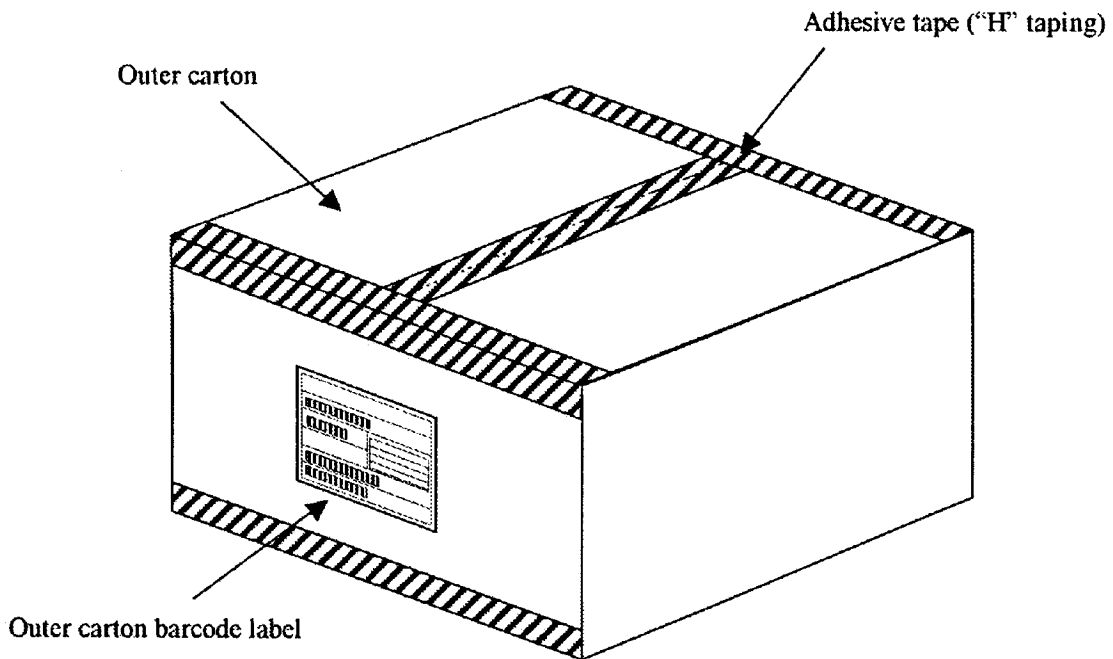
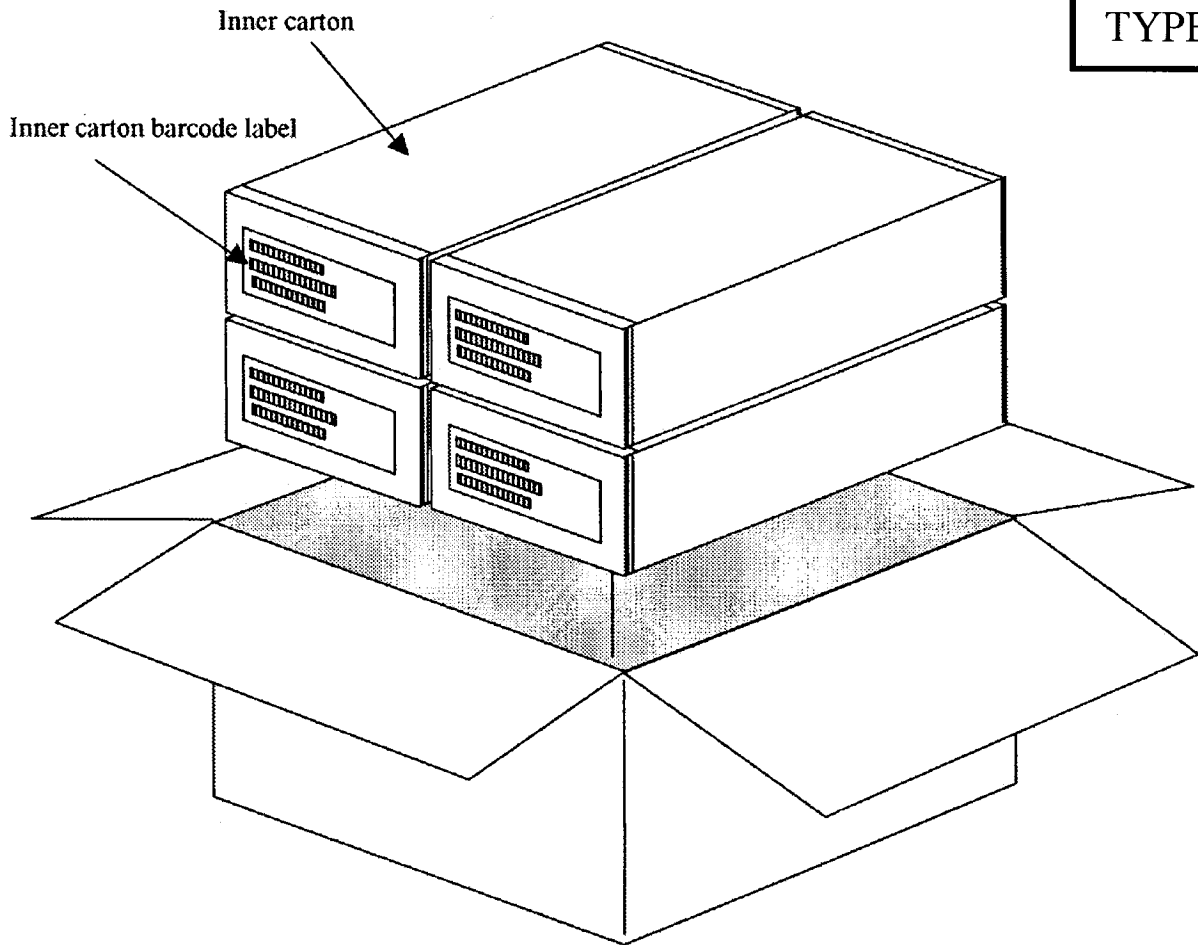
(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

TYPE-B



L × W × H

Inner carton - Outer dimensions : 335×150×85

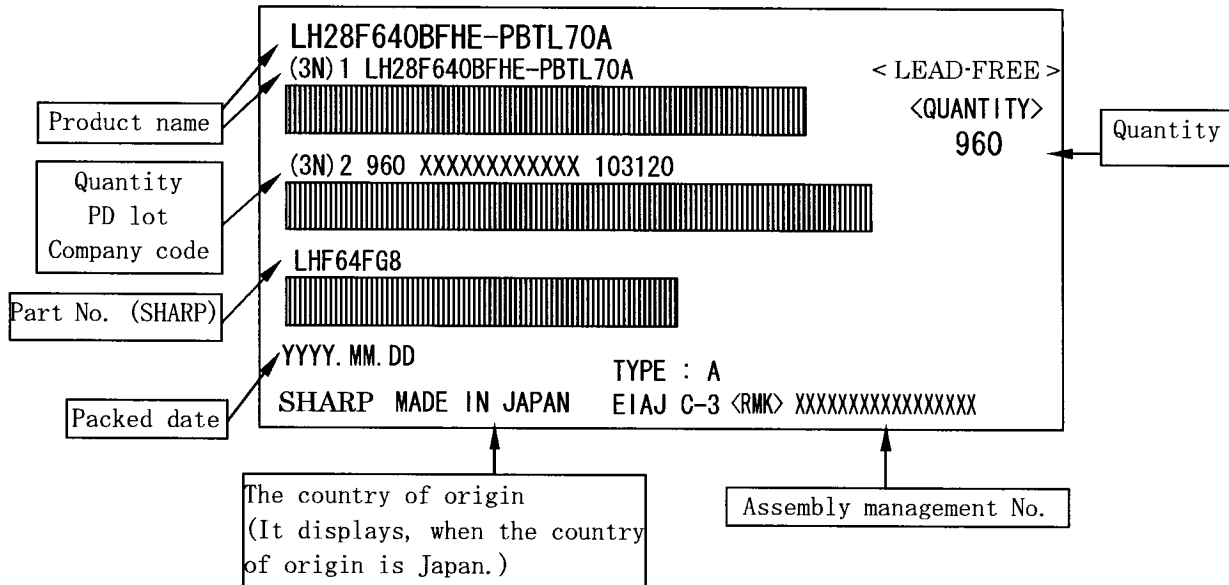
Outer carton - Outer dimensions : 360×335×220

NOTE There is a possibility different from this specification when the number of shipments is fractions.

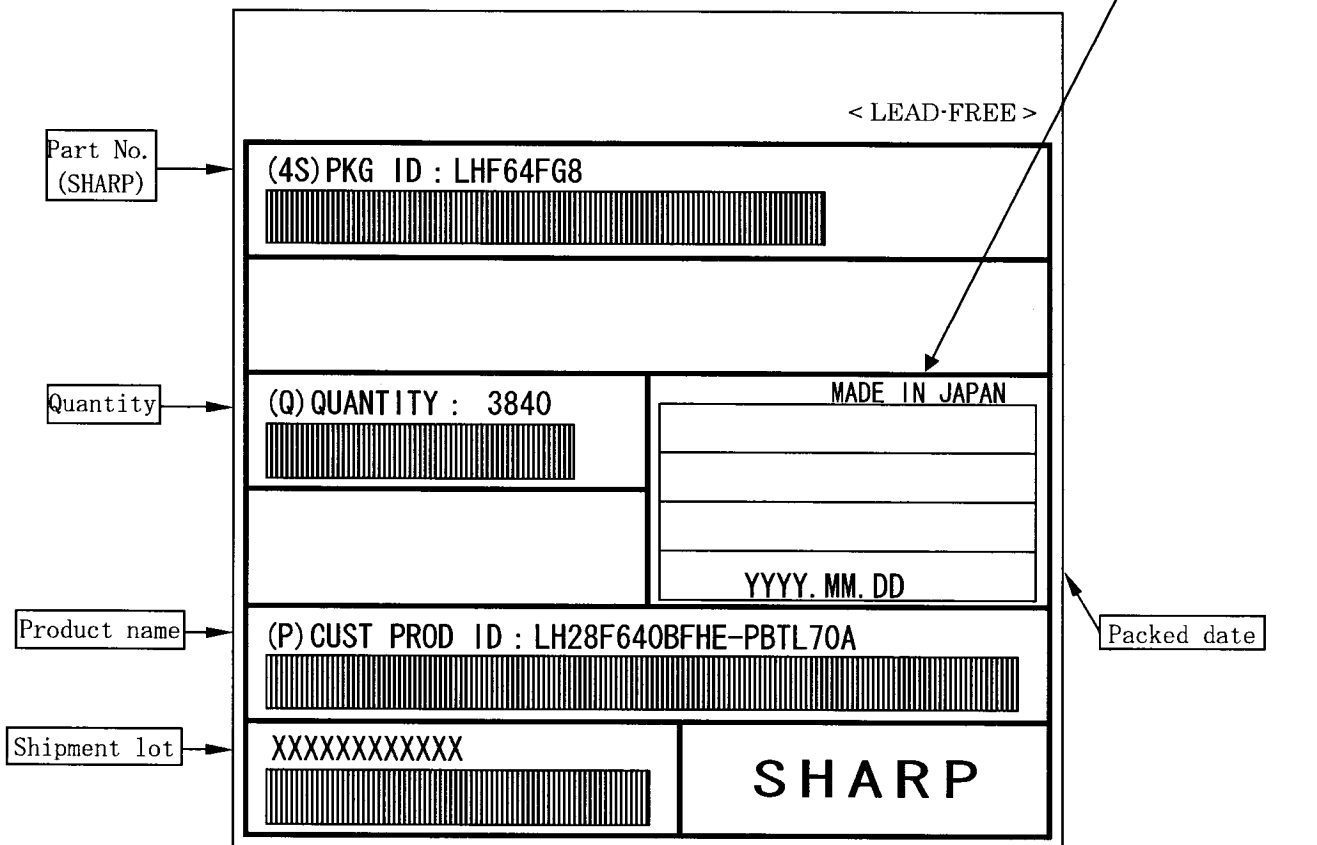
NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

(Note) The <LEAD-FREE> display shows a lead-free article.

## Inner carton label



## Outer carton label



(Former) EIAJ B Standard conforming

## LH28F640BFXX-XXXXXX Flash MEMORY ERRATA

### 1. Electrical Specifications

#### **PROBLEM**

The table below summarizes the Operating Conditions.

Electrical Specifications - Operating Conditions

Parameter	Symbol	Max.	Unit
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	3.3	V
I/O Supply Voltage	V <sub>CCQ</sub>	3.3	V
V <sub>PP</sub> Voltage when Used as a Logic Control	V <sub>PPH1</sub>	3.3	V

#### **WORKAROUND**

V<sub>CC</sub> Supply Voltage, I/O Supply Voltage and V<sub>PP</sub> Voltage when Used as a Logic Control should not be over 3.3V.

#### **STATUS**

This is intended to be fixed in future devices.

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

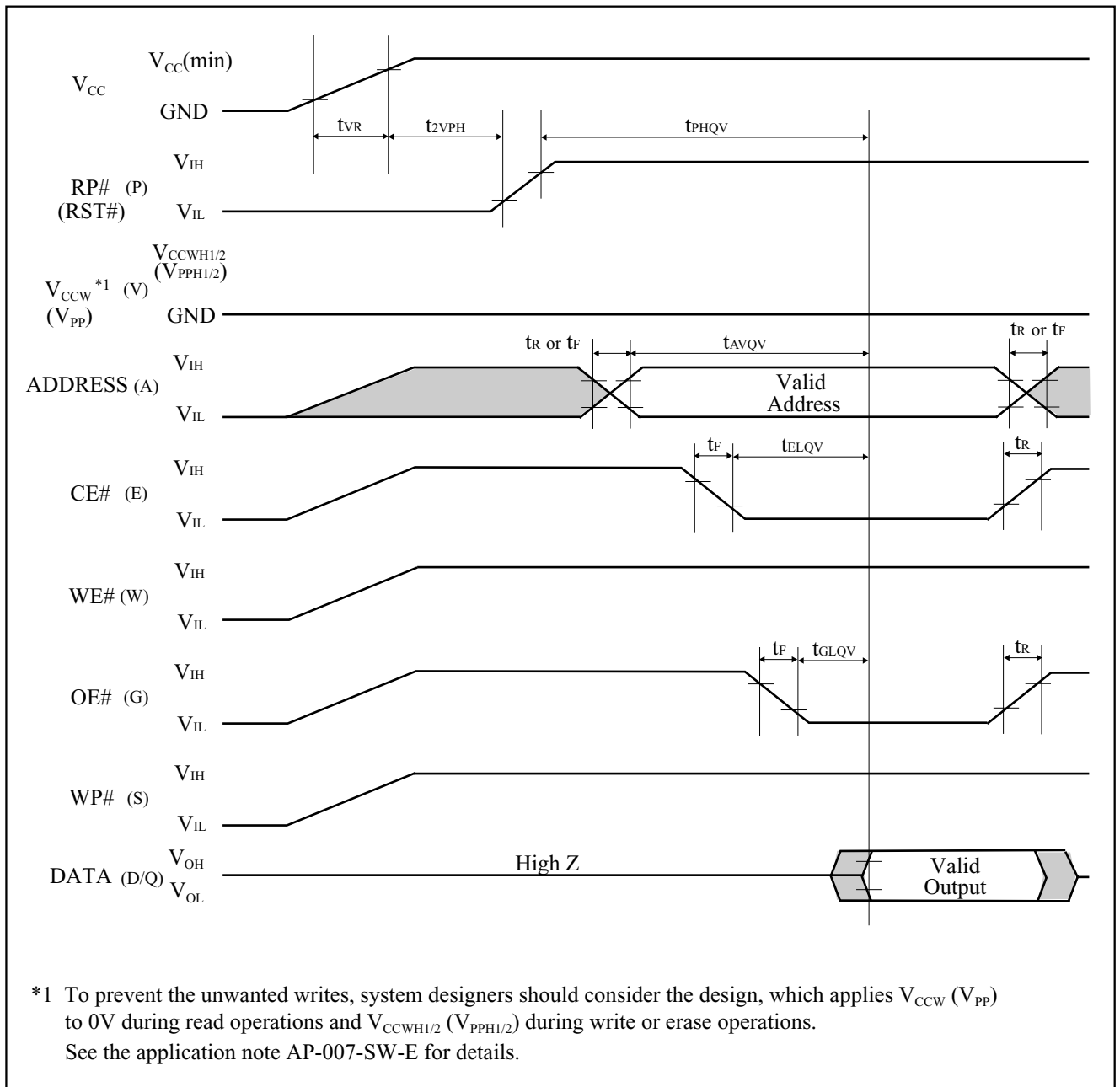


Figure A-1. AC Timing at Device Power-Up

For the AC specifications  $t_{VR}$ ,  $t_{R}$ ,  $t_{F}$  in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

## A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{VR}$	$V_{CC}$ Rise Time	1	0.5	30000	$\mu\text{s/V}$
$t_R$	Input Signal Rise Time	1, 2		1	$\mu\text{s/V}$
$t_F$	Input Signal Fall Time	1, 2		1	$\mu\text{s/V}$

### NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

## A-1.2 Glitch Noises

Do not input the glitch noises which are below  $V_{IH}$  (Min.) or above  $V_{IL}$  (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

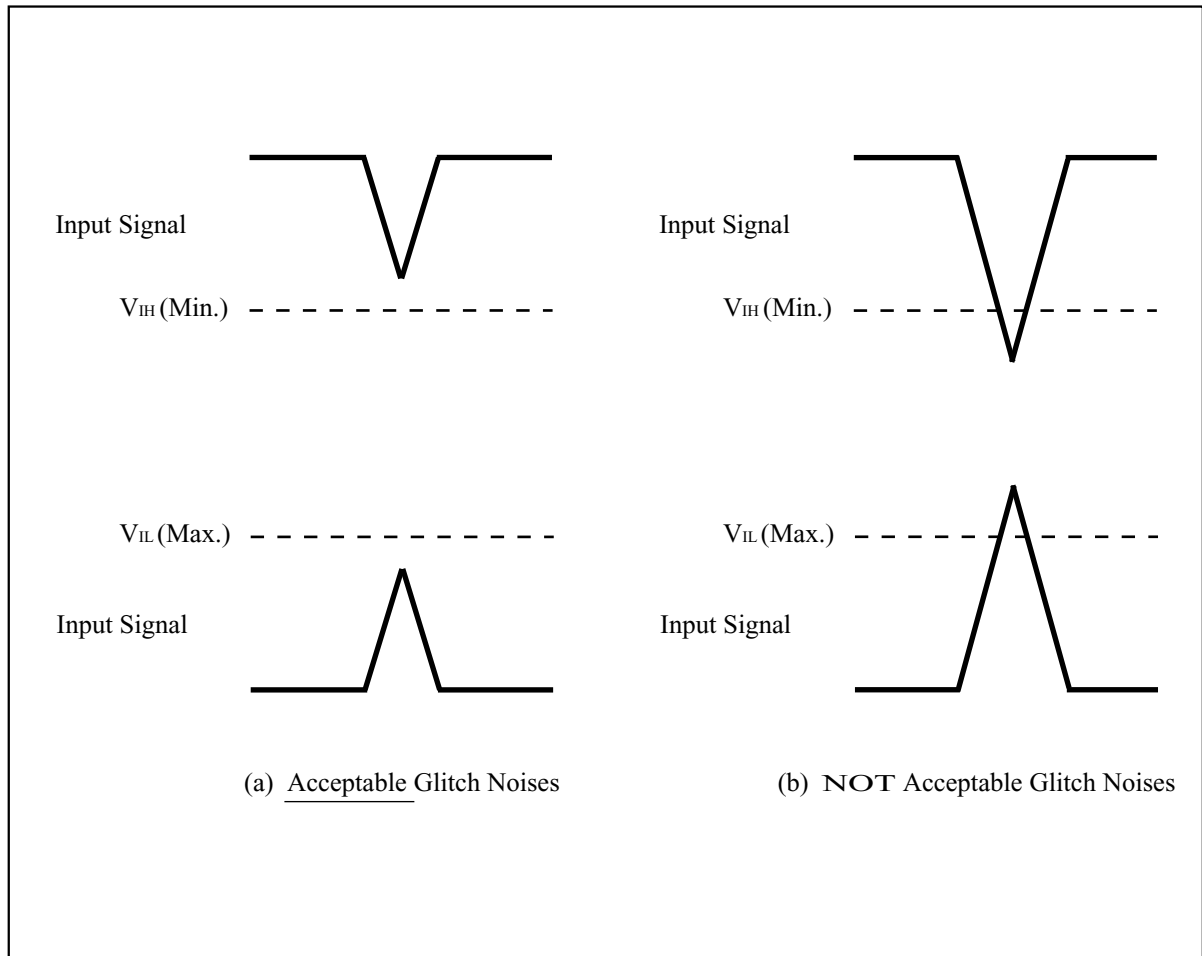


Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS” described in specifications for  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.).

## A-2 RELATED DOCUMENT INFORMATION<sup>(1)</sup>

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, $V_{PP}$ Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.



## A-3 STATUS REGISTER READ OPERATIONS

If AC timing for reading the status register described in specifications is not satisfied, a system processor can check the status register bit SR.15 instead of SR.7 to determine when the erase or program operation has been completed.

Table A-3-1. Status Register Definition (SR.15 and SR.7)

	NOTES:
<p>SR.15 = WRITE STATE MACHINE STATUS: (DQ<sub>15</sub>)</p> <p>1 = Ready in All Partitions</p> <p>0 = Busy in Any Partition</p>	<p>SR.15 indicates the status of WSM (Write State Machine). If SR.15="0", erase or program operation is in progress in any partition.</p>
<p>SR.7 = WRITE STATE MACHINE STATUS FOR EACH PARTITION: (DQ<sub>7</sub>)</p> <p>1 = Ready in the Addressed Partition</p> <p>0 = Busy in the Addressed Partition</p>	<p>SR.7 indicates the status of the partition. If SR.7="0", erase or program operation is in progress in the addressed partition. Even if the SR.7 is "1", the WSM may be occupied by the other partition.</p>

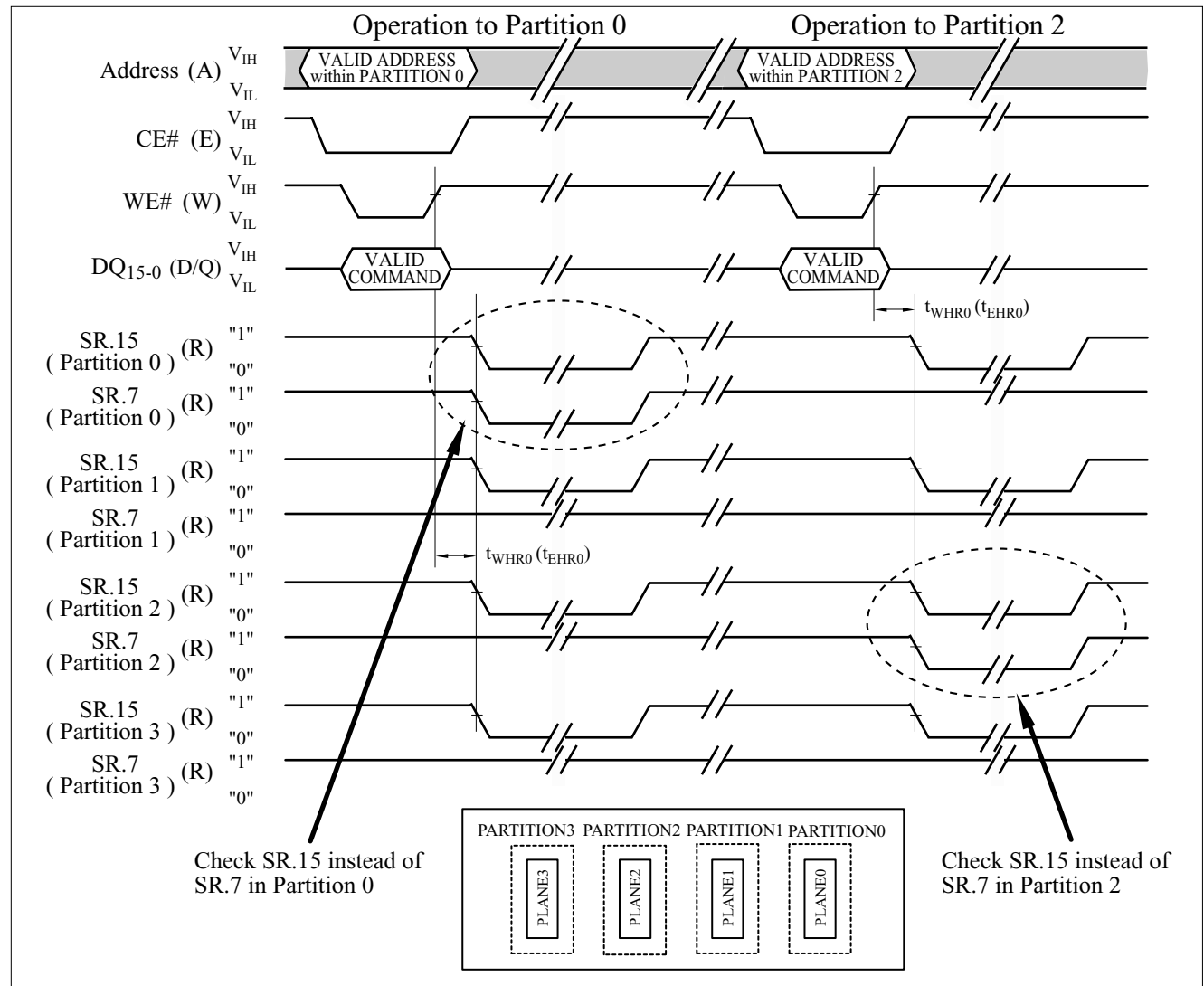


Figure A-3-1. Example of Checking the Status Register  
(In this example, the device contains four partitions.)

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