

Advanced Voltage Mode Pulse Width Modulator

FEATURES

- 700kHz Operation
- Integrated Oscillator/ Voltage Feed Forward Compensation
- Accurate Duty Cycle Limit
- Accurate Volt-second Clamp
- Optocoupler Interface
- Fault Counting Shutdown
- Fault Latch off or Automatic Shutdown
- Soft Stop Optimized for Synchronous Rectification
- 1A Peak Gate Drive Output
- 130 μ A Start-up Current
- 750 μ A Operating Current

DESCRIPTION

The UCC35701/UCC35702 family of pulse width modulators is intended for isolated switching power supplies using primary side control. They can be used for both off-line applications and DC/DC converter designs such as in a distributed power system architecture or as a telecom power source.

The devices feature low startup current, allowing for efficient off-line starting, yet have sufficient output drive to switch power MOSFETs in excess of 500kHz.

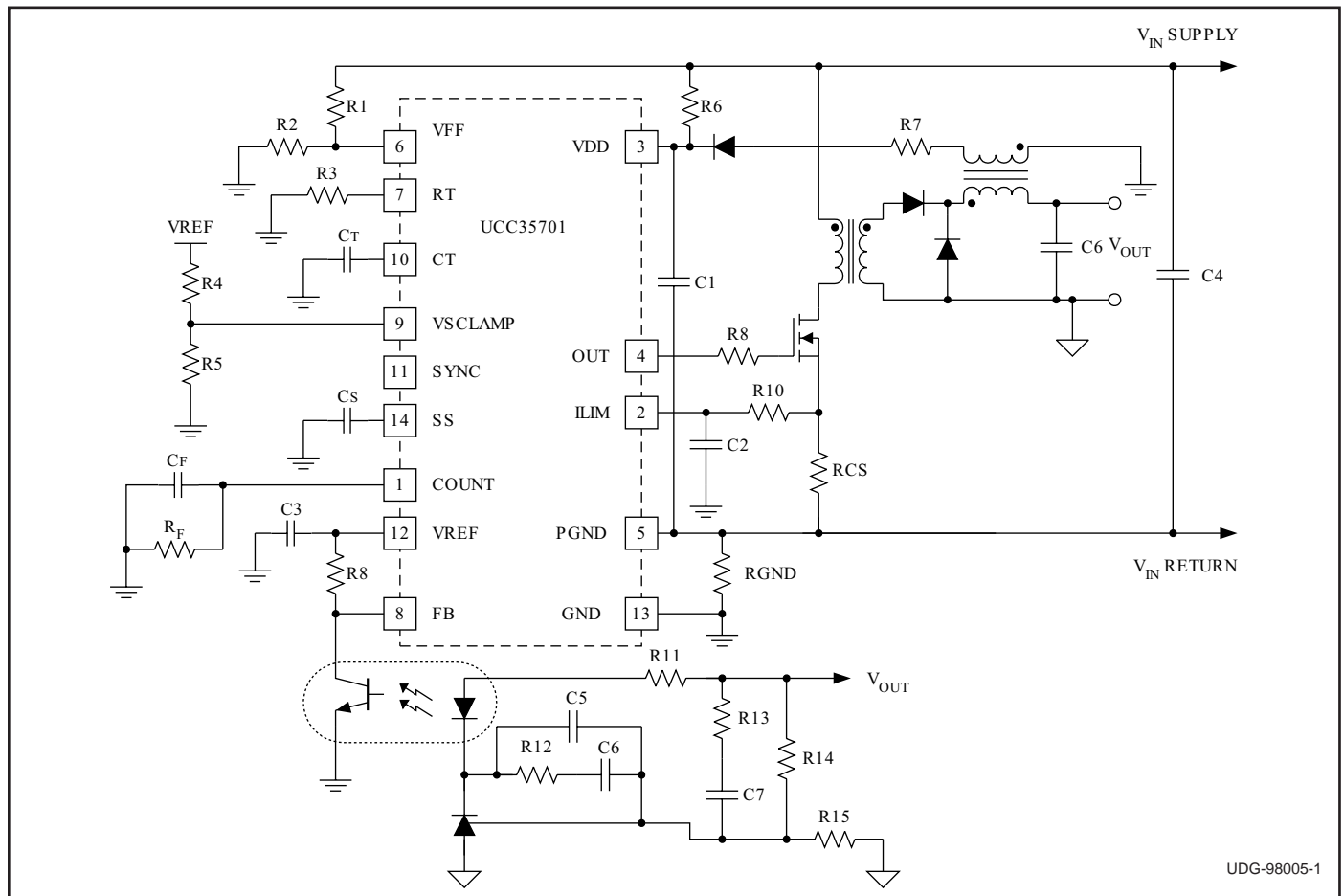
Voltage feed forward compensation is operational over a 5:1 input range and provides fast and accurate response to input voltage changes over a 4:1 range. An accurate volt-second clamp and maximum duty cycle limit are also featured.

Fault protection is provided by pulse by pulse current limiting as well as the ability to latch off after a programmable number of repetitive faults has occurred.

Two UVLO options are offered. UCC35701 family has turn-on and turn-off thresholds of 13V/9V and UCC35702 family has thresholds of 9.6V/8.8V.

The UCC35701/2 and the UCC25701/2 are offered in the 14 pin SOIC (D), 14 pin PDIP (N) or in 14 pin TSSOP (PW) packages. The UCC15701/2 is offered in the 14 pin CDIP (J) package.

TYPICAL APPLICATION DIAGRAM

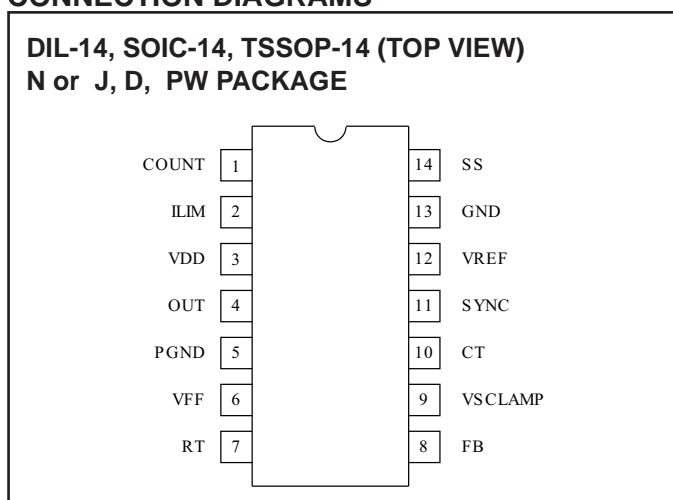


ABSOLUTE MAXIMUM RATINGS

Supply voltage (Supply current limited to 20mA) 15V
 Supply Current. 20mA
 Input pins (ILIM,VFF,RT,CT,VSCLAMP,SYNC,SS, FB) . . . 6V
 Output Current (OUT) DC. +/-180mA
 Output Current (OUT) Pulse (0.5ms) +/-1.2A
 Storage Temperature. -65°C to +150°C
 Junction Temperature. -55°C to +150°C
 Lead Temperature (Soldering, 10 sec.) +300°C

Note: All voltages are with respect to GND. Currents are positive into the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



ORDERING INFORMATION

T _A = T _J	UVLO Option	Package	Part Number
-55°C to +125°C	13V / 9V	CDIP-14	UCC15701J
	9.6V / 8.8V	CDIP-14	UCC15702J
-40°C to +85°C	13V / 9V	SOIC-14	UCC25701D
		PDIP-14	UCC25701N
		TSSOP-14	UCC25701PW
	9.6V / 8.8V	SOIC-14	UCC25702D
		PDIP-14	UCC25702N
		TSSOP-14	UCC25702PW
0°C to +70°C	13V / 9V	SOIC-14	UCC35701D
		PDIP-14	UCC35701N
		TSSOP-14	UCC35701PW
	9.6V / 8.8V	SOIC-14	UCC35702D
		PDIP-14	UCC35702N
		TSSOP-14	UCC35702PW

The D and PW packages are available taped and reeled. Add TR suffix to the device type (e.g., UCC35701DTR).

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 11V, RT = 60.4k, C_T = 330pF, C_{REF} = C_{VDD} = 0.1 F, V_{FF} = 2.0V, and no load on the outputs.

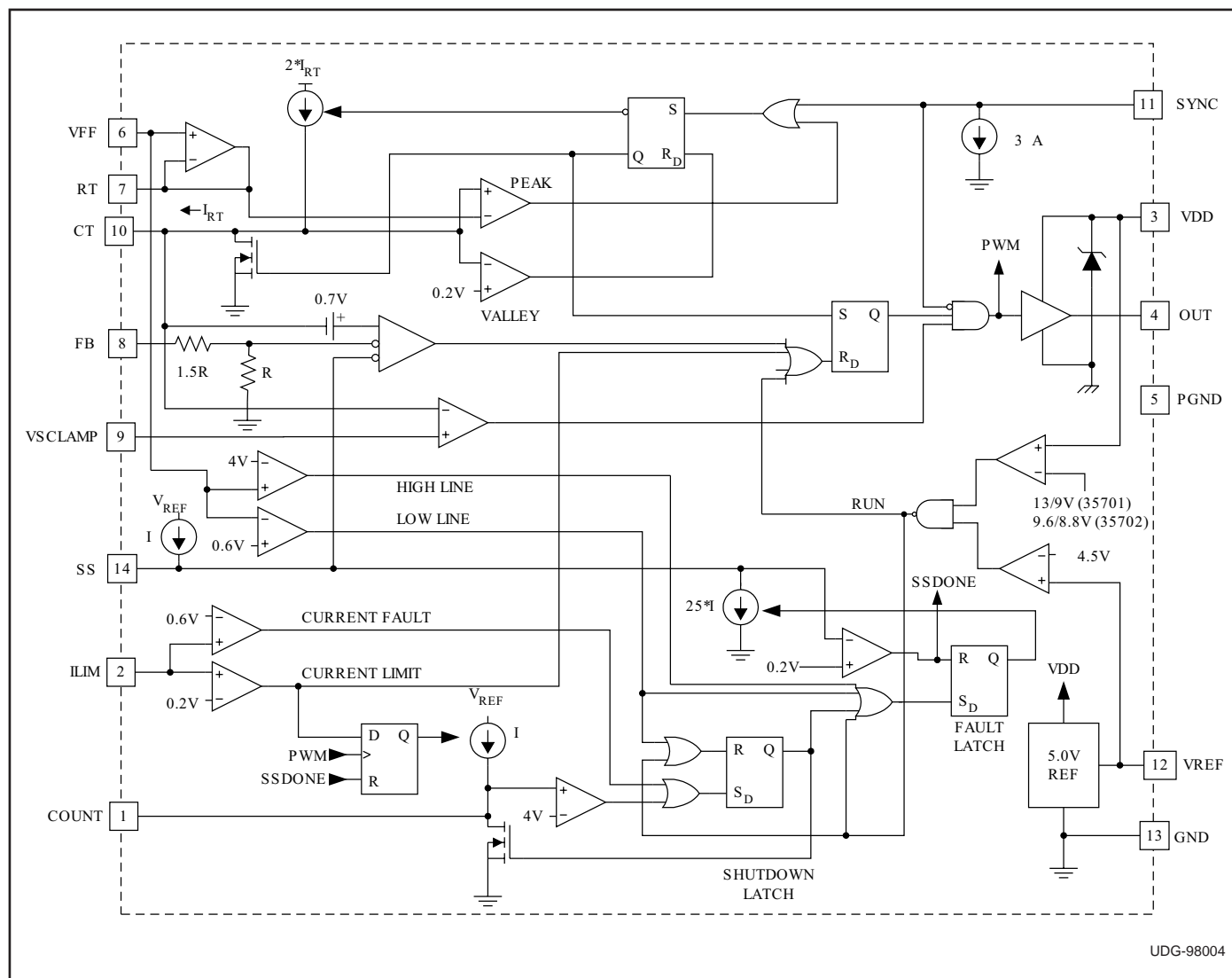
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
Start Threshold	(UCCX5701)	12	13	14	V
	(UCCX5702)	8.8	9.6	10.4	V
Stop Threshold	(UCCX5701)	8	9	10	V
	(UCCX5702)	8.0	8.8	9.6	V
Hysteresis	(UCCX5701)	3	4		V
	(UCCX5702)	0.3	0.8		V
Supply Current					
Start-up Current	(UCCX5701) V _{DD} = 11V, V _{DD} Comparator Off		130	200	μA
	(UCCX5702) V _{DD} = 8V, V _{DD} Comparator Off		120	190	μA
I _{DD} Active	V _{DD} Comparator On		0.75	1.5	mA
V _{DD} Clamp Voltage	(UCCX5701) I _{DD} = 10mA	13.5	14.3	15	V
	(UCCX5702) I _{DD} = 10mA	13	13.8	15	V
V _{DD} Clamp – Start Threshold	(UCCX5701)		1.3		V
	(UCCX5702)		4.2		V
Voltage Reference					
V _{REF}	V _{DD} = 10V to 13V, I _{VREF} = 0mA to 2mA	4.9	5	5.1	V
Line Regulation	V _{DD} = 10V to 13V		20		mV
Load Regulation	I _{VREF} = 0mA to 2mA		2		mV
Short Circuit Current	V _{REF} = 0V, T _J = 25°C		20	50	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, $V_{DD} = 11V$, $R_T = 60.4k$, $C_T = 330pF$, $C_{REF} = C_{VDD} = 0.1 F$, $V_{FF} = 2.0V$, and no load on the outputs.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Sense					
V _{th} High Line Comparator		3.9	4	4.1	V
V _{th} Low Line Comparator		0.5	0.6	0.7	V
Input Bias Current		-100		100	nA
Oscillator Section					
Frequency	$V_{FF} = 0.8V$ to $3.2V$	90	100	110	kHz
Frequency	$V_{FF} = 0.6V$ to $3.4V$ (Note 1)	90	100	110	kHz
SYNC VIH		2			V
SYNC VIL				0.8	V
SYNC Input Current	$V_{SYNC} = 2.0V$		3	10	μA
RT Voltage	$V_{FF} = 0.4V$	0.5	0.6	0.7	V
	$V_{FF} = 0.8V$	0.75	0.8	0.85	V
	$V_{FF} = 2.0V$	1.95	2.0	2.05	V
	$V_{FF} = 3.2V$	3.15	3.2	3.25	V
	$V_{FF} = 3.6V$	3.3	3.4	3.5	V
C _T Peak Voltage	$V_{FF} = 0.8V$ (Note 1)		0.8		V
	$V_{FF} = 3.2V$ (Note 1)		3.2		V
C _T Valley Voltage	(Note 1)		0		V
Soft Start/Shutdown/Duty Cycle Control Section					
I _{SS} Charging Current		10	18	30	μA
I _{SS} Discharging Current		300	500	750	μA
Saturation	$V_{DD} = 11V$, IC Off		25	100	mV
Fault Counter Section					
Threshold Voltage	$V_{FF} = 0.8V$ to $3.2V$	3.8	4	4.2	V
Saturation Voltage	$V_{FF} = 0.8V$ to $3.2V$			100	mV
Count Charging Current		10	18	30	μA
Current Limit Section					
Input Bias Current		-100	0	100	nA
Current Limit Threshold		180	200	220	mV
Shutdown Threshold		500	600	700	mV
Pulse Width Modulator Section					
FB Pin Input Impedance	$V_{FB} = 3V$	30	50	100	k Ω
Minimum Duty Cycle	$V_{FB} \leq 1V$			0	%
Maximum Duty Cycle	$V_{FB} \geq 4.5V$, $V_{SCLAMP} \geq 2.0V$	95	99	100	%
PWM Gain	$V_{FF} = 0.8V$	35	50	70	%/V
Volt Second Clamp Section					
Maximum Duty Cycle	$V_{FF} = 0.8V$, $V_{SCLAMP} = 0.6V$	69	74	79	%
Minimum Duty Cycle	$V_{FF} = 3.2V$, $V_{SCLAMP} = 0.6V$	17	19	21	%
Output Section					
VOH	$I_{OUT} = -100mA$, ($V_{DD} - V_{OUT}$)		0.4	1	V
VOL	$I_{OUT} = 100mA$		0.4	1	V
Rise Time	$C_{LOAD} = 1000pF$		20	100	ns
Fall Time	$C_{LOAD} = 1000pF$		20	100	ns

Note 1: Ensured by design. Not 100% tested in production.

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

VDD: Power supply pin. A shunt regulator limits supply voltage to 14V typical at 10mA shunt current.

PGND: Power Ground. Ground return for output driver and currents.

GND: Analog Ground. Ground return for all other circuits. This pin must be connected directly to PGND on the board.

OUT: Gate drive output. Output resistance is 10Ω maximum.

VFF: Voltage feedforward pin. This pin connects to the power supply input voltage through a resistive divider and provides feedforward compensation over a 0.8V to 3.2V range. A voltage greater than 4.0V or less than 0.6V on this pin initiates a soft stop cycle.

RT: The voltage on this pin mirrors VFF over a 0.8V to 3.2V range. A resistor to ground sets the ramp capacitor charge current. The resistor value should be between 20k and 200k.

CT: A capacitor to ground provides the oscillator/feedforward sawtooth waveform. Charge current is $2 \cdot I_{RT}$, resulting in a CT slope proportional to the input voltage. The ramp voltage range is GND to V_{RT} .

Period and oscillator frequency is given by:

$$T = \frac{V_{RT} \cdot C_T}{2 \cdot I_{RT}} + t_{DISCH} \approx 0.5 \cdot R_T \cdot C_T$$

$$F \approx \frac{2}{R_T \cdot C_T}$$

PIN DESCRIPTIONS (cont.)

VSCLAMP: Voltage at this pin is compared to the CT voltage, providing a constant volt-second limit. The comparator output terminates the PWM pulse when the ramp voltage exceeds VSCLAMP. The maximum on time is given by:

$$t_{ON} = \frac{V_{VSCLAMP} \cdot CT}{2 \cdot I_{RT}}$$

The maximum duty cycle limit is given by:

$$D_{MAX} = \frac{t_{ON}}{T} = \frac{V_{VSCLAMP}}{V_{RT}}$$

FB: Input to the PWM comparator. This pin is intended to be driven with an optocoupler circuit. Input impedance is 50kΩ. Typical modulation range is 1.6V to 3.6V.

SYNC: Level sensitive oscillator sync input. A high level forces the gate drive output low and resets the ramp capacitor. On-time starts at the negative edge the pulse. There is a 3μA pull down current on the pin, allowing it to be disconnected when not used.

VREF: 5.0V trimmed reference with 2% variation over line, load and temperature. Bypass with a minimum of 0.1μF to ground.

SS: Soft Start pin. A capacitor is connected between this pin and ground to set the start up time of the converter. After power up ($V_{DD} > 13V$ AND $V_{REF} > 4.5V$), or after a fault condition has been cleared, the soft start capacitor is charged to V_{REF} by a nominal 18μA internal current

source. While the soft start capacitor is charging, and while $V_{SS} < (0.4 \cdot V_{FB})$, the duty cycle, and therefore the output voltage of the converter is determined by the soft start circuitry.

At High Line or Low Line fault conditions, the soft start capacitor is discharged with a controlled discharge current of about 500μA. During the discharge time, the duty cycle of the converter is gradually decreased to zero. This soft stop feature allows the synchronous rectifiers to gradually discharge the output LC filter. An abrupt shut off can cause the LC filter to oscillate, producing unpredictable output voltage levels.

All other fault conditions (UVLO, VREF Low, Over Current (0.6V on ILIM) or COUNT) will cause an immediate stop of the converter. Furthermore, both the Over Current fault and the COUNT fault will be internally latched until V_{DD} drops below 9V or V_{FF} goes below the 600mV threshold at the input of the Low Line comparator.

After all fault conditions are cleared and the soft start capacitor is discharged below 200 mV, a soft start cycle will be initiated to restart the converter.

ILIM: Provides a pulse by pulse current limit by terminating the PWM pulse when the input is above 200mV. An input over 600mV initiates a latched soft stop cycle.

COUNT: Capacitor to ground integrates current pulses generated when ILIM exceeds 200mV. A resistor to ground sets the discharge time constant. A voltage over 4V will initiate a latched soft stop cycle.

APPLICATION INFORMATION

(Note: Refer to the Typical Application Diagram on the first page of this datasheet for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.

Power Sequencing

V_{DD} is normally connected through a high impedance (R6) to the input line, with an additional path (R7) to a low voltage bootstrap winding on the power transformer. V_{FF} is connected through a divider (R1/R2) to the input line.

For circuit activation, all of the following conditions are required:

1. V_{FF} between 0.6V and 4.0V (operational input voltage range).
2. V_{DD} has been under the UVLO stop threshold to reset the shutdown latch.
3. V_{DD} is over the UVLO start threshold.

The circuit will start at this point. I_{VDD} will increase from the start up value of 130μA to the run value of 750μA. The capacitor on SS is charged with a 18μA current. When the voltage on SS is greater than 0.8V, output pulses can begin, and supply current will increase to a level determined by the MOSFET gate charge requirements to $I_{VDD} \sim 1mA + QT \cdot fs$. When the output is active, the bootstrap winding should be sourcing the supply current. If V_{DD} falls below the UVLO stop threshold, the controller will enter a shutdown sequence and turn the controller off, returning the start sequence to the initial condition.

VDD Clamp

An internal shunt regulator clamps V_{DD} so the voltage does not exceed a nominal value of 14V. If the regulator is active, supply current must be limited to less than 20mA.

APPLICATION INFORMATION (cont.)

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and is driven low by voltages on CT, FB or VSCLAMP.

The following conditions cause the output to be immediately driven low until a clock period starts where none of the conditions are true:

1. $I_{LIM} > 0.2V$
2. FB or SS is less than 0.8V

Current Limiting

ILIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse over-current control for excessive loads. This comparator also causes C_F to be charged for the remainder of the clock cycle.

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than $(4 \cdot R_4) \cdot (1 - D_{MAX})$.

Latched Shutdown

If ILIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SS and COUNT, and reduce I_{DD} to approximately 750 μ A. When, and if, V_{DD} falls below the UVLO stop threshold, the shutdown latch will reset and I_{DD} will fall to 130 μ A, allowing the circuit to restart. If V_{DD} remains above the UVLO stop threshold (within the UVLO band), an alternate restart will occur if VFF is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or ILIM pins.

Voltage Feedforward

The voltage slope on CT is proportional to line voltage over a 4:1 range and equals $2 \cdot V_{FF} (R_T \cdot C_T)$. The capacitor charging current is set by the voltage across R_T . $V(R_T)$ tracks VFF over a range of 0.8V to 3.2V. A changing line voltage will immediately change the slope of $V(CT)$, changing the pulse width in a proportional manner without using the feedback loop, providing excellent dynamic line regulation.

VFF is intended to operate accurately over a 4:1 range between 0.8V and 3.2V. Voltages at VFF below 0.6V or above 4.0V will initiate a soft stop cycle and a chip restart when the under/over voltage condition is removed.

Volt-Second Clamp

A constant volt-second clamp is formed by comparing the timing capacitor ramp voltage to a fixed voltage derived from the reference. Resistors R_4 and R_5 set the volt-second limit. For a volt-second product defined as $V_{IN} t_{ON(max)}$, the required voltage at VSCLAMP is:

$$\frac{\left(\frac{R_2}{R_1 + R_2}\right) \cdot (V_{IN} \cdot t_{ON(max)})}{R_T \cdot C_T}$$

The duty cycle limit is then:

$$\frac{V_{VSCLAMP}}{V_{VFF}}, \text{ or } \frac{V_{VSCLAMP}}{V_{IN} \cdot \left(\frac{R_2}{R_1 + R_2}\right)}$$

The maximum duty cycle is realized when the feedforward voltage is set at the low end of the operating range ($V_{FF} = 0.8V$).

The absolute maximum duty cycle is:

$$D_{MAX} = \frac{V_{VSCLAMP}}{0.8} = \frac{V_{REF}}{0.8} \cdot \frac{R_5}{R_4 + R_5}$$

Frequency Set

The frequency is set by a resistor from R_T to ground and a capacitor from C_T to ground. The frequency is approximately: $F = \frac{2}{(R_T \cdot C_T)}$

External synchronization is via the SYNC pin. The pin has a 1.5V threshold, making it compatible with 5V and 3.3V CMOS logic. The input is level sensitive, with a high input forcing the oscillator ramp low and the output low. An active pull down on the SYNC pin allows it to be unconnected when not used.

Gate Drive Output

The UCC35701/2 is capable of a 1A peak output current. Bypass with at least 0.1 μ F directly to PGND. The capacitor must have a low equivalent series resistance and inductance. The connection from OUT to the power MOSFET gate should have a 2 Ω or greater damping resistor and the distance between chip and MOSFET should be minimized. A low impedance path must be established between the MOSFET source (or ground side of the current sense resistor), the V_{DD} capacitor and PGND. PGND should then be connected by a single path (shown as RGND) to GND.

TYPICAL WAVEFORMS (cont.)

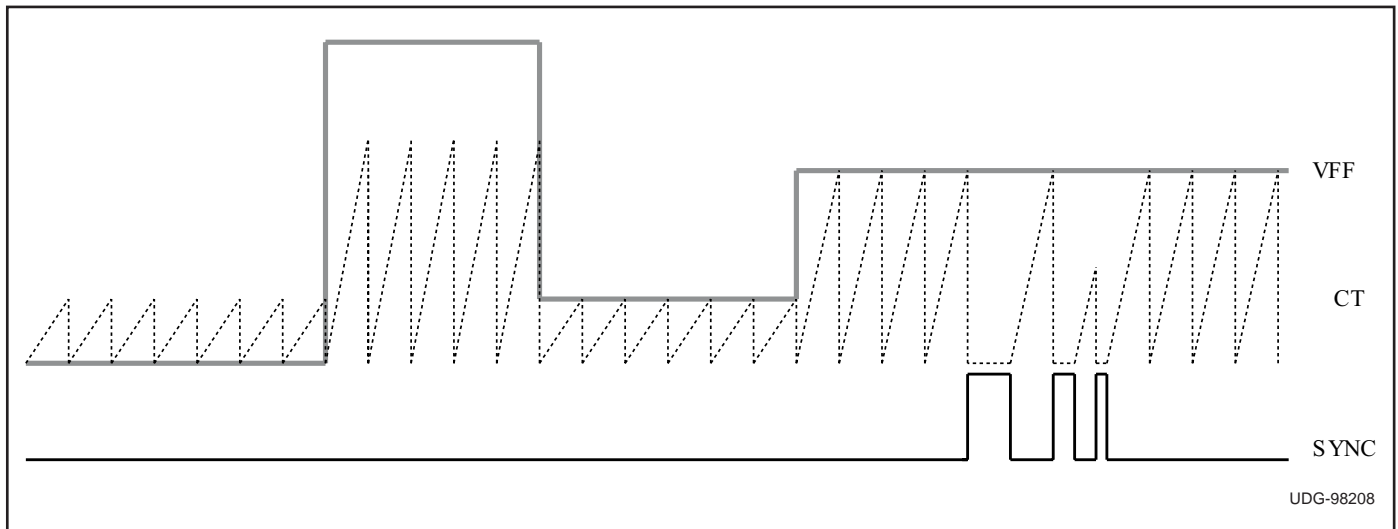


Figure 2. Timing diagram for oscillator waveforms showing feedforward action and synchronization.

TYPICAL CHARACTERISTIC CURVES

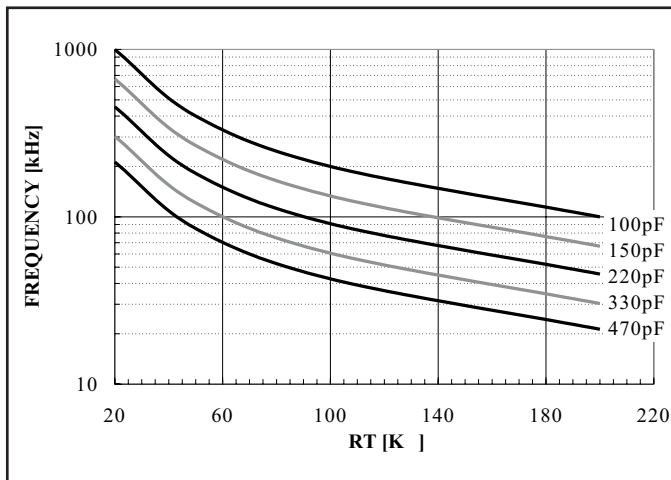


Figure 3. Oscillator frequency vs. RT and CT.

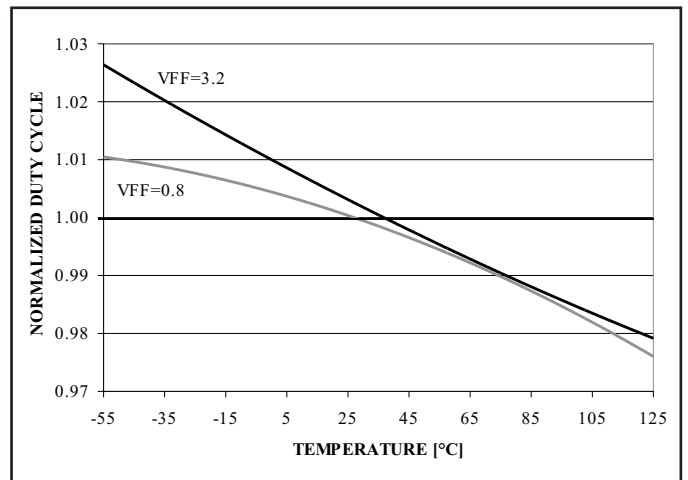


Figure 5. Normalized maximum duty cycle vs. temperature.

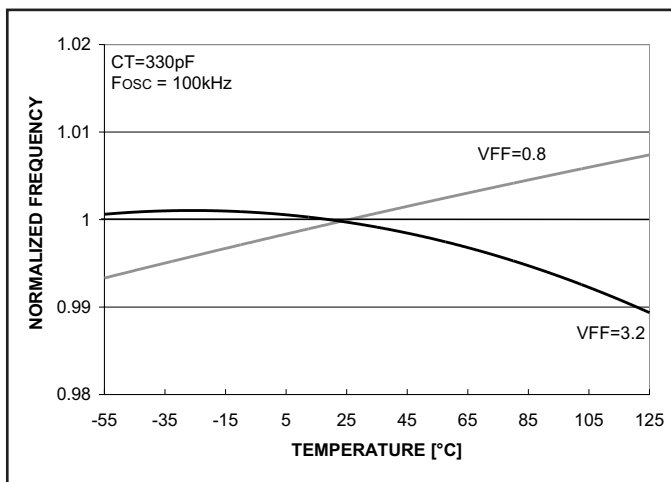
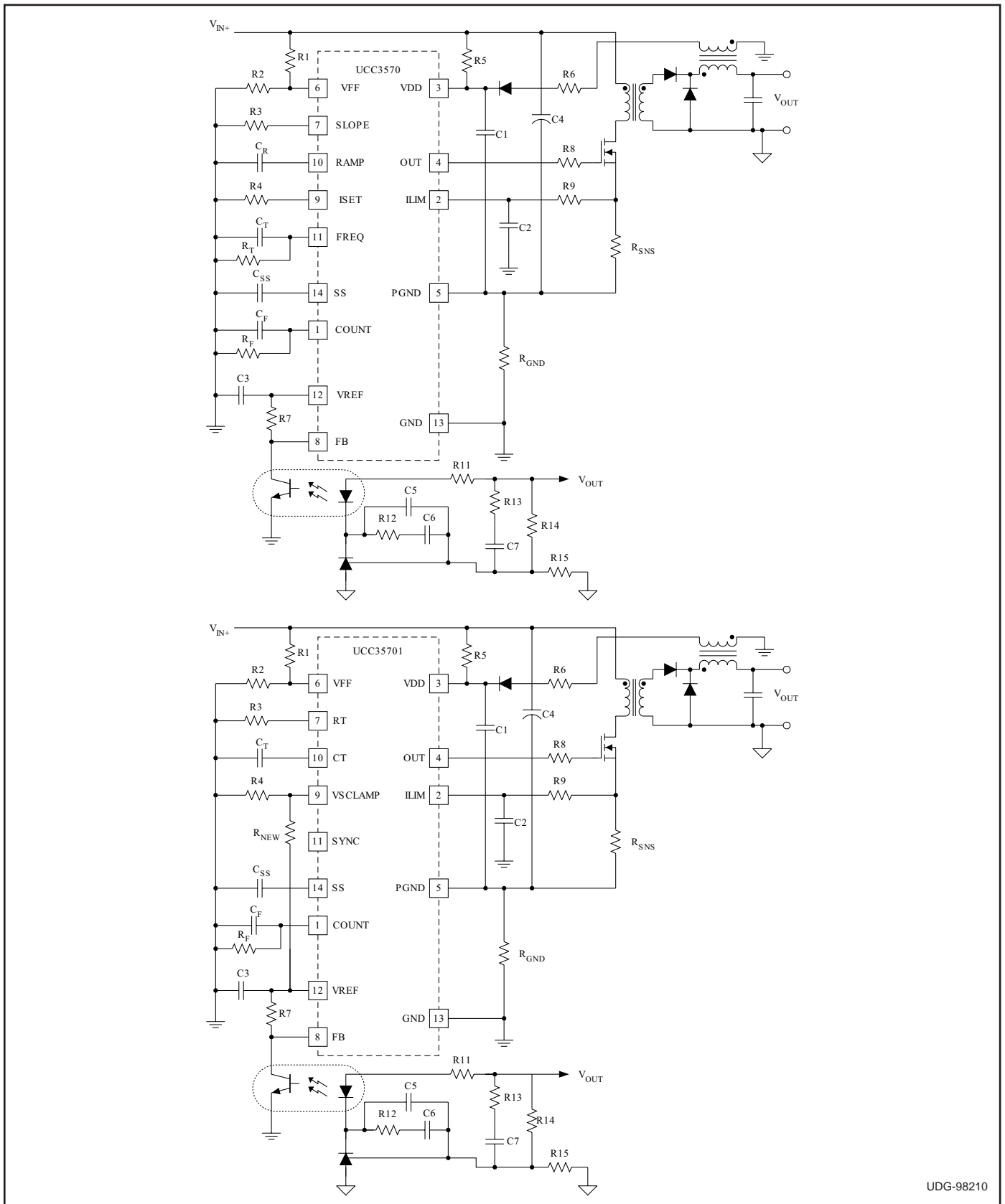


Figure 4. Oscillator frequency vs. temperature.

APPLICATION INFORMATION (cont.)



UDG-98210

Figure 6. Single-ended forward circuit comparison between UCC3570 and UCC37501.

REVISION HISTORY

DATE	REVISION	REASON
02/16/05	SLUS293B	Add FB to abs max table. Created revision history table.
6/16/05	SLUS293C	Updated block diagram and the SS pin description.



www.ti.com

PACKAGE OPTION ADDENDUM

28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC15701J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	Samples Not Available
UCC15701L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
UCC25701D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC25701DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC25701DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC25701DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC25701N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC25701NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC25701PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC25701PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC25701PWTR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC25701PWTRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC25702D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC25702DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC25702DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC25702DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC25702N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC25702NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples



www.ti.com

PACKAGE OPTION ADDENDUM

28-Aug-2010

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC25702PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC25702PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC25702PWTR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC25702PWTRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC35701D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC35701DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC35701DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC35701DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
UCC35701N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC35701NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC35701PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC35701PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
UCC35701Q	OBSOLETE		UTR	20		TBD	Call TI	Call TI	Samples Not Available
UCC35701QTR	OBSOLETE		UTR	20		TBD	Call TI	Call TI	Samples Not Available
UCC35702D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC35702DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
UCC35702N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC35702NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
UCC35702PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples



www.ti.com

PACKAGE OPTION ADDENDUM

28-Aug-2010

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC35702PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC15701, UCC35701 :

● Catalog: [UCC35701](#)

● Military: [UCC15701](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product



www.ti.com

PACKAGE OPTION ADDENDUM

28-Aug-2010

-
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25701DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UCC25701PWTR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
UCC25702DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UCC25702PWTR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
UCC35701DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25701DTR	SOIC	D	14	2500	333.2	345.9	28.6
UCC25701PWTR	TSSOP	PW	14	2000	346.0	346.0	29.0
UCC25702DTR	SOIC	D	14	2500	333.2	345.9	28.6
UCC25702PWTR	TSSOP	PW	14	2000	346.0	346.0	29.0
UCC35701DTR	SOIC	D	14	2500	333.2	345.9	28.6

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

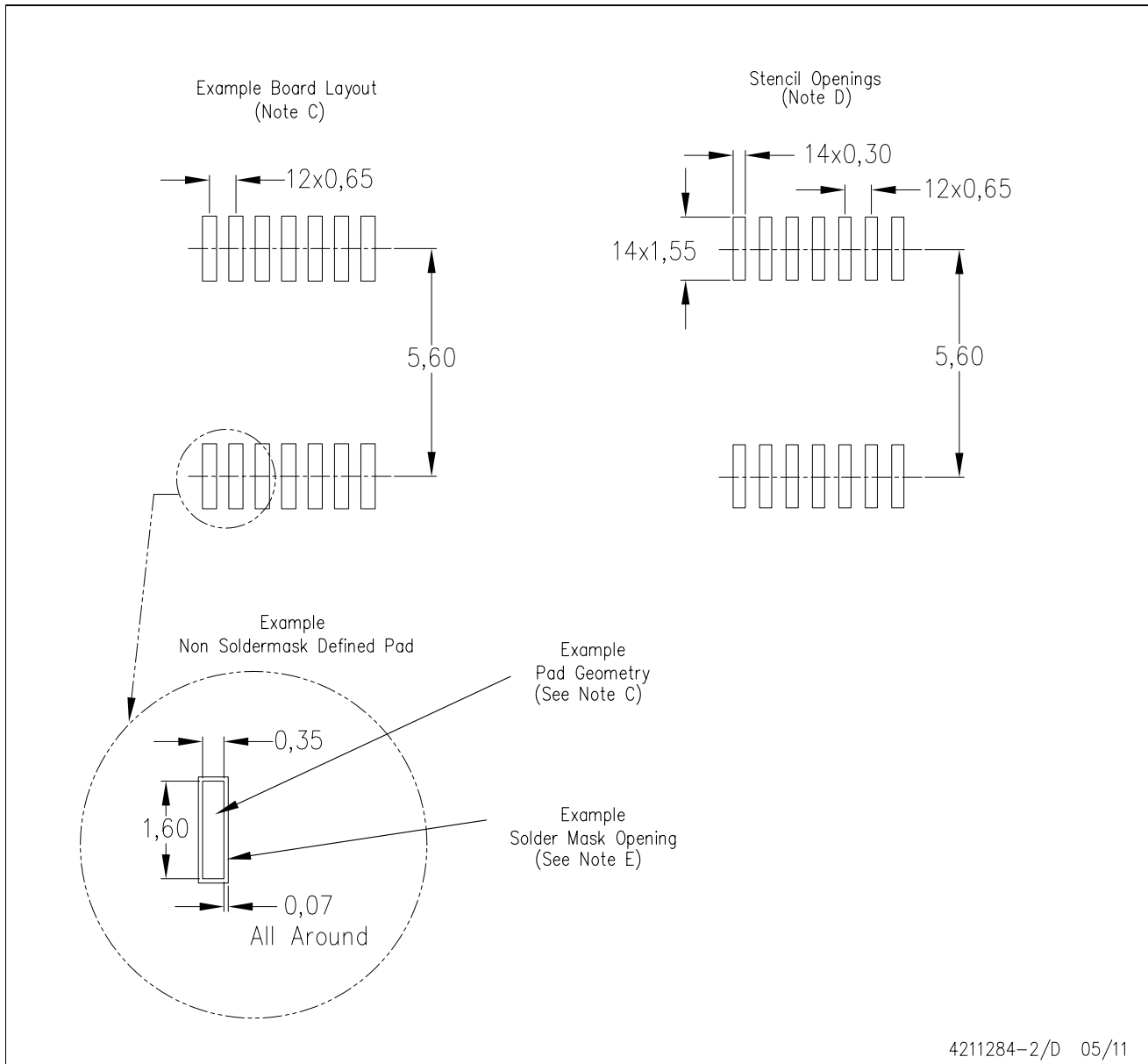


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/D 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated