

These release notes for the DDR and DDR2 SDRAM Controller Compiler version 3.4.1 contain the following information:

- System Requirements
- New Features & Enhancements
- Errata Fixed in This Release
- Obtain & Install the DDR & DDR2 SDRAM Controller
- Contacting Altera
- Revision History

## System Requirements

To use DDR and DDR2 SDRAM Controller Compiler v3.4.1, the following system requirements exist:

- A computer running any of the following operating systems:
  - Windows 2000/XP
  - Red Hat Enterprise Linux 3 or 4WS (with support for 32-bit , AMD64, or Intel EM64T workstations)
  - Solaris 8 or 9 (32-bit or 64-bit)
- Quartus® II software version 6.0 or higher
- Adobe Reader version 5.0 or higher, for viewing PDF documentation
- Mozilla Firefox 1.0 or higher on computers running the RedHat Linux or Solaris operating systems for following web links

## New Features & Enhancements

The following list outlines new features and enhancements in this release:

- Support for Cyclone II A devices

## Errata Fixed in This Release

The following errata were fixed in this release:

- Verify Timing Script Fails (Stratix II Devices)
- Verify Timing Script Fails (Stratix II GX Devices)



For existing up-to-date errata, refer to the *DDR and DDR2 SDRAM Controller Compiler v3.4.1 Errata Sheet* at [www.altera.com/literature/es/es\\_ddr\\_ddr2\\_sdram\\_341.pdf](http://www.altera.com/literature/es/es_ddr_ddr2_sdram_341.pdf).

## Obtain & Install the DDR & DDR2 SDRAM Controller

Before you can start using Altera® MegaCore functions, you must obtain the MegaCore files and install them on your computer. Altera MegaCore functions can be installed from the MegaCore IP Library CD-ROM during or after Quartus II installation, or downloaded individually from the Altera web site and installed separately.

### Download the DDR & DDR2 SDRAM Controller Compiler

If you have Internet access, you can download MegaCore functions from Altera's web site at [www.altera.com](http://www.altera.com). Follow the instructions below to obtain the DDR and DDR2 SDRAM Controller Compiler from the Internet. If you do not have Internet access, contact your local Altera representative to obtain the MegaCore IP Library CD-ROM.

1. Point your web browser to [www.altera.com/ipmegastore](http://www.altera.com/ipmegastore).
2. Type DDR in the **IP MegaSearch** box.
3. Click **Go**.
4. Choose **DDR SDRAM Controller** or **DDR2 SDRAM Controller** from the search results page. The product description web page displays.
5. Click **Download Free Evaluation** on the product description web page.
6. Fill out the registration form and click **Submit Request**.
7. Read the Altera MegaCore license agreement, turn on the **I have read the license agreement** check box, and click **Proceed to Download Page**.
8. Follow the instructions on the DDR and DDR2 SDRAM Controller Compiler download and installation page to download the function and save it to your hard disk.



Ensure you download the MegaCore function for the operating system on which the MegaCore function will be running.

### Installing the DDR & DDR2 SDRAM Controller Compiler Files

The following instructions describe how you install the DDR and DDR2 SDRAM Controller Compiler on computers running the Windows, Linux, or Solaris operating systems.

### *Windows*

To install the DDR and DDR2 SDRAM controller on a computer running the Windows operating system, follow these steps:

1. Choose **Run** (Start menu).
2. Type `<path name>\ddr_ddr2_sdram-v3.4.1.exe`, where *<path name>* is the location of the downloaded MegaCore function.
3. Click **OK**. The **DDR & DDR2 SDRAM Controller Installation** dialog box appears. Follow the on-screen instructions to finish installation.

### *Solaris & Linux*

To install the DDR & DDR2 SDRAM controller on a computer running the Solaris and Linux operating systems, type the following command:

1. Decompress the package by typing the following command:

```
gzip -d ddr_ddr2_sdram-v3.4.1_linux.tar.gz↵
```

*or*

```
gzip -d ddr_ddr2_sdram-v3.4.1_solaris.tar.gz↵
```

2. Extract the package by typing the following command:

```
tar xvf ddr_ddr2_sdram-v3.4.1_linux.tar↵
```

*or*

```
tar xvf ddr_ddr2_sdram-v3.4.1_solaris.tar↵
```

## **Contacting Altera**

Although every effort has been made to ensure that this version of the DDR and DDR2 SDRAM Controller works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera world-wide website at [www.altera.com](http://www.altera.com). You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Information Type	USA & Canada	All Other Locations
Technical support	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	<a href="http://www.altera.com">www.altera.com</a>	<a href="http://www.altera.com">www.altera.com</a>
Altera literature services	<a href="mailto:literature@altera.com">literature@altera.com</a>	<a href="mailto:literature@altera.com">literature@altera.com</a>
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	<a href="ftp://ftp.altera.com">ftp.altera.com</a>	<a href="ftp://ftp.altera.com">ftp.altera.com</a>

## Revision History

[Table 2](#) shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

Version	Date	Revision
3.4.1	June 2006	See <a href="#">“New Features &amp; Enhancements”</a> on page 1.
3.4.0	April 2006	<ul style="list-style-type: none"> <li>• Datapath includes round-trip delay model</li> <li>• Support for clock generation using dedicated PLL outputs</li> <li>• Improved support for fed-back clock</li> <li>• Full support for Cyclone™ II devices</li> </ul>
3.3.1	November 2005	Maintenance release.
3.3.0	October 2005	<ul style="list-style-type: none"> <li>• Custom control of on-die termination (ODT) settings for DDR2 SDRAM</li> <li>• Support for eight banks</li> <li>• Each data strobe (DQS) signal supports four or eight data bits (DQ) on Stratix II devices</li> <li>• Full support for Stratix® II devices in DDR2 SDRAM</li> <li>• Preliminary support for HardCopy® II and Stratix II GX devices</li> <li>• Improved Cyclone II constraints for push-button 167-MHz performance</li> <li>• Improved timing analysis scripts and constraints</li> </ul>



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
[www.altera.com](http://www.altera.com)  
**Applications Hotline:**  
(800) 800-EPLD  
**Literature Services:**  
[literature@altera.com](mailto:literature@altera.com)

Copyright © 2006 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

