PCI Compiler

April 2006, Compiler Version 4.1.1 — Release Notes

These release notes for the PCI Compiler version 4.1.1 contain the following information:

System Requirements

To use the PCI Compiler version 4.1.1, the following system requirements exist:

- A computer running any of the following operating systems:
  - Windows 2000/XP
  - Red Hat Enterprise Linux 3 or 4 WS (with support for 32-bit, AMD64, or Intel EM64T workstations)
  - Solaris 8 or 9 (32-bit or 64-bit)
- Quartus® II software version 6.0 or higher
- PCI Compiler version 4.1.1
- Mozilla Firefox 1.0 or higher on computers running the RedHat Linux or Solaris operating systems for following web links
- Adobe Reader version 5.0 or higher for viewing PDF documentation
- ModelSim® or ModelSim-Altera Edition simulator version 6.1d or higher or any other Altera supported simulator.

New Features & Enhancements

This is a maintenance release. The following list outlines new features and enhancements in this release:

- Updated HardCopy® II Device Family Support
- Updated Stratix® II GX Device Family Support

Errata Fixed in This Release

The only erratum from PCI Compiler v4.1.0, the default installation path correction, has been corrected in the updated *PCI Compiler User Guide* for this release.

For existing up-to-date errata, refer to the PCI Compiler version 4.1.1 errata sheet on the following errata page of the Altera website:

www.altera.com/literature/es/es_pci_compiler_411.pdf

Obtain & Install the PCI Compiler

Before you can use the PCI Compiler, you must obtain the files and install them on your computer. Altera MegaCore® functions can be installed from the MegaCore IP Library CD-ROM during or after Quartus II installation, or downloaded individually from the Altera website and installed separately.

Download the PCI Compiler

If you have Internet access, you can download PCI Compiler from Altera's website at www.altera.com. Follow the instructions below to obtain the PCI Compiler MegaCore functions from the Internet. If you do not have Internet access, contact your local Altera representative to obtain the MegaCore IP Library CD-ROM.

1. Point your web browser to **www.altera.com/ipmegastore**
2. Type **PCI** in the IP MegaSearch box.
3. Click **Go**.
4. Choose PCI Compiler from the search results page. The product description web page displays.
5. Click **Download Free Evaluation** on the top right of the product description web page. Fill out the registration form and click **Submit Request**.
6. Read the Altera MegaCore license agreement, turn on the I have read the license agreement check box, and click **Proceed to Download Page**.

7. Follow the instructions on the PCI Compiler download and installation page to download the appropriate PCI Compiler installation file.

Install the PCI Compiler Files

The following instructions describe how you install the PCI Compiler on computers running the Windows, Linux, or Solaris operating systems.

Windows

Follow these steps to install PCI Compiler on a PC running a supported version of the Windows operating system:

1. Choose **Run** (Windows Start menu).

2. Type <*path name*>\pci_compiler-v4.1.1.exe, where <*path*> is the location of the downloaded MegaCore function.

3. Click **OK**. The **PCI Compiler Installation** dialog box appears. Follow the on-screen instructions to finish installation.

Solaris & Linux

Follow these steps to install PCI Compiler on computers running supported versions of the Solaris or Linux operating systems:

1. Move the compressed files to the desired installation directory and make that directory your current directory.

2. Decompress the package by typing the following command:

   gunzip -d pci_compiler-v4.1.1_<*operating system*>.tar.gz ↵

   where <*operating system*> is either solaris or linux.

3. Extract the package contents by typing the following command:

   tar -xvf pci_compiler-v4.1.1_<*operating system*>.tar ↵

   where <*operating system*> is either solaris or linux.

Contact Altera

Although every effort has been made to ensure that this version of the PCI Compiler works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera website at **www.altera.com**. You can also contact Altera through your local sales representative or any of the sources listed in Table 1.

Table 1. Contacting Altera

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Revision History

Table 2 shows the revision history for the PCI Compiler version 4.1.1.

Table 2. PCI Compiler Revision History

Version	Date	Revision
4.1.1	April 2006	• Maintenance release; updated documentation and screen shots to reflect release version. • Fixed the default installation path in the documentation. • Removed installation instructions from the PCI Compiler User Guide. • Moved the reference design and timing information from the release notes to the user guide.
4.1.0	October 2005	• Added preliminary support for Stratix II GX and HardCopy II device families. • Updated support for Stratix II, MAX II, and Cyclone II device families. • Reduced device utilization for PCI-Avalon Bridge • Fixed the following MegaWizard Plug-In Manager flow problems: - The CIS pointer default value was made to be 0x00000000 instead of 0x00000001 • Fixed the following SOPC Builder flow problems: -The prefetchable write transactions were made to disconnect at BAR boundary. - Fixed a configuration address translation bug that prevented the selection of `idsel=AD[31]` - Fixed the issue in which for 32-bit master read transactions, byte enables from the Avalon side were not being passed to the PCI side. - Corrected the issue where `intan` was asserted after `reset` if the Control register module is not implemented. • Fixed the following issues that affect both flows: - The pci_mt64 did not end the PCI master transactions immediately following the `lm_lastn` assertion in the case of a 32-bit PCI target response to a 64-bit write request and the PCI Target is asserting random wait states. - In the case of an Address parity error detected by the PCI core, the PCI core used to also enable the perrn drivers although it does not assert `devseln`. - Fixed protocol violation where `stopn` was asserted after the end of the transaction in the case of wait states on `irdyn`. - Fixed protocol violation where `framen` was not deasserted immediately after detecting `stopn` asserted during 64-bit master write transaction to 32-bit target with target wait states. - Fixed a protocol violation where `framen` was asserted for one cycle during single cycle DAC memory read transaction.

Table 2. PCI Compiler Revision History

Version	Date	Revision
4.0.0	April 2005	• Updated user guide of the PCI Compiler. Divided the user guide into two sections. The first section contains the previous version of the user guide, which describes the PCI Compiler with the MegaWizard flow. The second section describes the PCI Compiler with the SOPC Builder flow, new feature added in v4.0.0 of the PCI Compiler. • Provided an SOPC Builder ready PCI component. • PCI MegaCore function fixes • Corrected the problem when `framen` and `req64n` are not asserted properly during dual address cycle transactions if `lm_lastn` signal is asserted during the address phase in the single-cycle master read transaction.
3.2.0	June 2004	• Added preliminary support for Cyclone II device family • Added support for the *PCI Local Bus Specification, Revision 3.0*
3.1.0	April 2004	• Added preliminary support for MAX II device family Added support for the *PCI Local Bus Specification, Revision 2.3* Concatenated the constraint files of all the device densities and packages for a given device family to a single constraint file Tcl script. For example, the **pci310_q40sp1_cyclone_cf.tcl** Tcl script includes PCI constraints for all the PCI supported devices and packages in the Cyclone family. Includes constraint files for all supported device families and development boards Modified the installation directory structure to include example Quartus II projects for all PCI MegaCore functions in the **/qexample** directory PCI MegaCore function fixes. • Corrected the problem that had previously caused the PCI bus to behave badly when a single cycle master write transaction, in which `lm_rdyn` was asserted in the same clock cycle as `lm_adr_ackn` on the local side interface, resulted in the `framen` signal on the PCI bus to stay low.
3.0.0	February 2004	• Added preliminary support for Stratix II device family • Added OpenCore® Plus evaluation feature • Updated the pci_mt64 and pci_mt32 reference designs to support Stratix II, Stratix, Stratix GX, and Cyclone devices • Made PCI MegaCore function fixes: - Corrected the master's handling retry in the case where the local logic does not assert `lm_rdyn` signal. - Corrected the target read data output when the `lt_rdyn` signal from the previous target write transaction is overly extended to the current transaction. - Fixed the problem where incorrect data was transferred to the local side when `lm_req32n` or `lm_req64n` was asserted by the local master logic and the PCI MegaCore function also was performing a target write transaction.

Table 2. PCI Compiler Revision History

Version	Date	Revision
2.4.0	September 2003	• Improved timing for Stratix and Cyclone device families. • Added IP Toolbench, a toolbar from which you can quickly and easily view documentation, specify the MegaCore function (pci_mt64, pci_mt32, pci_t64, or pci_t32), customize the MegaCore function, and generate all of the files necessary for integrating the parameterized MegaCore function variation into your design.You also can use this to generate an IP functional simulation model that you can use to verify your custom PCI MegaCore function in any Altera-supported simulator. • PCI MegaCore function fixes: • Corrected the issue with pci_mt64 and pci_mt32 where `irdy`, under rare conditions, is not asserted properly during the last data phase of a master memory burst write transaction. The conditions include cases where the PCI target issues a disconnect with data and the local side de-asserts `lm_rdyn` in the same clock cycle.
2.3.0	February 2003	• Improved timing for Stratix device family. • PCI MegaCore function fixes.
2.2.0	September 2002	• Added Cyclone Device Support Updated pci_mt32 and pci_mt64 reference designs for pci_mt64 and pci_mt32 MegaCore functions v2.2.0. • Consolidated documentation and reduced number of PDF documents. • 66-MHz support for FLEX® 10KE and ACEX® 1K devices is supported in Quartus II software. • 66-MHz support in MAX+PLUS II is discontinued. • Corrected PCI MegaWizard issues in Solaris platform. Updated PCI Behavioral models to use latest simulator and VIP software. • Updated PCI Reference designs to the latest pci_mt64 and pci_mt32 revisions. • PCI MegaCore function fixes: • Corrected behavior of `l_ldat_ackn` and `l_hdat_ackn` when an incomplete master read transaction if followed by target read transaction. • Corrected behavior during bus parking while the bus is not idle. • Master will indicate master abort even during configuration transactions. • Corrected behavior of `ack64n` getting asserted for one additional clock during rare master local wait cycles during a target retry condition

Table 2. PCI Compiler Revision History

Version	Date	Revision
2.0.0	August 2001	• Improved the look and feel of the PCI Compiler wizard and added support for new PCI MegaCore features. Updated the PCI MegaCore functions to v2.0.0. See the revision history in the readme files for each individual PCI MegaCore function for details on the changes. Included behavioral simulation models for all PCI MegaCore functions to support VHDL and Verilog HDL simulators. Included an open source PCI testbench in VHDL and Verilog HDL. Updated pci_mt32 and pci_mt64 reference designs for pci_mt64 and pci_mt32 MegaCore functions v2.0.0. Due to enhanced support in the PCI Compiler wizard for constraint files, the command line utility set_constraint was removed from the PCI Compiler. Use the PCI Compiler MegaWizard to create project specific constraint files for your design. **Added PCI MegaCore function features:** • Added the **Add Internal Data Steering Logic for 32/64-Bit Systems** option, which provides improved logic optimization to let you attain 66 MHz performance more easily. When disabled, this option removes the internal data steering logic from `l_dato[63..32]` and `l_beno[7..4]`, providing valid data on `l_dato[31..0]` and `l_beno[3..0]` during a 32-bit transaction. When enabled, valid data is available on `l_dato[63..0]` and `l_beno[7..0]` during a 32-bit transaction and the operation is fully compatible with previous versions of pci_mt64. The Add Internal Data Steering Logic for 32/64-Bit Systems option is available in the PCI Compiler wizard; the option sets bit 14 of the `ENABLE_BITS` parameter. • Added the **Host Bridge Enable** option to allow the pci_mt64 function to be used as a system host. When enabled, the option causes the pci_mt64 MegaCore function to power up with the master enable bit in the command register hardwired to 1 and allows the master interface to initiate configuration read and write transactions to the internal configuration space. The Host Bridge Enable option is available in the PCI Compiler wizard; the option sets bit 13 of the `ENABLE_BITS` parameter. • Added the **64-Bit Only Devices option** to provide enhanced functionality for 64-bit only systems. When enabled, the option improves the latency of the pci_mt64 master PCI signals (especially `irdyn`) to be the same as those in 32-bit transactions. This feature also enables single-cycle master writes and adds the functionality previously offered through the `PCI_64BIT_SYSTEM` parameter. The 64-Bit Only Devices option is available in the PCI Compiler wizard; the option sets bit 16 of the `ENABLE_BITS` parameter. • The **PCI_64BIT_SYSTEM parameter** has been disabled. You must enable this option in designs that previously used the `PCI_64BIT_SYSTEM` parameter. • Added the ability to permanently **disable the pci_mt64 master latency timer registerm** which prevents the latency timer from expiring. The option is available in the PCI Compiler wizard; the option sets bit 15 of the `ENABLE_BITS` parameter. • **Enabled the master** to keep the PCI bus when `gntn` is asserted and the latency timer expires. Additionally, the local side signal `lm_tsr[4]`, which indicates that the latency timer has expired, is not set until `gnt` is removed.

Table 2. PCI Compiler Revision History

Version	Date	Revision
1.3.0	February 2001	• First release • PCI MegaCore functions included the pci_mt64, pci_mt32, pci_t64, and pci_t32 functions.

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