



Quick Start

PCB2115 Demonstration Board

ADC1613D, ADC1413D, ADC1213D, ADC1113D series

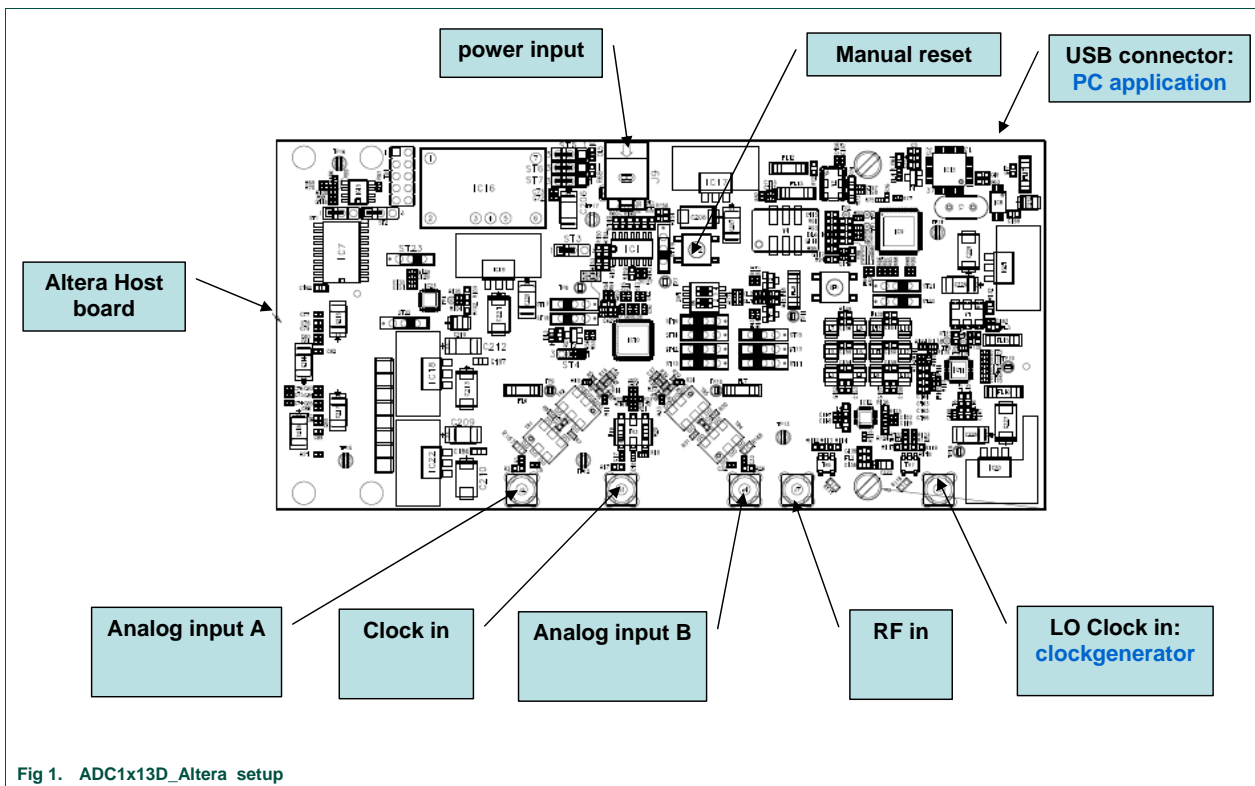
Rev. 1 — 10th March 2010

Document information	
Info	Content
Keywords	PCB2115, Demonstration board, ADC, ADC1613D, ADC1413D, ADC1213D, ADC1113D, Altera, Xilinx, Lattice,
Abstract	This document describes how to use the demonstration board PCB2115 (ADC1x13D board without FPGA)
Block Diagram	<p>The I/Q Demodulator down converts an RF signal to IF frequency based on programmed LO synthesizer frequency. The dual ADC performs IF baseband sampling, and transmits real digital data to FPGA connector via the JESD204A interface. The Clock Generator provides clocks for entire system, including ADC and FPGA. The SPI interface provides control and status of all programmable elements. In standalone mode, the SPI bus is controlled by USB interface. In FPGA mode the SPI bus is directly controlled by FPGA.</p>
Main features	<ul style="list-style-type: none"> • ADC sampling rate = 125MSPS max. • The ADC clock provided by either on board clock generator or by an external clock generator • ADC input connected to either on board RF I/Q demodulator or to external IF inputs. • Demodulation sampling rate controlled by either on board LO synthesizer or by an external clock. • Maximum ADC analog input bandwidth will be 600MHz. • Standalone mode : <ul style="list-style-type: none"> ○ ADC, ADC clock generator and Demodulator clock synthesizer are controlled by PC application via SPI/USB interface ○ Single 6.5Vdc external power supply • FPGA mode : <ul style="list-style-type: none"> ○ ADC, ADC clock generator and Demodulator clock synthesizer are controlled by FPGA via SPI interface ○ Power supply from 12Vdc FPGA host board

1. Quick start

1.1 Setup overview

The following figure presents the connections of the ADC1x13D_Altera board.

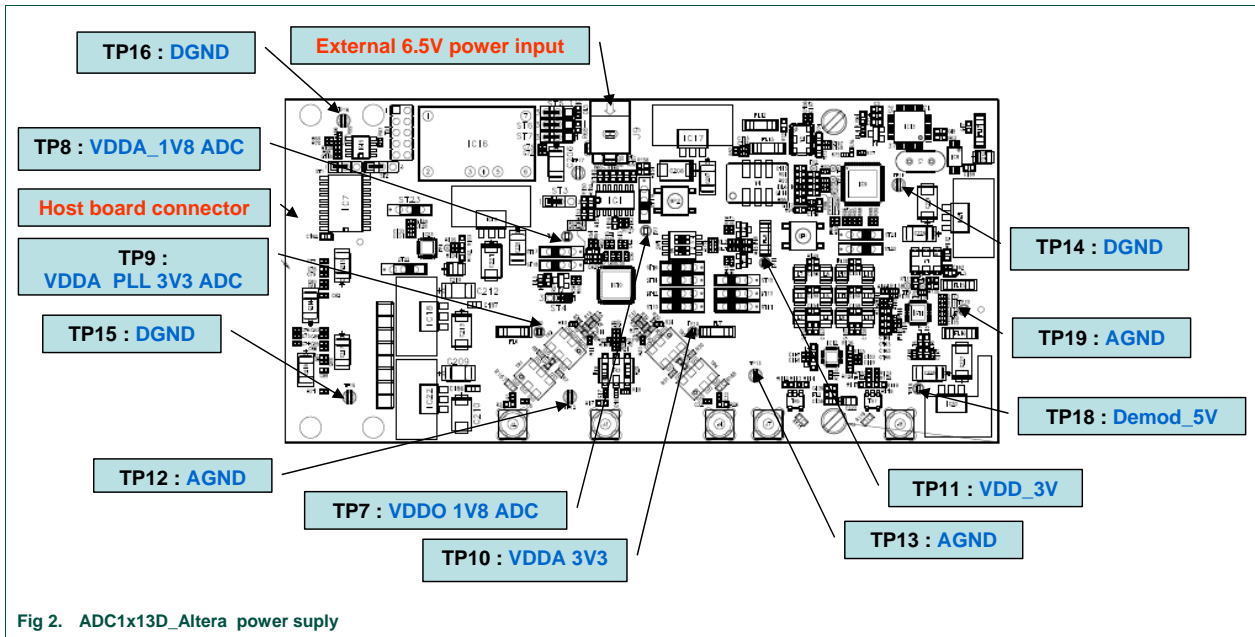


1.2 FPGA Board interface

The PCB2115 board includes an HSMC connector in order to connect it to the Altera evaluation board. In order to connect to the Xilinx evaluation board, the board adaptor reference HSDC_ACC01/DB need to be used. In order to connect to the Lattice evaluation board, the board adaptor reference HSDC_ACC02/DB need to be used. Both addaptator need to be ordered separately.

1.3 Power supply

The following figure presents the power supply input / test point of the ADC1x13D_Altera board:



1.4 Board configuration

The ADC1x13D_Altera board could be used in several configurations:

- SPI bus could be controlled by FPGA (=host board) or by USB interface (=PC application)
- The board could be power by host board or by external power supply
- FPGA clock could be provided by on board clock generator or by external clock.
- ADC clock could be provided by on board clock generator or by external clock.
- ADC inputs could be connected to on board demodulator or external source.

The selection between above configurations is done using mounting options, jumpers or switches. The following figure enables to locate the components used in these different configurations. Following chapter give detail information about all these configurations.

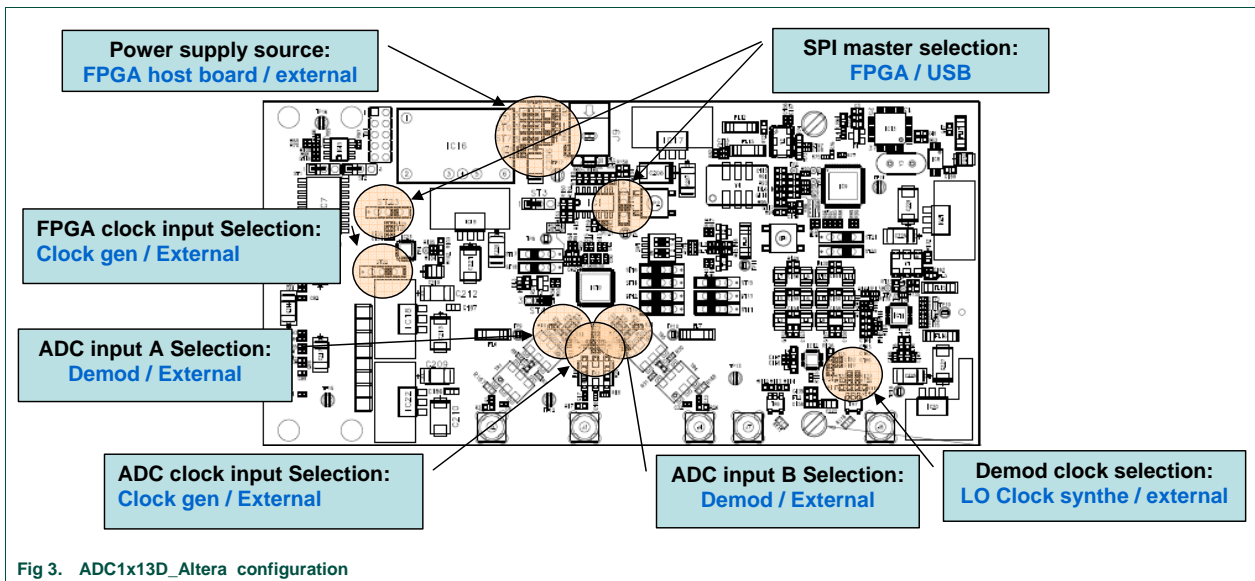
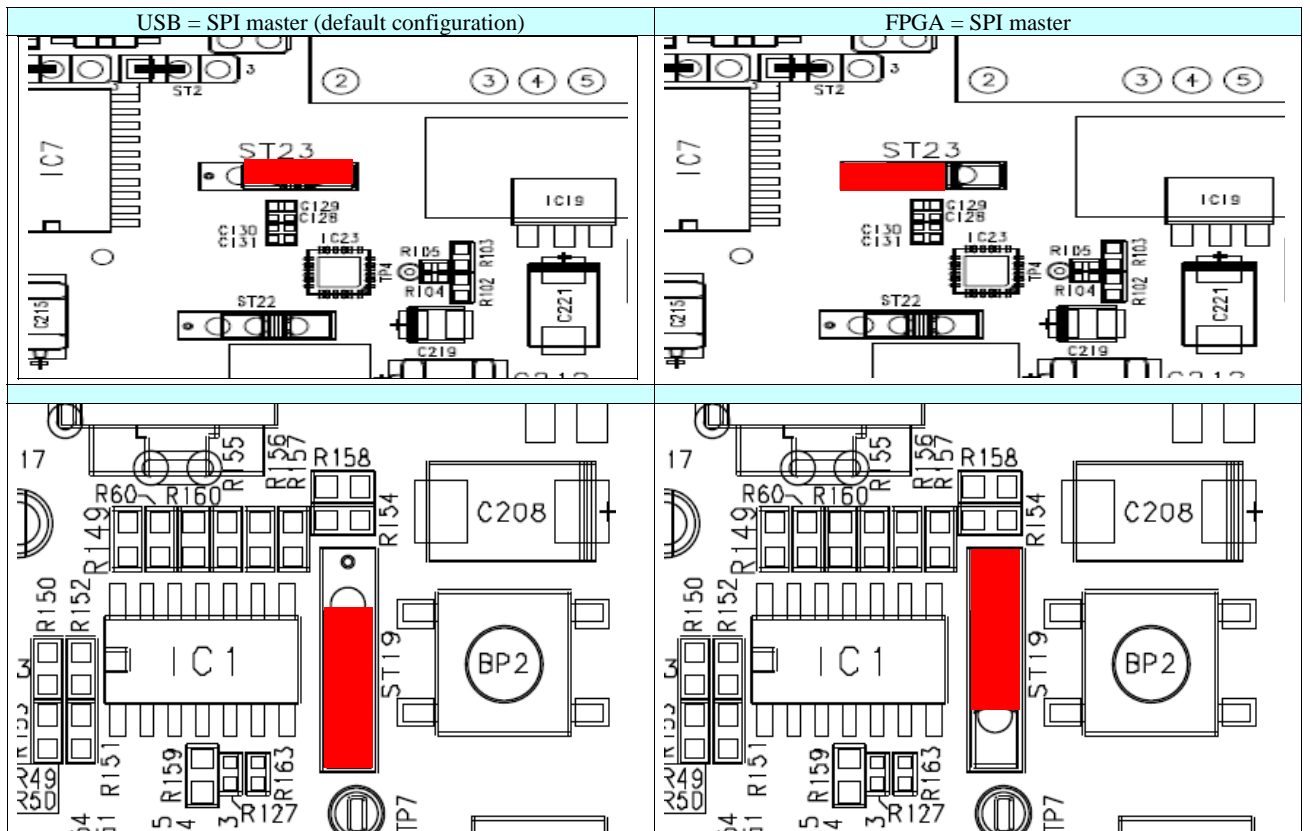


Fig 3. ADC1x13D_Altera configuration

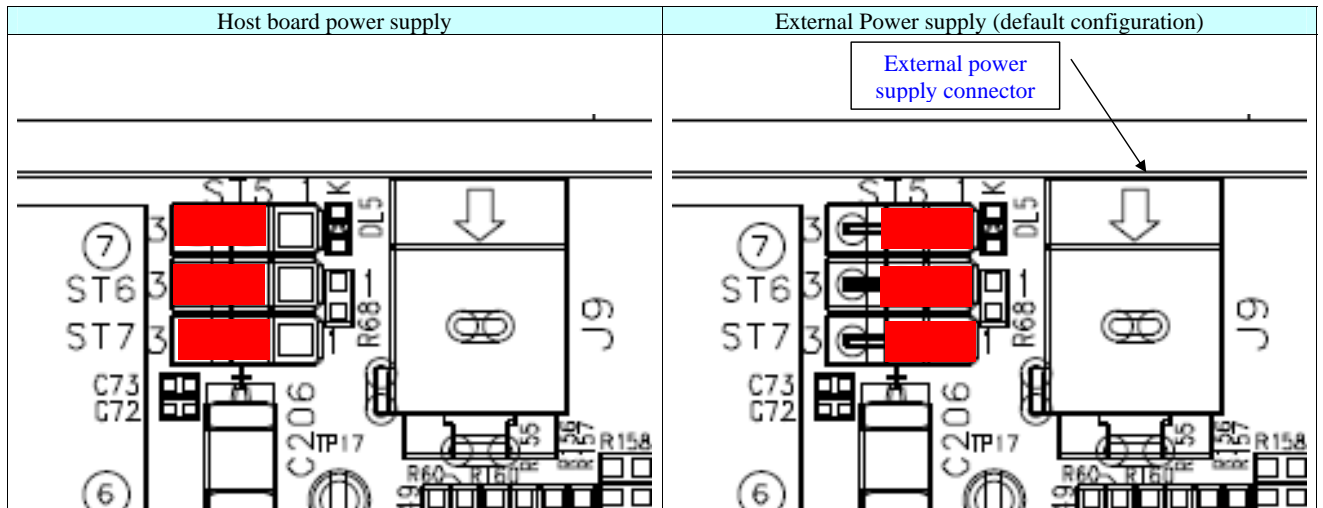
1.4.1 SPI bus master configuration

The ADC, the ADC clock generator and the Demodulator clock synthesizer are programmable using SPI interface. The SPI master could either be the FPGA from the host board or the PC application (USB). Selection between these 2 modes is done as indicated below:



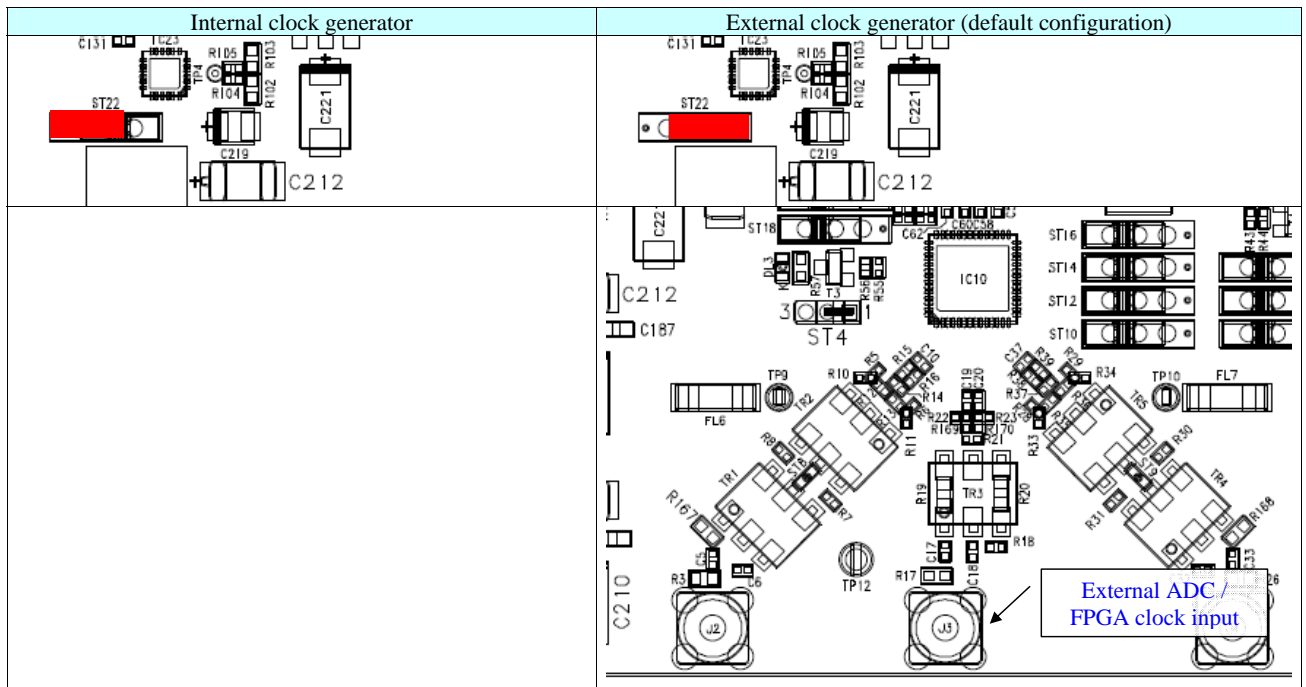
1.4.2 Power supply configuration

The board could be powered by either the host board or by an external power supply. Selection between these 2 modes is done as indicated below:



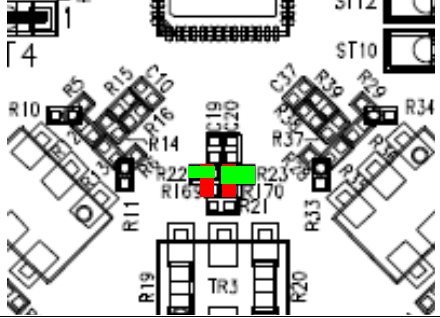
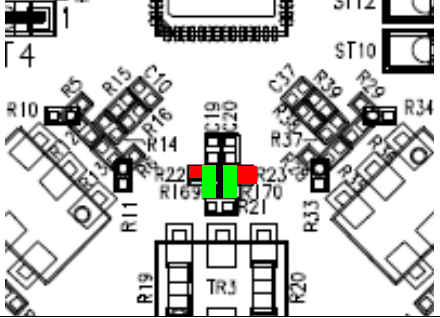




1.4.3 FPGA clock configuration

The FPGA could use the on board clock generator as reference clock or could use an external clock. Selection between these 2 modes is done as indicated below:



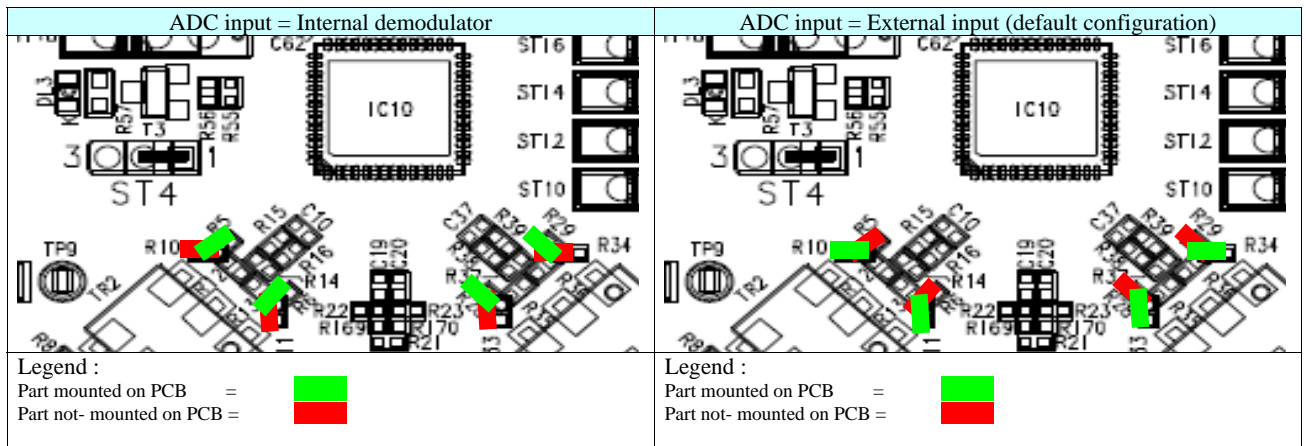
1.4.4 ADC clock configuration

The ADC could use the on board clock generator or an external clock as sampling clock. Selection between these 2 modes is done as indicated below:

Internal clock generator	external clock generator (default configuration)
	
<p>Legend :</p> <p>Part mounted on PCB = </p> <p>Part not- mounted on PCB = </p>	<p>Legend :</p> <p>Part mounted on PCB = </p> <p>Part not- mounted on PCB = </p>

1.4.5 ADC input configuration

The ADC input could be connected to the on board demodulator or to an external source. Selection between these 2 modes is done as indicated below:



2. SPI quick start

2.1 Install

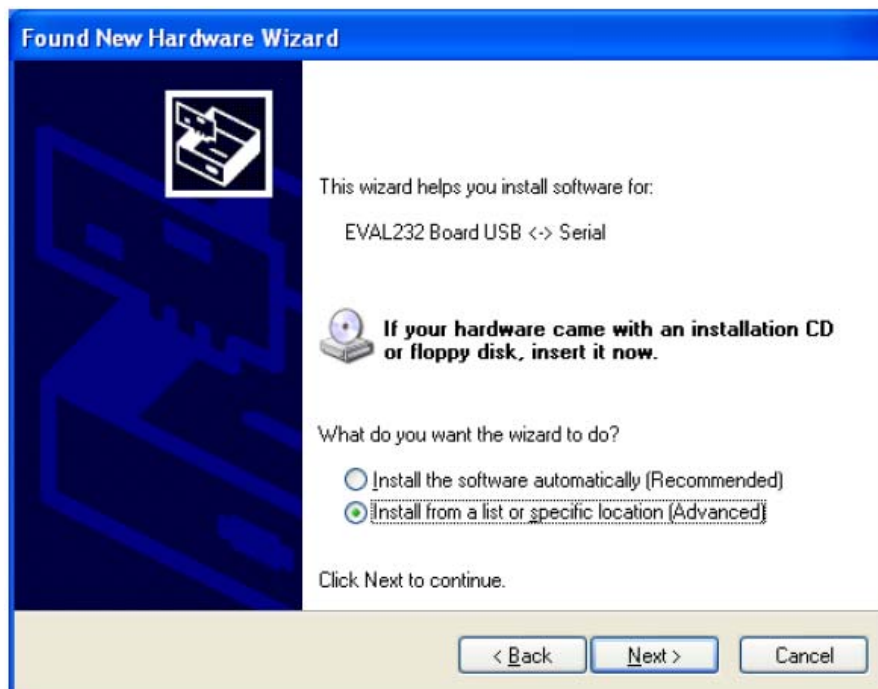
- Step 1

Connect the device to a USB port on your PC. Windows 'Found New Hardware Wizard' will be launched. Select '**No, not this time**' from the options available and then click '**Next**' to proceed with the installation.



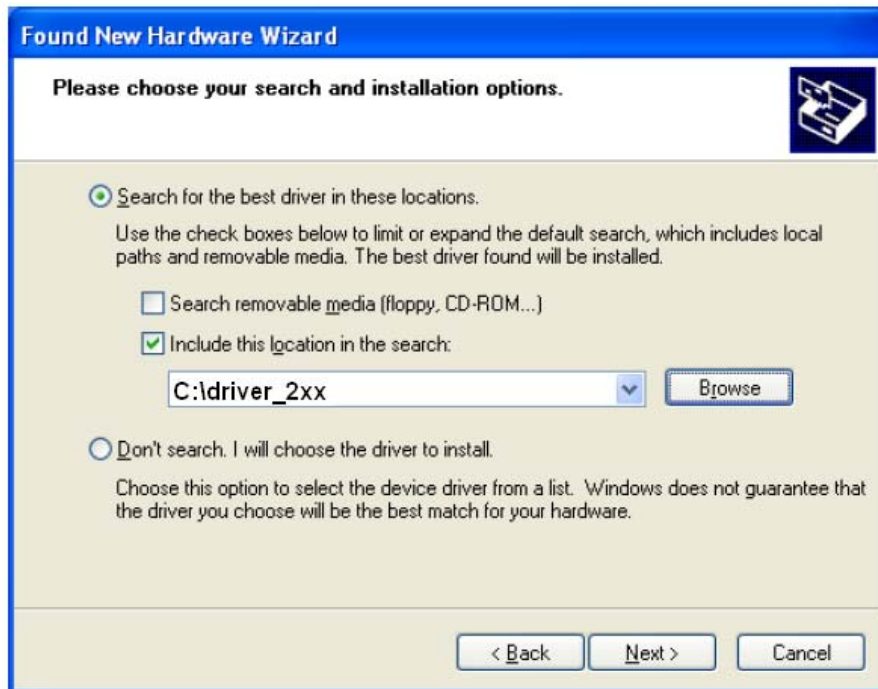
- Step 2

Select '**Install from a list or specific location (Advanced)**' as shown below and then click '**Next**'.



- Step 3

Select **'Search for the best driver in these locations'** and enter the file path of the folder **'driver_2xx'** in the combo-box ('C:\driver_2xx' in the example below) or browse to it by clicking the browse button. Once the file path has been entered in the box, click **'next'** to proceed.



- Step 4

Windows should then display a message indicating that the installation was successful. Click **'Finish'** to complete the installation for the first port of the device.



- Step 5

The Found New Hardware Wizard will continue by installing the USB Serial Converter driver for the second port of the device. The procedure for installing the second port is identical to that for installing the first port from the first screen of the Found New Hardware Wizard.

Once the second port is installed, the device should be ready to be used.

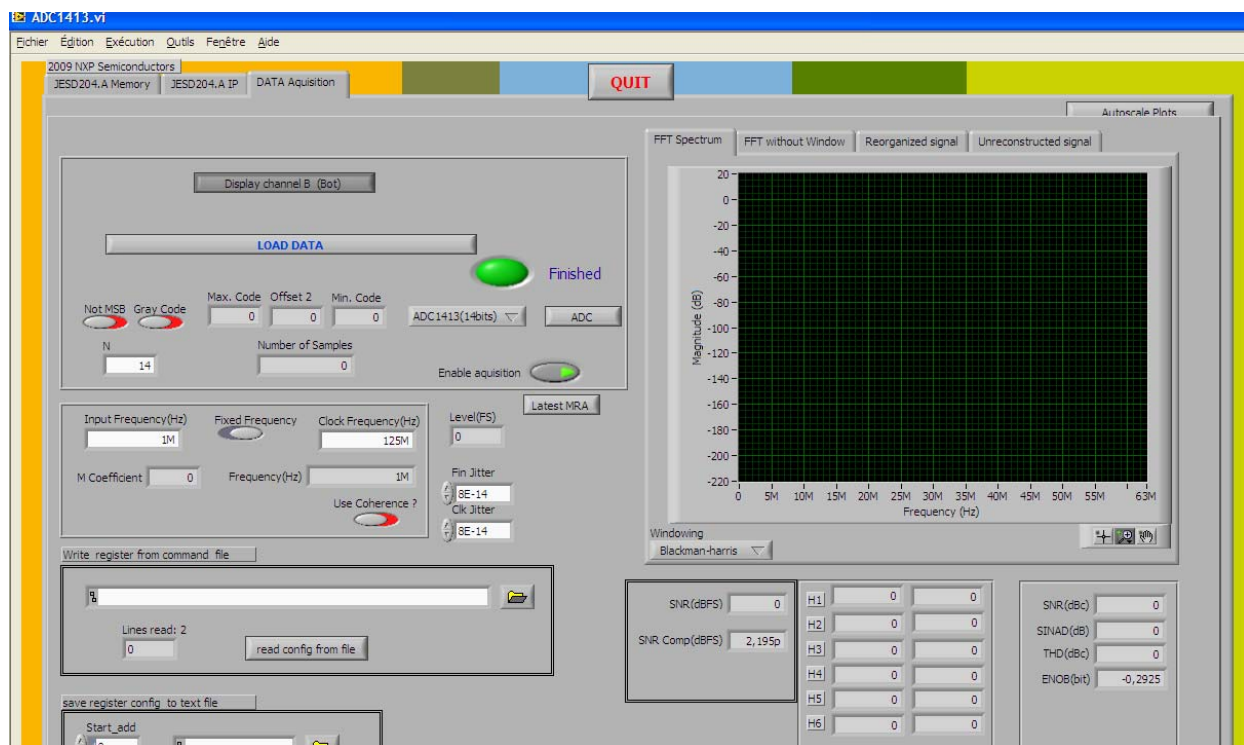
2.2 SPI interface

- Step 1

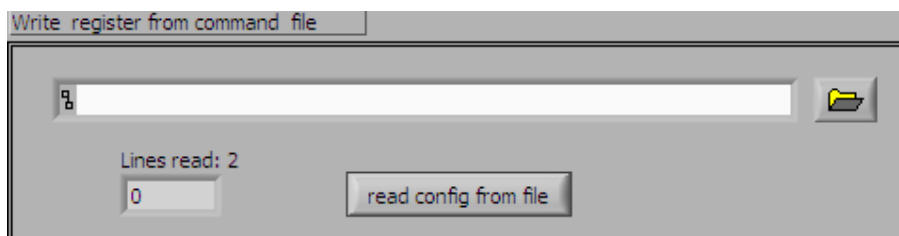
Install the LabVIEW Run-time Engine [LabVIEW85RuntimeEngineFull.exe](#) (if not already installed).

- Step 2

Start the LabVIEW application “ADC1x13.exe”. a graphical window will pop-up



Under the “ Write register from command file” field, choose the write configuration file from “ADC Command” directory depending on the used operating points.



Click on the “read from config file”.

Push the Push_A button on the board to make a manual synchronization of the JESD204A communication.

Input Frequency(Hz) Fixed Frequency Clock Frequency(Hz)

M Coefficient Frequency(Hz)

Use Coherence ?

Fill the Input Frequency and Clock Frequency fields with the wanted operating points.

Display channel B (Bot)

LOAD DATA

Not MSB Gray Code

Max. Code Offset 2 Min. Code

ADC1413(14bits)

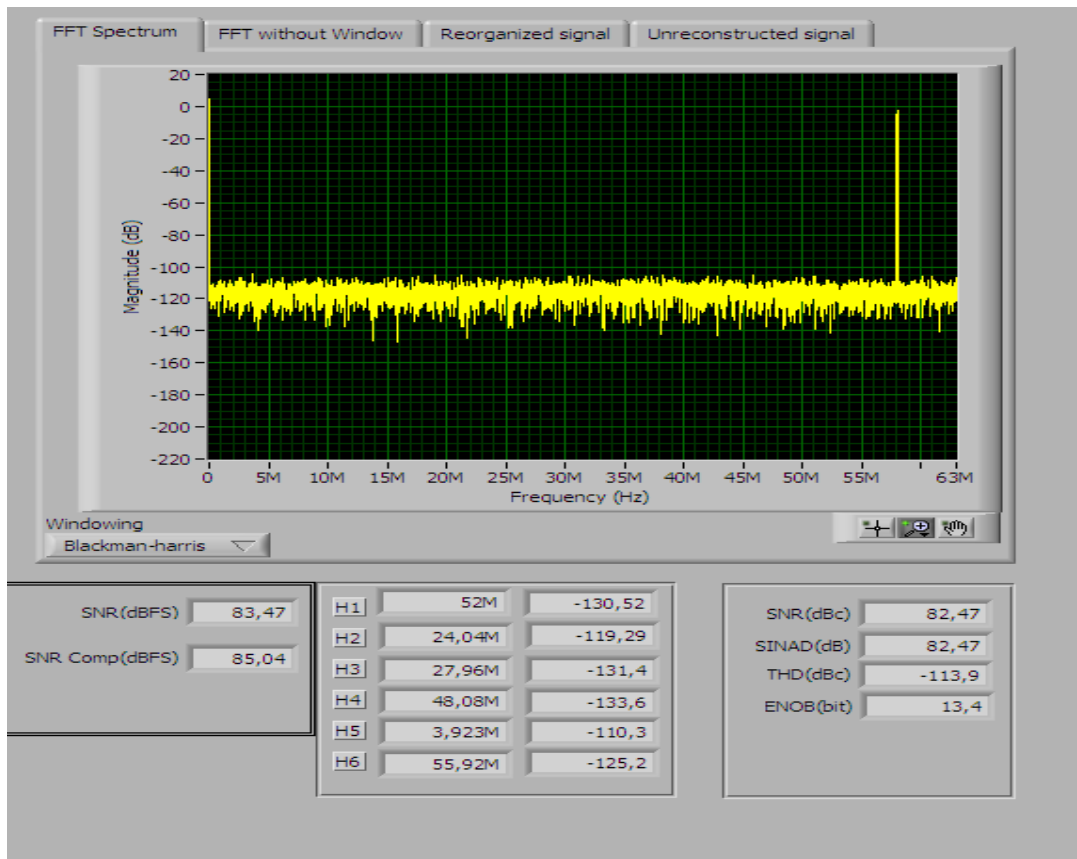
N Number of Samples

Enable aquisition

Finished

Click on ADC button to choose between internal ADC capture or FPGA capture

Click on Load DATA to get the FFT and the ADC performances



Overview of the user interface :

The screenshot shows a software interface for ADC characterization. It includes a control panel on the left with various input fields and buttons, a central plot area showing a spectrum, and a results table on the right. Callout boxes provide instructions for using the interface.

Callout Boxes:

- Load Data to start capturing**: Points to the "LOAD DATA" button.
- Select « latest MRA » → button must be green**: Points to the "Finished" indicator.
- Check input level here**: Points to the "M Coefficient" field.
- Select - Input signal frequency - ADC sampling frequency**: Points to the "Input Frequency (Hz)" and "Clock Frequency (Hz)" fields.
- Select « use coherence » when clock input coherence is OK in order to get SFDR value calculation**: Points to the "Use Coherence?" checkbox.
- Select SPI setting file then click «read config from file» in order to write SPI setting in the device.**: Points to the "read config from file" button.
- SNR value (dbFS)**: Points to the "SNR(dBFS)" field in the results table.
- SFDR value (dBFS) Valid only with single tone signal**: Points to the "SFDR(dBFS)" field in the results table.
- Display Zoom selection**: Points to the zoom controls in the plot area.
- Select FFT without window, Only If clock coherency is OK**: Points to the "FFT without window" radio button.

Results Table:

SNR(dBFS)	7.027	H1	3.631	0	SNR(dB)	8.16n
SNR Comp(dBFS)	7.023	H2	7.2191	-92.558	SNRAC(dB)	0.0416
SFDR(dBFS)	8.22	H3	10.839	-97.494	THK(dB)	20.16
		H4	14.449	-101	ENR(dB)	< 2918
		H5	18.059	-99.01	SFDR(dBc)	2.56
		H6	21.669	-105.7		

