Fully Integrated, Hall Effect-Based Linear Current Sensor IC with High Voltage Isolation and a Low-Resistance Current Conductor

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: November 2, 2009

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

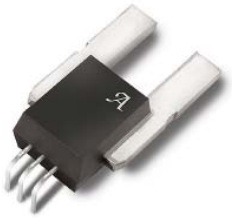
ACS755xCB-150

Fully Integrated, Hall Effect-Based Linear Current Sensor IC with High Voltage Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Monolithic Hall IC for high reliability
- Single +5 V supply
- 3 kV_{RMS} isolation voltage between terminals 4/5 and pins 1/2/3 for up to 1 minute
- 35 kHz bandwidth
- Automotive temperature range
- End-of-line factory-trimmed for gain and offset
- Ultra-low power loss: 100 μΩ internal conductor resistance
- Ratiometric output from supply voltage
- Extremely stable output offset voltage
- Small package size, with easy mounting capability
- Output proportional to DC currents

Package: 5 pin package (leadform PSF)



Description

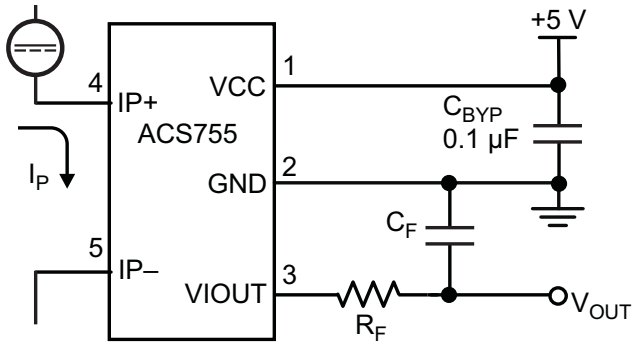
The Allegro ACS755 family of current sensor ICs provides economical and precise solutions for DC current sensing in industrial, automotive, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, power supplies, and overcurrent fault protection.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory.

The output of the device will be valid when a current flows through the primary copper conduction path from terminal 4 to terminal 5, which is the path used for current sampling. The internal resistance of this conductive path is 100 μΩ typical, providing low power loss.

Continued on the next page…

Typical Application



Application 1. The ACS755 outputs an analog signal, V_{OUT}. that varies linearly with the unidirectional DC primary sampled current, I_P, within the range specified. C_F is recommended for noise management, with values that depend on the application.

Description (continued)

The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 1 through 3). This allows the ACS755 family of sensor ICs to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS75x family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

Selection Guide

Part Number	T_{OP} (°C)	Primary Sampled Current, I_P (A)	Sensitivity Sens (Typ.) (mV/A)	Bandwidth (kHz)	Package		Packing[1]
					Terminals	Signal Pins	
~~ACS755KCB-150-PSF~~[2]	–40 to 125	150	26	35	Straight	Formed	170 pieces per bulk bag

[1] Contact Allegro for additional packing options.

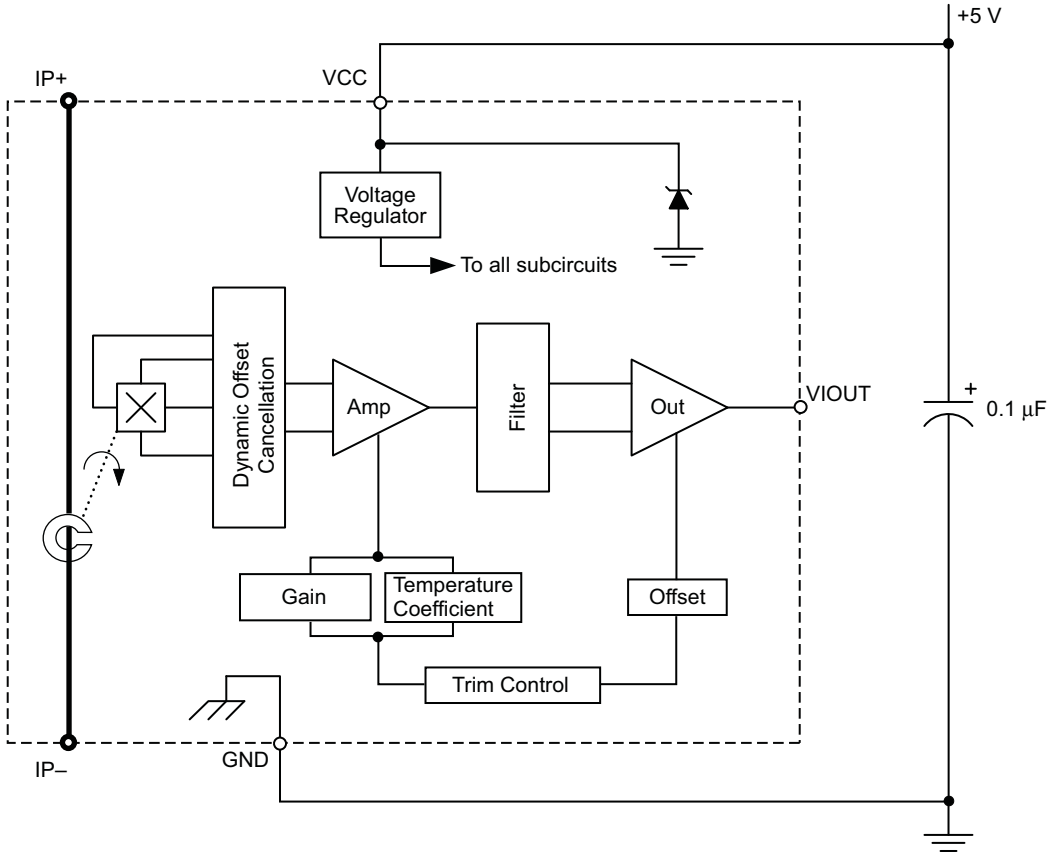
[2] Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 4, 2009. Deadline for receipt of LAST TIME BUY orders is November 4, 2009.

Absolute Maximum Ratings

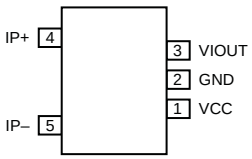
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		16	V
Reverse Supply Voltage	V_{RCC}		–16	V
Output Voltage	V_{IOUT}		16	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Maximum Basic Isolation Voltage	V_{ISO}		353 VAC, 500 VDC, or V_{pk}	V
Maximum Rated Input Current	I_{IN}		200	A
Output Current Source	$I_{OUT(Source)}$		3	mA
Output Current Sink	$I_{OUT(Sink)}$		10	mA
Nominal Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
		Range S	–20 to 85	°C
Maximum Junction	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

TÜV America Certificate Number: U8V 04 11 54214 001	Fire and Electric Shock EN60950-1:2001

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1	VCC	Device power supply pin
2	GND	Signal ground pin
3	VIOUT	Analog output signal pin
4	IP+	Terminal for current being sampled
5	IP–	Terminal for current being sampled

ELECTRICAL CHARACTERISTICS, over operating ambient temperature range unless otherwise stated

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Primary Sampled Current	I_P		0	–	150	A
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	6.5	8	10	mA
Output Resistance	R_{OUT}	I_{OUT} = 1.2 mA	–	1	2	Ω
Output Capacitance Load	C_{LOAD}	VOUT to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VOUT to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	I_P = +50A; T_A = 25°C	–	100	–	µΩ
Isolation Voltage	V_{ISO}	Pins 1-3 and 4-5; 60 Hz, 1 minute	3.0	–	–	kV
PERFORMANCE CHARACTERISTICS, -20°C to +85°C, V_{CC} = 5 V unless otherwise specified						
Propagation time	t_{PROP}	I_P = +50 A, T_A = 25°C	–	4	–	µs
Response time	$t_{RESPONSE}$	I_P = +50 A, T_A = 25°C	–	10	–	µs
Rise time	t_r	I_P = +50 A, T_A = 25°C	–	10	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C	–	35	–	kHz
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	–	26	–	mV/A
		Over full range of I_P	24.5	–	27.5	mV/A
Noise	V_{NOISE}	Peak-to-peak, T_A = 25°C, no external filter	–	50	–	mV
Linearity	E_{LIN}	Over full range of I_P	–	–	±0.95	%
Zero Current Output Voltage	$V_{OUT(Q)}$	I = 0 A, T_A = 25°C	–	0.6	–	V
Electrical Offset Voltage (Magnetic error not included)	V_{OE}	I = 0 A, T_A = 25°C	–15	–	15	mV
		I = 0 A	–25	–	25	mV
Magnetic Offset Error	I_{ERROM}	I = 0 A, after excursion of 150 A	–	±0.1	±0.30	A
Total Output Error (Including all offsets)	E_{TOT}	Over full range of I_P, T_A = 25°C	–	±1.0	–	%
		Over full range of I_P	–	–	±5.0	%
PERFORMANCE CHARACTERISTICS, -40°C to +125°C, V_{CC} = 5 V unless otherwise specified						
Propagation time	t_{PROP}	I_P = +50 A, T_A = 25°C	–	4	–	µs
Response time	$t_{RESPONSE}$	I_P = +50 A, T_A= 25°C	–	10	–	µs
Rise time	t_r	I_P = +50 A, T_A = 25°C	–	10	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C	–	35	–	kHz
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	–	26	–	mV/A
		Over full range of I_P	24	–	28	mV/A
Noise	V_{NOISE}	Peak-to-peak, T_A = 25°C, no external filter	–	50	–	mV
Linearity	E_{LIN}	Over full range of I_P	–	–	±0.95	%
Zero Current Output Voltage	$V_{OUT(Q)}$	I = 0 A, T_A = 25°C	–	0.6	–	V
Electrical Offset Voltage (Magnetic error not included)	V_{OE}	I = 0 A, T_A= 25°C	–15	–	15	mV
		I = 0 A	–40	–	40	mV
Magnetic Offset Error	I_{ERROM}	I = 0 A, after excursion of 150 A	–	±0.1	±0.30	A
Total Output Error (Including all offsets)	E_{TOT}	Over full range of I_P, T_A = 25°C	–	±1.0	–	%
		Over full range of I_P	–	–	±7.0	%

Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left[1-\frac{V_{\text{IOUT\_3/4 full-scale IP}}-V_{\text{IOUT(Q)}}}{3\left(V_{\text{IOUT\_1/4 full-scale IP}}-V_{\text{IOUT(Q)}}\right)}\right]$$

where

$V_{\text{IOUT\_¼ full-scale IP}}$ (V) is the output voltage when the sampled current approximates 0.25 × I_P(max), and
$V_{\text{IOUT\_¾ full-scale IP}}$ (V) is the output voltage when the sampled current approximates 0.75 × I_P(max).

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at 0.6. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value due to nonmagnetic causes.

Magnetic offset error (I_{ERROM}). The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator. The larger magnetic offsets are observed at the lower operating temperatures.

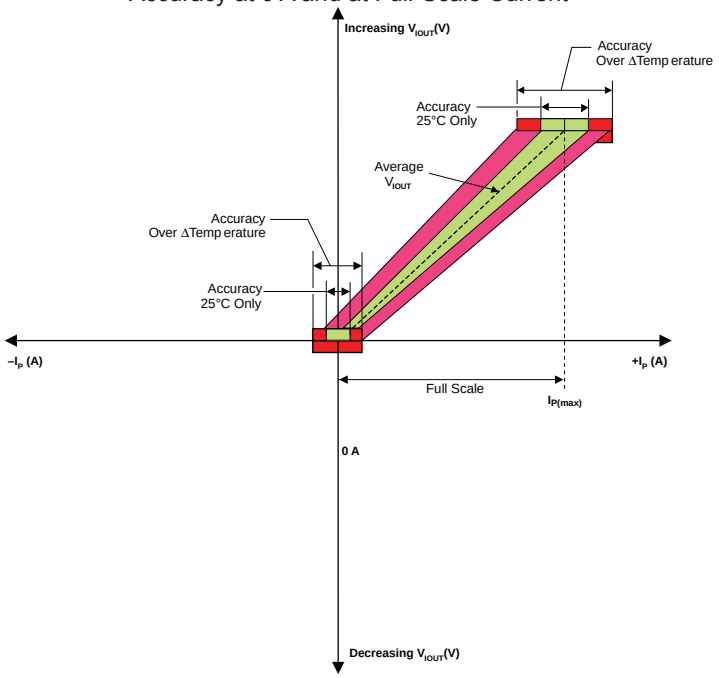
Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart on the following page.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

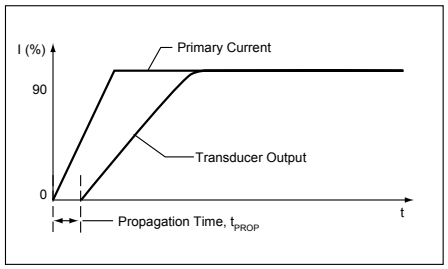
Output Voltage versus Sampled Current

Accuracy at 0 A and at Full-Scale Current

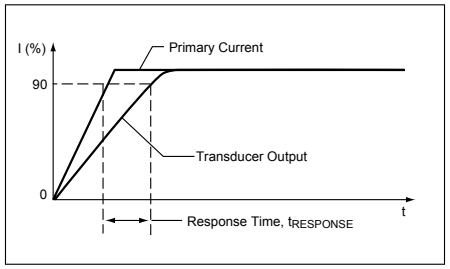


Definitions of Dynamic Response Characteristics

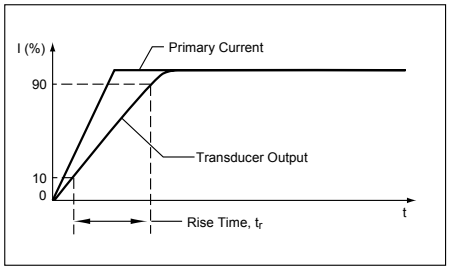
Propagation delay (t_{PROP}). The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



Response time ($t_{RESPONSE}$). The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied current.

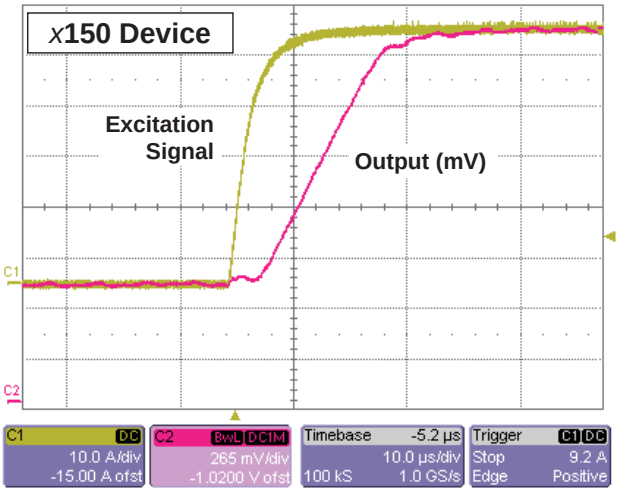


Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\text{ dB}) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

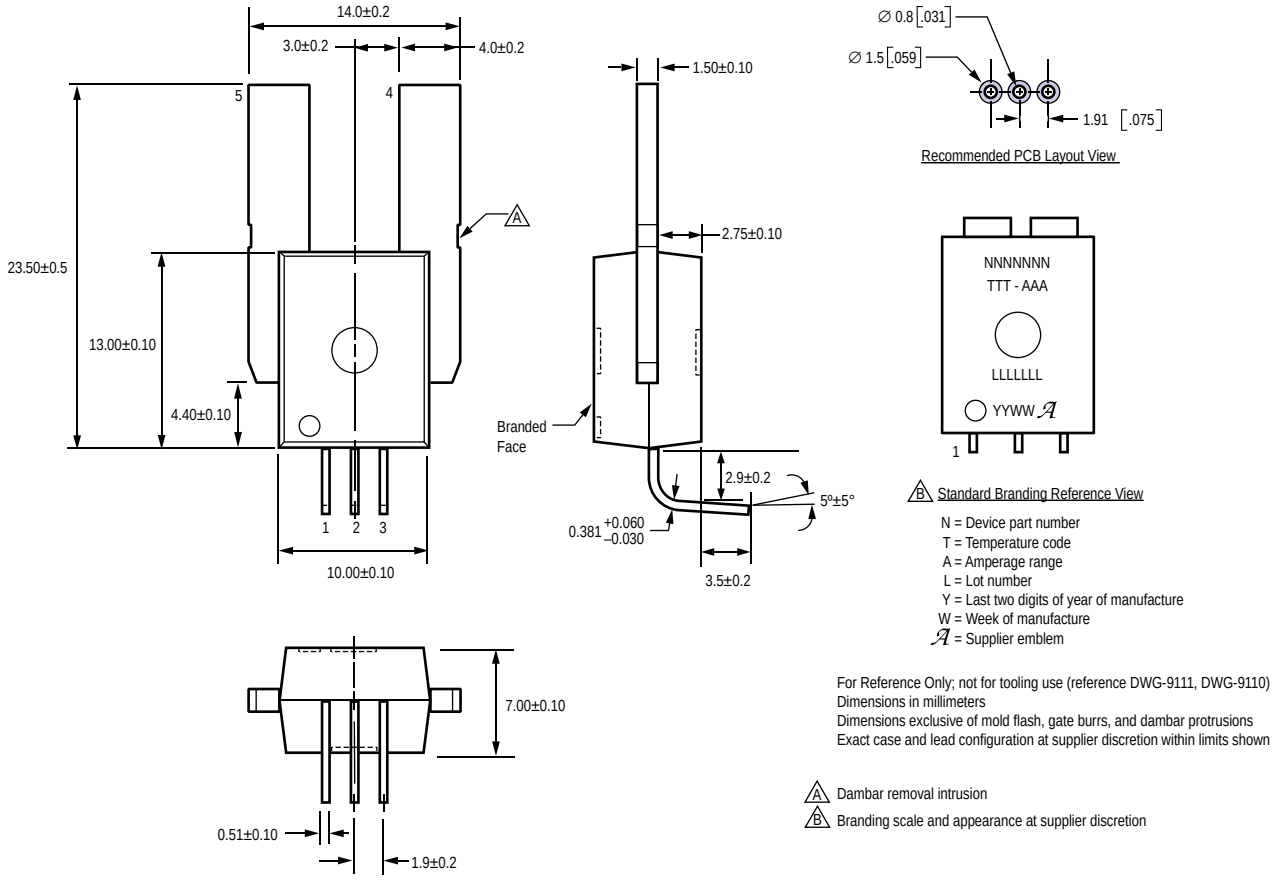


Step Response

50 A Excitation Signal, T_A=25°C



Package CB, 5-pin package
Leadform PSF



Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

The products described herein are manufactured under one or more of the following U.S. patents: 5,619,137; 5,621,319; 6,781,359; 7,075,287; 7,166,807; 7,265,531; 7,425,821; or other patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

www.allegromicro.com