

## 54ABT573

### Octal D-Type Latch with TRI-STATE® Outputs

#### General Description

The 'ABT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

This device is functionally identical to the 'ABT373 but has different pinouts.

#### Features

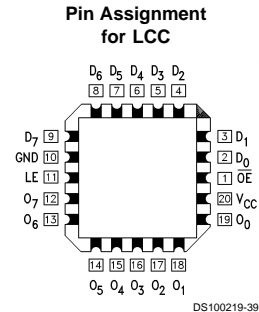
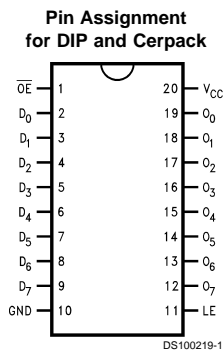
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors

- Functionally identical to 'ABT373
- TRI-STATE outputs for bus interfacing
- Output sink capability of 48 mA, source capability of 24 mA
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed latching protection
- High impedance glitch-free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9321901

#### Ordering Code

Military	Package Number	Package Description
54ABT573J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT573W-QML	W20A	20-Lead Cerpack
54ABT573E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

#### Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

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**54ABT573 Octal D-Type Latch with TRI-STATE Outputs**

## Functional Description

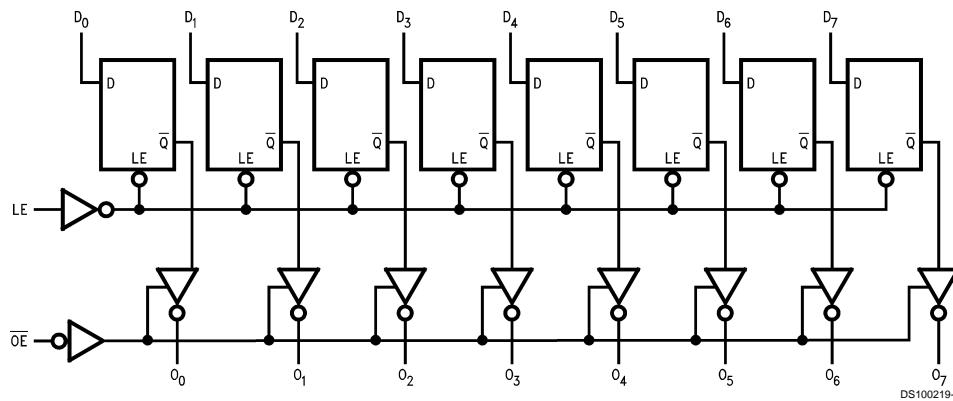
The 'ABT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $O_0$  = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100219-3

## Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	Twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	ABT573			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8		V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA
		54ABT	2.0				I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Note 4)
				5			V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 4)
				-5			V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			50	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}$ = V <sub>CC</sub> All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled		2.5	mA		V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE		2.5	mA	Max	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE		2.5	mA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 4)	No Load			mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, LE = V <sub>CC</sub> (Note 3) One Bit Toggling, 50% Duty Cycle

**Note 3:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed but not tested.

## DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V <sub>CC</sub>	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.9	V	5.0	T <sub>A</sub> = 25°C (Note 5)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>		-1.7	V	5.0	T <sub>A</sub> = 25°C (Note 5)

**Note 5:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

## AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = –55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>PLH</sub>	Propagation Delay	1.0	6.4	ns	Figure 4
t <sub>PHL</sub>	D <sub>n</sub> to O <sub>n</sub>	1.5	6.7		
t <sub>PLH</sub>	Propagation Delay	1.0	7.1	ns	Figure 4
t <sub>PHL</sub>	LE to O <sub>n</sub>	1.5	7.5		
t <sub>PZH</sub>	Output Enable Time	0.8	6.5	ns	Figure 6
t <sub>PZL</sub>		1.5	7.2		
t <sub>PHZ</sub>	Output Disable Time	1.5	7.7	ns	Figure 6
t <sub>PLZ</sub>	Time	1.0	7.0		

## AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = –55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>s</sub> (H)	Set Time, HIGH	2.5		ns	Figure 7
t <sub>s</sub> (L)	or LOW D <sub>n</sub> to LE	2.5			
t <sub>h</sub> (H)	Hold Time, HIGH	2.5		ns	Figure 7
t <sub>h</sub> (L)	or LOW D <sub>n</sub> to LE	2.5			
t <sub>w</sub> (H)	Pulse Width, LE HIGH	3.3		ns	Figure 5

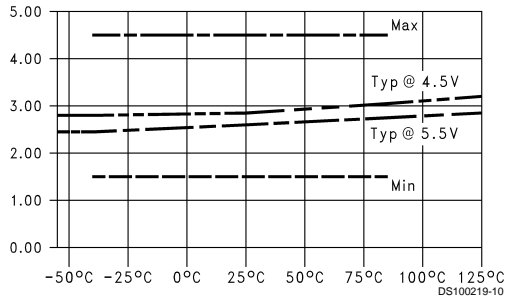
## Capacitance

Symbol	Parameter	Typ	Units	Conditions (T <sub>A</sub> = 25°C)
C <sub>IN</sub>	Input Capacitance	5	pF	V <sub>CC</sub> = 0V
C <sub>OUT</sub> (Note 6)	Output Capacitance	9	pF	V <sub>CC</sub> = 5.0V

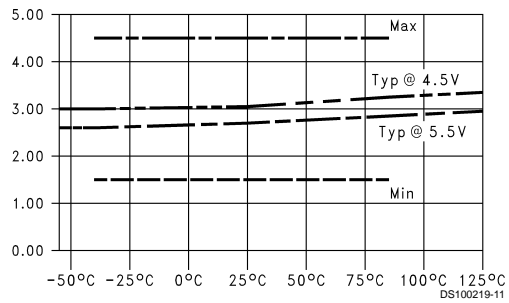
**Note 6:** C<sub>OUT</sub> is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

## Capacitance (Continued)

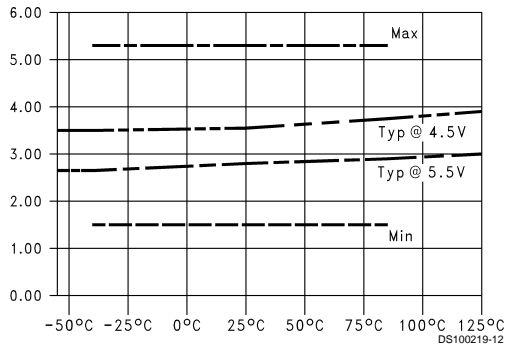
**$T_{PLH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to Output**



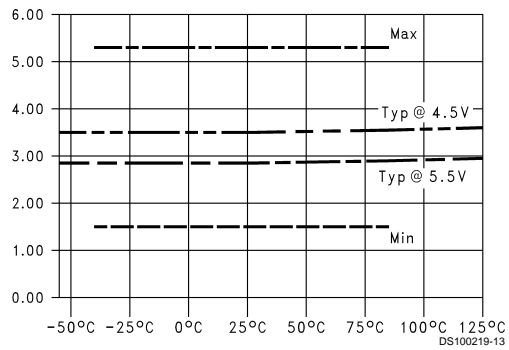
**$T_{PHL}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to Output**



**$T_{PZH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, OE to Output**



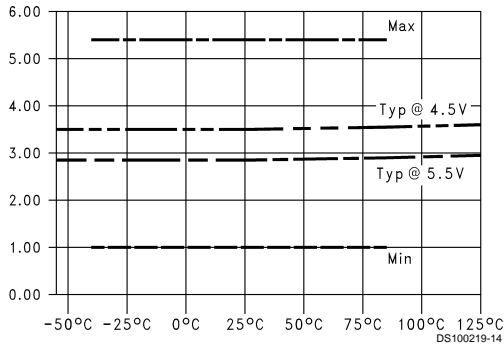
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1 Output Switching, OE to Output**



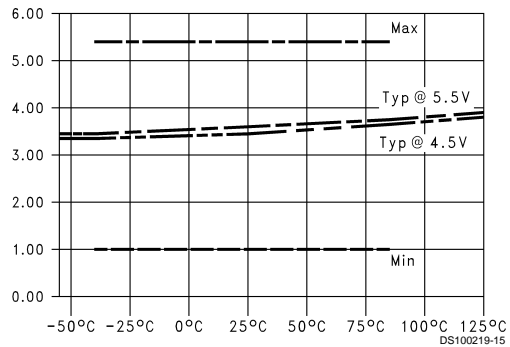
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

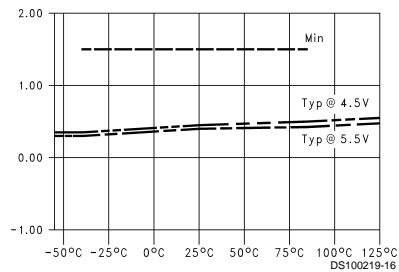
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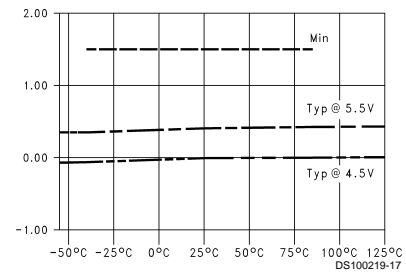
**$T_{PLZ}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, OE to Output**



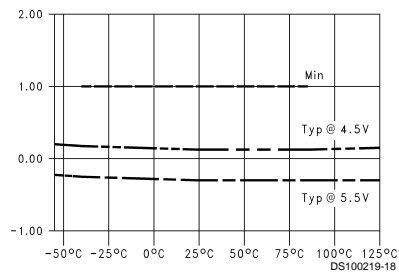
**$T_{SET}$  LOW vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to LE**



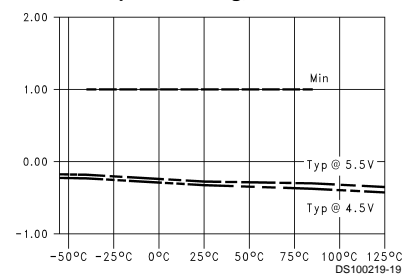
**$T_{SET}$  HIGH vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to LE**



**$T_{HOLD}$  HIGH vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to LE**



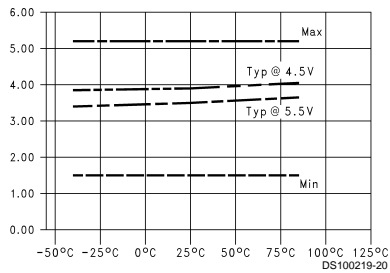
**$T_{HOLD}$  LOW vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, Data to LE**



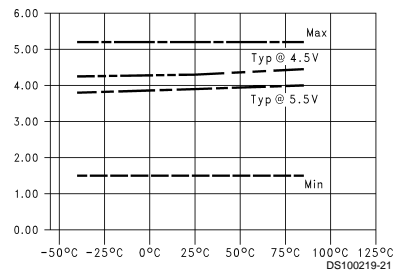
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

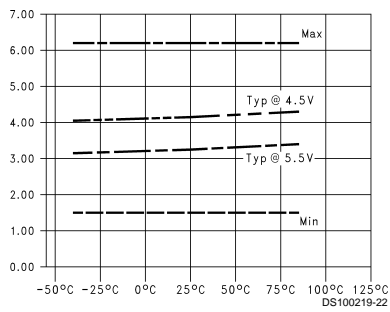
**$T_{PLH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, Data to Output**



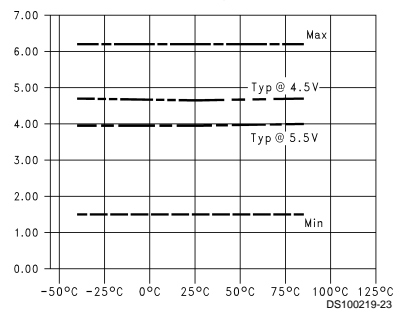
**$T_{PHL}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, Data to Output**



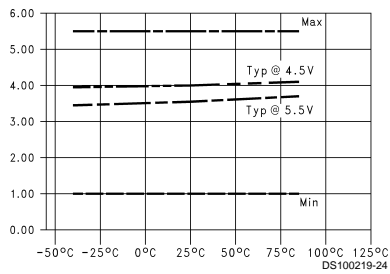
**$T_{PZH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, OE to Output**



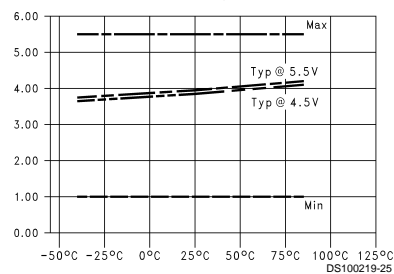
**$T_{PZL}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, OE to Output**



**$T_{PHZ}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, OE to Output**



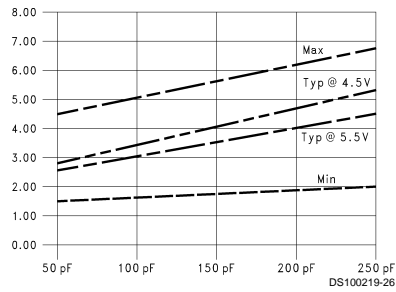
**$T_{PLZ}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, OE to Output**



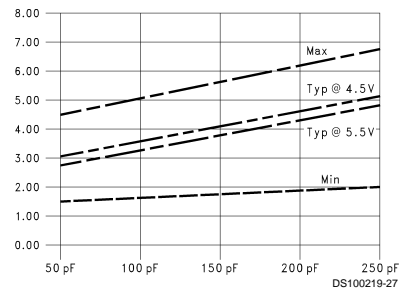
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

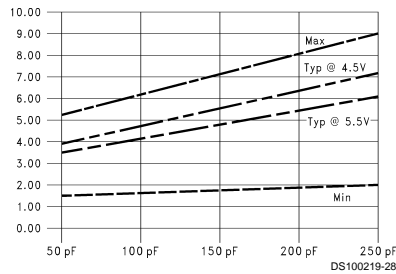
**$T_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching, Data to Output**



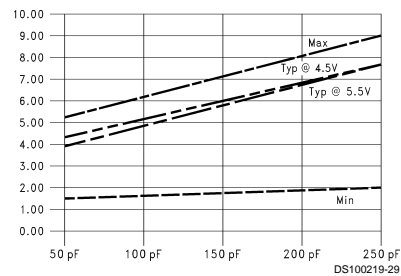
**$T_{PHL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
1 Output Switching, Data to Output**



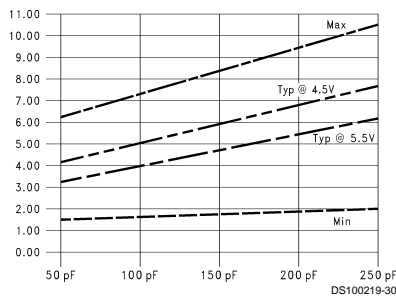
**$T_{PLH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching, Data to Output**



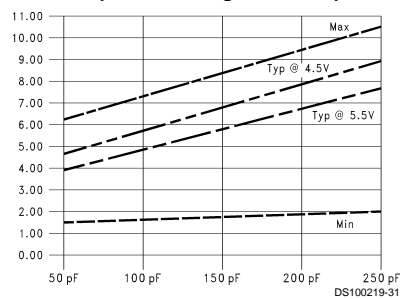
**$T_{PHL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching, Data to Output**



**$T_{PZH}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching, OE to Output**



**$T_{PZL}$  vs Load Capacitance  $T_A = 25^\circ\text{C}$ ,  
8 Outputs Switching, OE to Output**

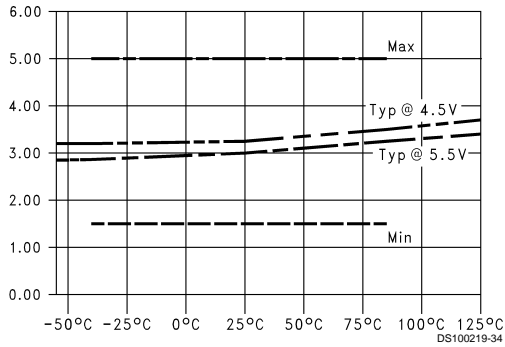


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

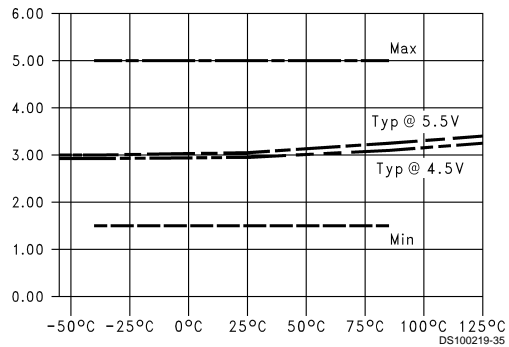


## Capacitance (Continued)

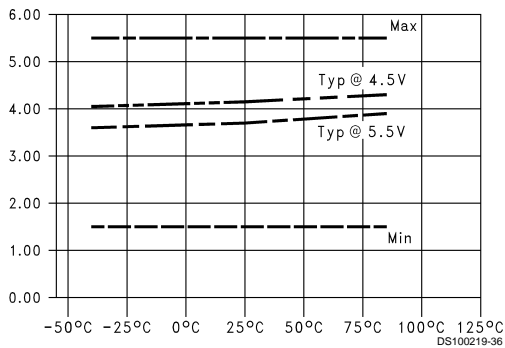
**$T_{PLH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, LE to Output**



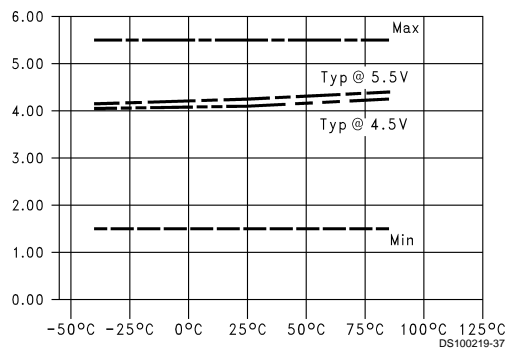
**$T_{PHL}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
1 Output Switching, LE to Output**



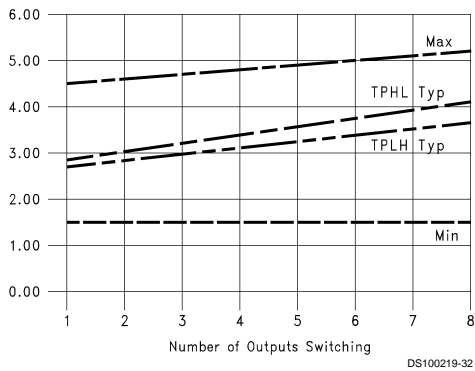
**$T_{PLH}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, LE to Output**



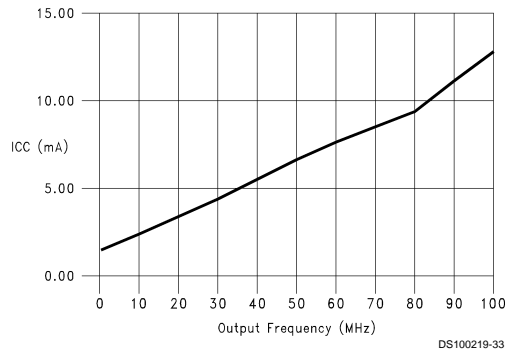
**$T_{PHL}$  vs Temperature ( $T_A$ ),  $C_L = 50$  pF,  
8 Outputs Switching, LE to Output**



**$T_{PLH}$  and  $T_{PHL}$  vs Number Outputs Switching,  
 $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ ,  
Outputs In Phase Data to Output**

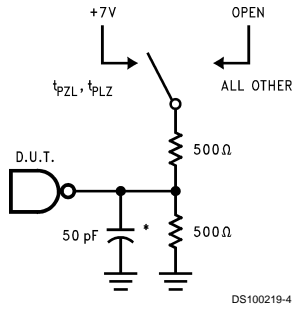


**Typical  $I_{CC}$  vs Output Switching Frequency,  
 $C_L = 0$  pF,  $V_{CC} = V_{IH} = 5.5\text{V}$ , LE = GND,  
1 Output Switching at 50% Duty Cycle, Data to Output,  
Transparent Mode with Unused Data Inputs =  $V_{IH}$**



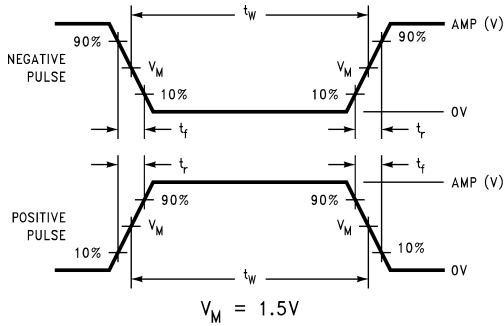
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

# AC Loading



\*Includes jig and probe capacitance

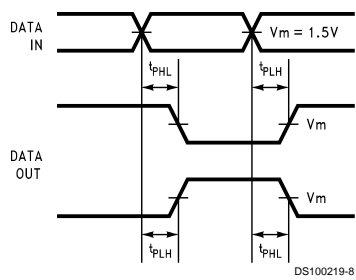
**FIGURE 1. Test Load**



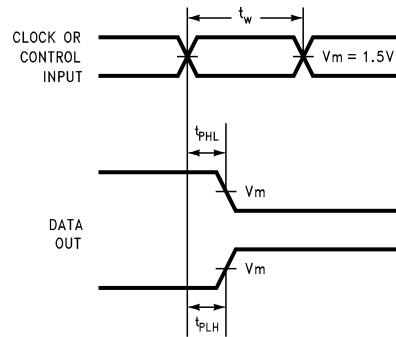
**FIGURE 2. Test Input Signal Levels**

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

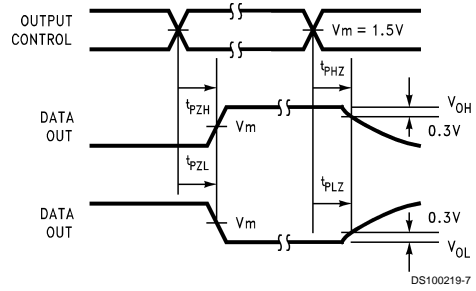
**FIGURE 3. Test Input Signal Requirements**



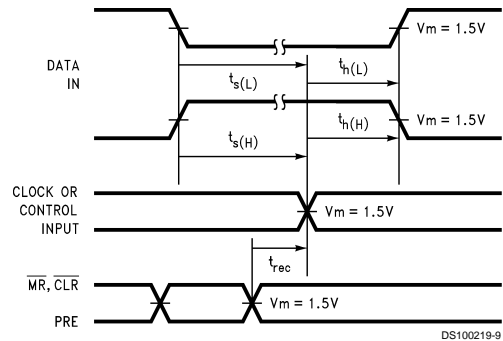
**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 5. Propagation Delay, Pulse Width Waveforms**

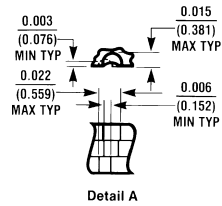
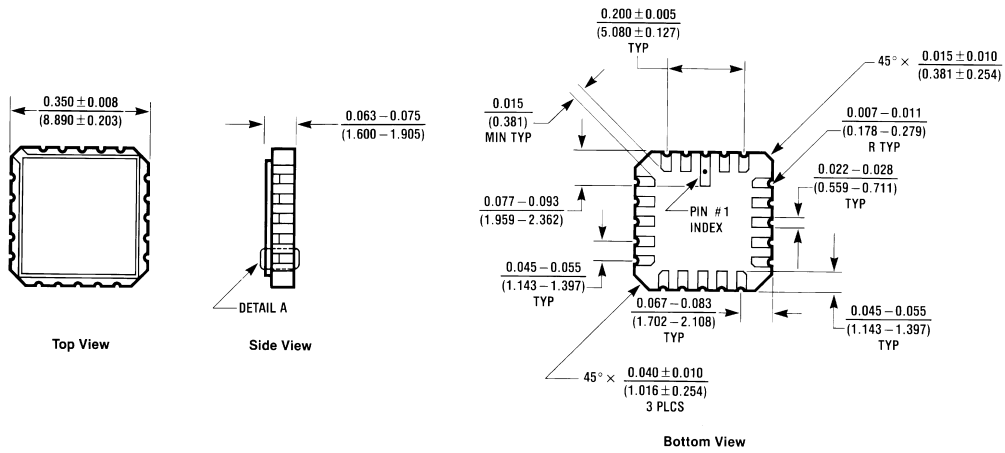


**FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times**



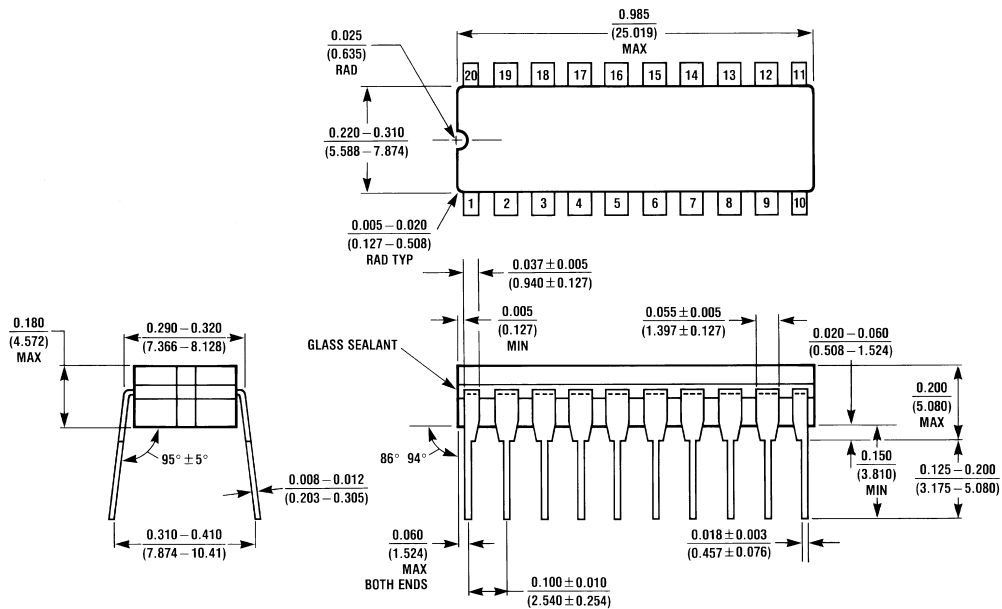
**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

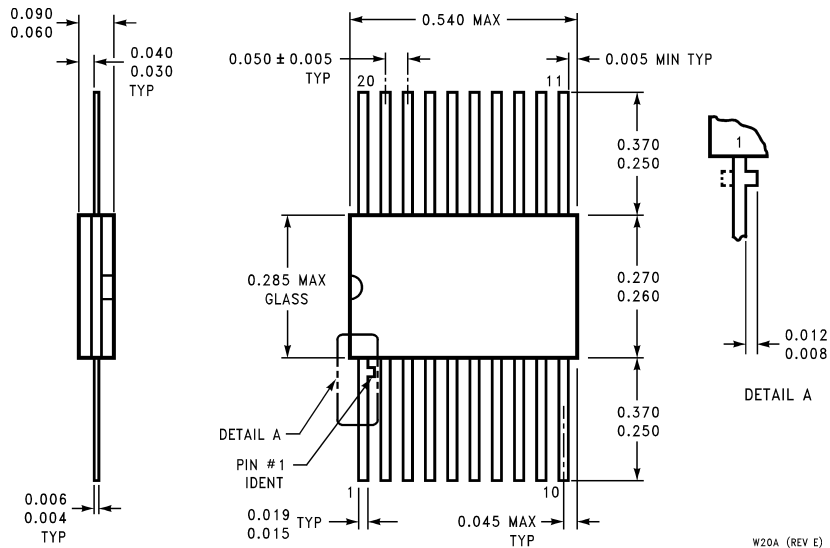
**20-Lead Ceramic Leadless Chip Carrier**  
 NS Package Number E20A



J20A (REV M)

**20-Lead Ceramic Dual-In-Line**  
 NS Package Number J20A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpack  
NS Package Number W20A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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