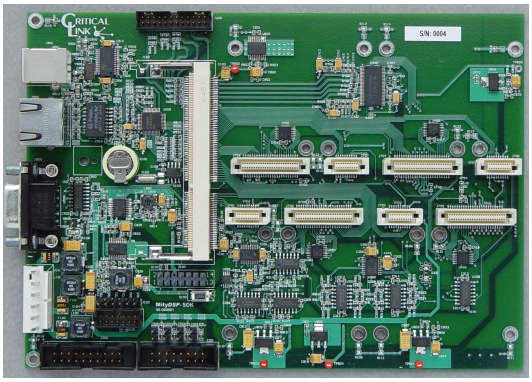
FEATURES

- Standard MityDSP SO-DIMM Interface
- USB Interface
  - 1.2/2.0 Compatible
  - 6 MBit Link Speed
  - Windows Drivers Available
- 10/100 MBit Ethernet Interface
- RS-232 Serial Interface
- 5 High Speed LVDS Pairs
  - Supports Quarter VGA Interface
- 8 On-Board Digital to Analog Converters
  - 12 Bit resolution
  - 1 usec settling time
- 8 On-Board Analog to Digital Converters
  - 12 Bit resolution
  - 200 Ksps sample rate
- Real Time Clock
- Four MDK-4 Daughter Card Expansion Slots
- Four MDK-12 Daughter Card Expansion Slots

APPLICATIONS

- MityDSP Evaluation
- Embedded Instrumentation
- Rapid Prototyping
- Control Processing
- Remote Sensing
- Embedded Signal Processing



DESCRIPTION

The MityDSP Development Kit Motherboard (MDK-MB) provides a low-cost target platform for integration and development using the MityDSP based family of Processor Cards. The MDK-MB is fully compatible with MityDSP and MityDSP-XM processor cards with Bank 7 configured in LVDS mode. The MDK-MB includes on board RS-232, 10/100 MBit Ethernet and Universal Serial Bus (USB) communications interfaces. For display, a quarter VGA (QGVA) display controller with backlight driver is provided. For basic data acquisition and control, an 8 channel 12-bit DAC and an 8 channel 12-bit ADC is included.

In addition to the on-board I/O interfaces, the MDK-MB provides interfaces for four MityDSP Development Kit (MDK) MDK-8 and four MDK-4 form factor daughter card sites for system expansion. The daughter card sites are laid-out to also allow the use of MDK-12, MDK-16, and MDK-24 size daughter cards by combining card slots as described in the Daughter Card Configuration section, below. The MDK daughter cards allow customization of the system card based on the application. Users may select from several off-the-shelf cards available from Critical Link or design their own based on their specific requirements.

The MDK-MB provides on board voltage regulation for provided digital and analog circuits. The card requires a power supply capable of providing a nominal +5 and ±15 Volts DC. The MDK-MB is intended to be run from typical off-the-shelf switch-mode power supplies such as the Mean Well® Q-60C DC power supply.

A block diagram of the MDK-MB is illustrated in Figure 1. All available FPGA I/O lines and the two 6711 McBSP ports are either used directly by the MDK-MB or are routed to the MDK daughter card sites. Control of the on-board interface hardware and connected daughter cards require proper configuration of the MityDSP FPGA and DSP. While not required, it is strongly recommended that the MityDSP software and firmware development kit and supplied API be used to manage these interfaces.

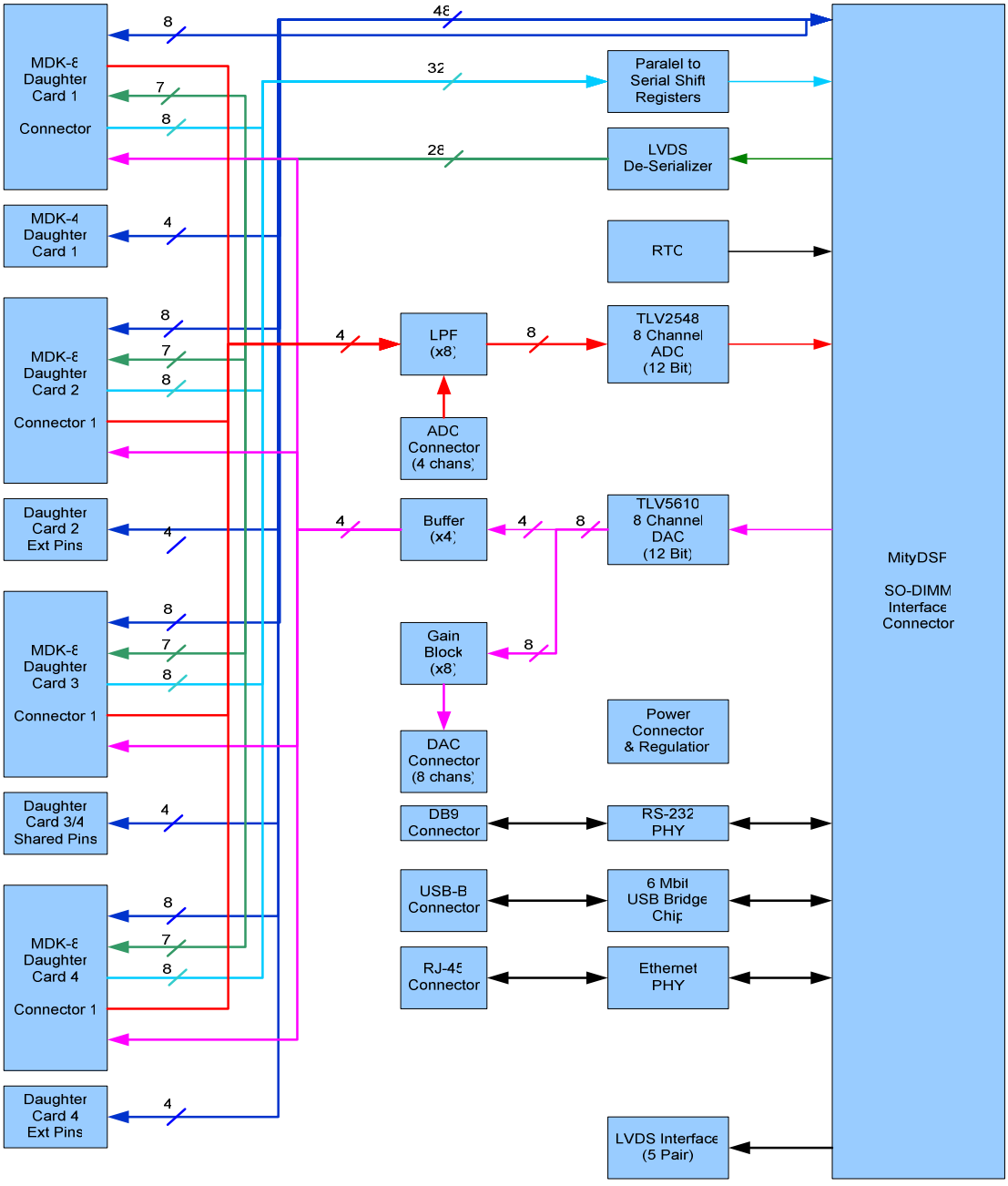


Figure 1 MityDSP Development Kit Block Diagram

RS-232 Interface Description
The on-board RS-232 level driver and DB-9 connector provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the primary MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MityDSP from this connector.

USB Interface Description
The on-board USB interface leverages an asynchronous serial to USB 2.0 compliant bridge chip that supports data rates up to 6 Mbits per second. Drivers for the USB interface are provided with the MityDSP software development kit and are compatible with Windows XP, 2000, and Vista. The USB serial interface is routed to the alternate MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MityDSP from this connector.

Ethernet Interface Description
The on-board Ethernet interface provides a network PHY capable of running at 10/100 Mbit including link auto-negotiation and includes complete MII/MDIO capability. In industry standard RJ-45 connector is provided for external connection. Use of the Ethernet interface requires an Ethernet media access controller implementation in the MityDSP FPGA. The MityDSP hardware and software development kit includes a full tested Ethernet MAC as well as an implementation of the LwIP TCP/IP stack, providing a full Ethernet capable platform ready for integration.

The Ethernet Interface may be used to perform remote code download and FLASH upgrades on an attached MityDSP.

ADC Description
The MDK-MB provides an on-board 8 channel 12-bit analog to digital converter to the MityDSP TI DSP via McBSP port 1. The ADC part is the TLV2548 from Texas Instruments / Burr Brown and is capable of sampling at rates up to 200 Ksps.

All input channels are low-pass filtered using a simple R/C network having a cut-off frequency of TBD Hz. Four of the eight input channels are routed (1 each) to the 4 MDK-8 daughter card slots and provide an input range of 0 to TBD volts. The remaining four ADC input channels are brought to JTBD, an external ADC connector. Each channel input may be configured (via jump and connector pin assignment) to provide a 0-10V input range or a 0-2 volt input range.

For details regarding the signal interface to the MityDSP McBSP port, please refer to the MDK-MB reference schematic. The MityDSP software development kit includes an API for interfacing to the TLV2548.

DAC Description

The MDK-MB provides an on-board 8 channel 12-bit digital to analog converter to the MityDSP TI DSP via McBSP port 2. The DAC part is the TLV5610 from Texas Instruments / Burr Brown and is capable of output settling times of 2 usec.

All output channels are buffered and provide an output impedance of less than TBD ohms. All eight channels are routed to the external DAC connector and provide a voltage output range of 0 to 10 Volts.

Four of eight channels are also independently buffered and routed (1 each) to the 4 MDK-8 daughter card slots and provide an output range of 0 to 4.096 Volts. Note: These 4 DAC outputs are effectively shared between the MDK-8 daughter card slots and the external connector. Use of an MDK-8 (or larger form factor cards in an MDK-8 slot) cards that require the use an associated DAC line implies that the corresponding pin on the external DAC connector should not be used. Please refer to the data sheet for a specific daughter card in order to determine if the DAC slot is required.

For details regarding the signal interface to the MityDSP McBSP port, please refer to the MDK-MB reference schematic. The MityDSP software development kit includes an API for interfacing to the TLV5610.

Real Time Clock Description

The MDK-MB provides a real-time clock using an I2C device with part number M41T81SM6F. Use of the RTC requires an implementation of an I2C driver interface within the FPGA of the MityDSP. The MityDSP software development kit includes an API for interfacing to the M41T81SM6F.

For details regarding the signal interface to the MityDSP I/O pins, please refer to the MDK-MB reference schematic.

LVDS Interface Description

The MDK-MB provides a flat-ribbon cable low profile interface for five Low Voltage Differential Signaling (LVDS) pairs. The interface design is intended to support high speed off board interconnects. In addition to custom user interfacing, the pairs may be used to interface to a Quarter VGA LCD screen using the MityDSP hardware and software development kit LCD interface libraries and an appropriate daughterboard interface. Off-the-shelf display solutions for QVGA interfaces are provided by Critical Link.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vsp	16 V
Maximum Supply Voltage, Vsd	5.3 V
Minimum Supply Voltage, Vsn	-15.5 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Power Dissipation					
Vsp	Voltage supply, positive 15 volt input.		15	14.5/15.5	Volts (Min/Max)
Vsd	Voltage supply, digital/5 volt input.		5	4.8/5.3	Volts (Min/Max)
Vsn	Voltage supply, negative 15 volt input.		-15	-15.5 / -14.5	Volts (Min/Max)
Isp	Current draw, positive 15 volt input		0.2[2]	1.0	Amps (Max)
Isd	Current draw, positive 5 volt input.		0.5[2]	2.0	Amps (Max)
Isn	Current draw, negative 15 volt input.		0.2[2]	1.0	Amps (Max)
On-Board Analog To Digital Converter					
BW_{ADC}	3 DB Bandwidth Analog to Digital Converter	R/C filtering	10	-	KHz
$V_{Min,ADC-Ext}$	Minimum Analog Input Voltage, External ADC connection.		0	TBD	Volts
$V_{Max,ADC-Ext}$	Maximum Analog Input voltage External ADC connection.		10[1]	TBD	Volts
$V_{Min,ADC-DBC}$	Minimum Analog Input Voltage, MDK-8 Daughter Board ADC Interface.		0	TBD	Volts
$V_{Max,ADC-DBC}$	Maximum Analog Input Voltage, MDK-8 Daughter Board ADC Interface.		2	TBD	Volts
FS_{ADC}	Maximum Sample Rate, ADC			TBD	KHz
$R_{IN,\ ADC-Ext}$	Input Impedence		10	8	KOhms (Min)
On-Board Digital To Analog Converter					
$V_{Min,DAC-Ext}$	Minimum Analog Input Voltage, External DAC connection.		0	-0.2	Volts
$V_{Max,DAC-Ext}$	Maximum Analog Input voltage External DAC connection.		10	10.2	Volts
$V_{Min,DAC-DBC}$	Minimum Analog Input Voltage, MDK-8 Daughter Board DAC Interface.		0	-0.2	Volts

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
$V_{Max,DAC-DBC}$	Maximum Analog Input Voltage, MDK-8 Daughter Board DAC Interface.		4.096	5	Volts
FS_{DAC}	Maximum Output Sample Rate, DAC		2	200	KHz
$R_{out\ DAC-Ext}$	Output Impedence		50	100	Ohms (Max)
MDK-8/12 Digital I/O					
$F_{clk,din}$	Clock Frequency, Digital Inputs		25	25	MHz
$T_{update,din}$	Update period, Digital inputs		1280	1280	ns
$F_{clk,dout}$	Clock Frequency, Digital Output LVDS clk entering deserializer		50	20 / 68	MHz (Min/Max)
$T_{update,dout}$	Update period, digital outputs		20	14.7 / 50	ns (Min/Max)
Notes:	1. 2 Volt External Interface also provided, see description of external ADC interface. 2. Power Supply load is dependent on Daughter Card configuration and utilization. Typical values represent MDK-MB populated with 1 MDK8-ADS8344 Card.				

DAUGHTER CARD CONFIGURATION

The MDK-MB and daughter card system provides a high level of flexibility in configuration in order to maximize the use of the available MityDSP expansion pins. The daughter cards used in the MDK system are sized according to their complexity and number of required I/O pins to the MityDSP. There are several possible form factors: MDK-4, MDK-8, MDK-12, MDK-16, MDK-24, and MDK-48. The primary form factors, however, are the MDK-4 and MDK-8 configurations. All of the other factors listed are simply a combination of these card times.

Figure 2 provides a top view of the MDK-MB circuit card and its corresponding interface connectors. In the figure, the daughter card sites are located on the right hand side of the board. The basic MDK-4 and MDK-8 card connectors are divided evenly into the top half of the card and the bottom half of the card. While this section illustrates configurations for the bottom half of the card, please note that the top half provides similar connectivity.

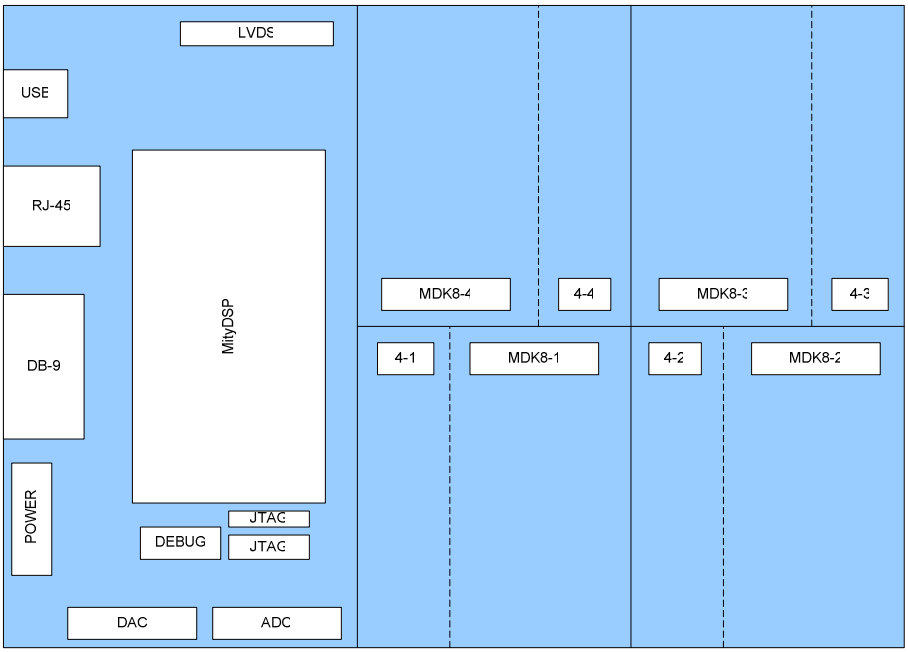


Figure 2 MDK-MB Connector Locations, Top View

Figure 3 illustrates the bottom half of the MDK-MB daughter card expansion area using two each of the MDK-4 and MDK-8 form factor daughter cards. In this configuration, the cards are simply plugged into their corresponding connectors on the board.

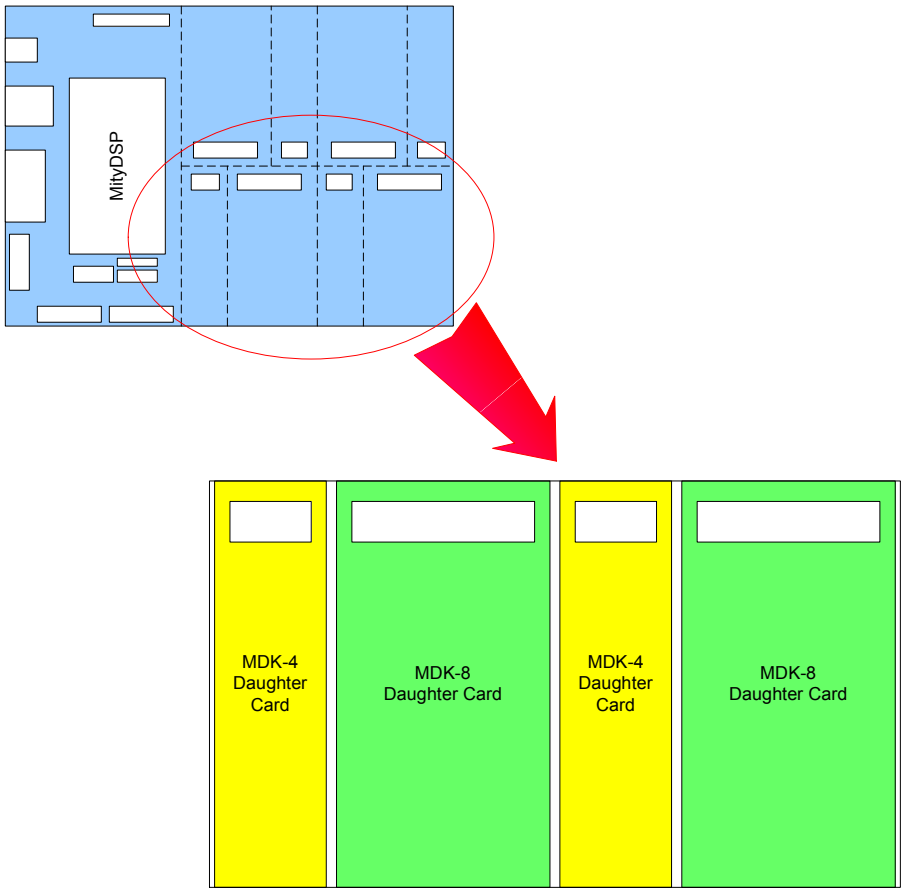


Figure 3 Daughter Card Configuration, 2 MDK-4 and 2 MDK-8 Cards (Top View)

Figure 4 illustrates the use of MDK-12 form factor daughter cards, which occupy one each of the MDK-4 and MDK-8 slot connectors. As is shown in Figure 5, the MDK-12 cards may be mixed and matched with MDK-4 or MDK-8 cards in an MDK-MB configuration. Card slots may be left empty.

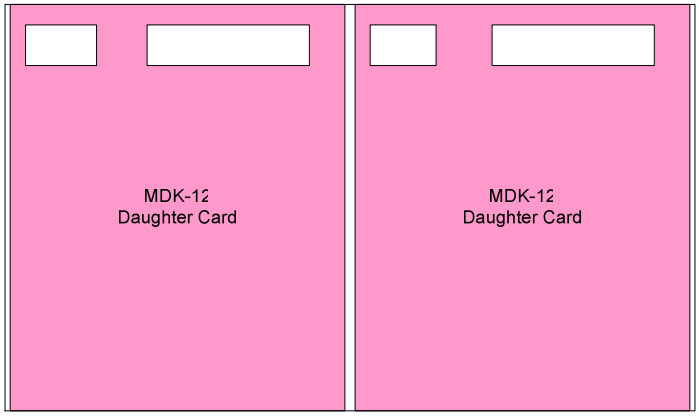


Figure 4 Daughter Card Configuration, 2 MDK-12 Cards (Top View)

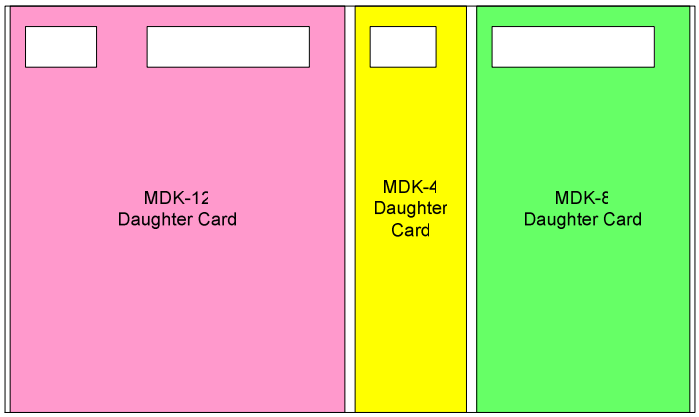


Figure 5 Daughter Card Configuration, 1 each MDK-12, MDK-4, and MDK-8 (Top View)

Use of an MDK-16 Daughter Card requires two MDK-4 slots and an MDK-8 slot as shown in Figure 6.

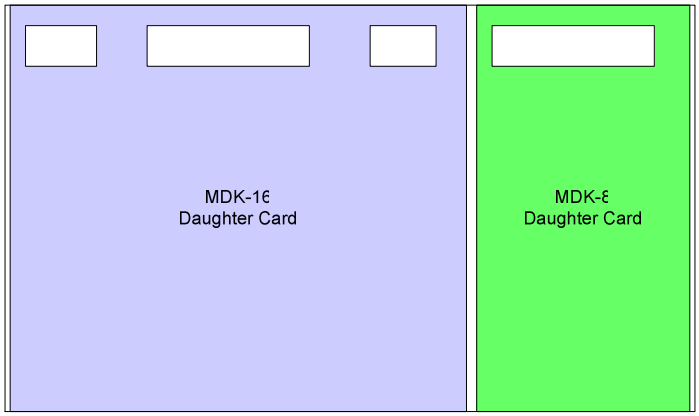


Figure 6 Daughter Card Configuration, MDK-16 and MDK-8 (Top View)

The MD-24 uses two each of the MDK-4 and MDK-8 slots as shown in Figure 7. Similarly (and not shown), an MDK-48 card would use all available slots on the MDK-MB. MDK-48 cards are typically full custom designs.

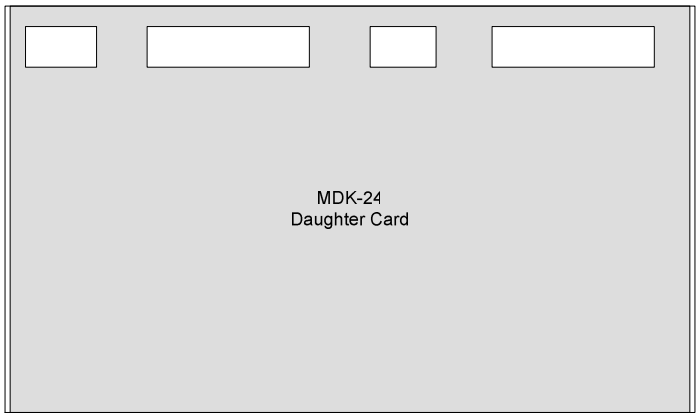


Figure 7 Daughter Card Configuration MDK-24 (Top View)

ELECTRICAL INTERFACE DESCRIPTION

MityDSP JTAG Interface

The MDK-MB provides a standard Spectrum Digital XDS510 keyed interface to the MityDSP TI6711 processor chip on J100. Pinout for the DSP emulator interface connector is shown in Table 1.

Table 1 J100 DSP / Emulator JTAG Connector

Position	Signal	Position	Signal
1	TMS	2	TRST#
3	TDI	4	GND
5	VCC (3.3V)	6	Key
7	TDO	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

The MDK-MB provides a 2.5 V JTAG interface to the MityDSP Spartan FPGA. Two connectors are available supporting the older style 0.100 inch single line Xilinx platform interface cable (J103) as well as the dual row 2 mm connector (J104). Pinouts for these interfaces are described in Table 2 and Table 3.

Table 2 J103 FPGA JTAG Connector

Position	Signal
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	VCC (2.5V)

Table 3 J104 FPGA JTAG Connector

Position	Signal	Position	Signal
1	GND	2	2.5 V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

Input Power

The MDK-MB power interface, J101, requires +5 V and +/- 15 V power supplies. J101 uses a locking Molex style header, and interfaces to a mating connector such as the AMP® TBD (or equivalent). Pinout for the power interface is included in Table 4.

Table 4 J101 Input Power Interface Pin Description

Signal	Position	Type	Standard	Notes
Vsp	1	I	15V	Input Voltage Supply, positive rail.
Vsd	2 3	-	-	Input Voltage Supply, 5 Volt / Logic rail.
GND	4 5	I	Ground	Power Supply Ground / Return.
Vsn	6	I	-15V	Input Voltage Supply, negative rail.

Analog I/O Connectors

The MDK-MB provides two 2 mm two-row shrouded connectors for the on-board DAC circuit outputs and the on board ADC connectors. Table 5 defines the DAC external interface connectors. A cable using AMP® connector TBD (or equivalent) should be used. Note that the first four DAC outputs are also shared with the MDK-8 daughter card positions. MDK-8 cards that require use of the DACs preclude the use of the external interface DAC position.

Table 5 J200 On-Board DAC External Interface Connector

Pin	Signal	Notes	Pin	Signal
1	DAC_1	0-10 V, Shared with MDK-8 Daughter Board 1	2	AGND
3	DAC_2	0-10 V, Shared with MDK-8 Daughter Board 2	4	AGND
5	DAC_3	0-10 V, Shared with MDK-8 Daughter Board 3	6	AGND
7	DAC_4	0-10 V, Shared with MDK-8 Daughter Board 4	8	AGND
9	DAC_5	0-10 V, Shared with MDK-4 Daughter Board 1	10	AGND
11	DAC_6	0-10 V, Shared with MDK-4 Daughter Board 2	12	AGND
13	DAC_7	0-10 V, Shared with MDK-4 Daughter Board 3	14	AGND
15	DAC_8	0-10 V, Shared with MDK-4 Daughter Board 4	16	AGND

Table 6 defines the ADC external interface connectors. A cable using AMP® connector TBD (or equivalent) should be used. Note that each of the four external ADC signals can be configured to use a 0-10V input voltage range or a 0-2V input range by selecting the proper pin position and populating one of the jumps as specified in the Notes column.

Table 6 J301 On-Board ADC External Interface Connector

Pin	Signal	Notes	Pin	Signal	Notes
1	ADC_1	1 0-10V, Populate J300	2	ADC_1	0-2V, De-Populate J300
3	ADC_2	1 0-10V, Populate J302	4	ADC_2	0-2V, De-Populate J302
5	ADC_3	1 0-10V, Populate J303	6	ADC_3	0-2V, De-Populate J303
7	ADC_4	1 0-10V, Populate J304	8	ADC_4	0-2V, De-Populate J304
9	GND		10	GND	
11	GND		12	GND	
13	GND		14	GND	

LVDS Interface

The LVDS interface connector provides up to 5 pairs of LVDS signals connected to the Spartan 3 device on a connected MityDSP. The interfaces uses a standard 2 mm 24 position male header. Table 7 defines the LVDS connector pinout. A cable using AMP® TBD connector (or equivalent) should be used. Use of the LVDS pairs as outputs will require addition of termination resistors (100 Ohm) on externally designed circuit assemblies. Use of the LVDS pairs as inputs will require population of 0402 sized termination resistors on the MDK-MB on the provided solder pads. Refer to the detailed schematic and assembly drawing for further information.

Table 7 JTBD LVDS Interface Pin Description

Signal	Position	Type	Standard	Notes
+15 V	1	-	-	Max 200 mA [TBC]
3.3 V	2	-	-	Max 100 mA [TBC]
GND	3	-	-	
GND	4	-	-	
LVDS_4P	5	I/O	LVDS	
LVDS_4N	6	I/O	LVDS	
GND	7	-	-	
GND	8	-	-	
LVDS_3P	9	I/O	LVDS	
LVDS_3N	10	I/O	LVDS	
GND	11	-	-	
GND	12	-	-	
LVDS_2P	13	I/O	LVDS	
LVDS_2N	14	I/O	LVDS	
GND	15	-	-	
GND	16	-	-	
LVDS_1P	17	I/O	LVDS	
LVDS_1N	18	I/O	LVDS	
GND	19	-	-	
GND	20	-	-	
LVDS_0P	21	I/O	LVDS	
LVDS_0N	22	I/O	LVDS	
GND	23	-	-	
GND	24	-	-	

MDK-8 Daughter Card Interface

The MDK-MB provides 4 MDK-8 Daughter Card interface positions. Each position includes one 50 position dual row sockets. Mating connectors for these sockets are the Hirose FX6-50P-0.8SV plugs. Table 8 defines the signals on each pin for the cards. Table 10 provides the electrical standards for the various nets.

Table 8 Daughter Card – MDK-8 Connector Pin Assignments

Pin	Signal	Pin	Signal
A1	IO_0	B1	+5 V
A2	IO_1	B2	+5 V
A3	IO_2	B3	+3.3 V
A4	IO_3	B4	+3.3 V
A5	IO_4	B5	+12 VA
A6	IO_5	B6	GND
A7	IO_6	B7	GND
A8	IO_7	B8	GND
A9	DO_0	B9	-12 VA
A10	DO_1	B10	+15 V
A11	DO_2	B11	+15 V
A12	DO_3	B12	-15 V
A13	DO_4	B13	-15 V
A14	DO_5	B14	AGND
A15	DO_6	B15	AGND
A16	DI_0	B16	DO_CLK
A17	DI_1	B17	RSV
A18	DI_2	B18	RSV
A19	DI_3	B19	RSV
A20	DI_4	B20	RSV
A21	DI_5	B21	RSV
A22	DI_6	B22	RSV
A23	DI_7	B23	RSV
A24	ADC	B24	RSV
A25	DAC	B25	RSV

MDK-4 Daughter Card Interface

The MDK-MB provides 4 MDK-4 Daughter Card interface positions. Each position includes one 20 position dual row socket. Mating connectors for these sockets are the Hirose FX6-20P-0.8SV plugs. Table 9 describes the interface connectors for the connector.

Table 9 Daughter Card MDK-4 Connector Assignments

Pin	Signal	Pin	Signal
A1	IO_0	B1	+5V
A2	IO_1	B2	+5V
A3	IO_2	B3	+3.3V
A4	IO_3	B4	+3.3V
A5	+15 V	B5	GND
A6	+15 V	B6	GND
A7	DAC	B7	RSV
A8	AGND	B8	RSV
A9	RSV	B9	RSV
A10	RSV	B10	RSV

Daughter Card Signal Description

Table 10 Daughter Card Signal Description

Signal	Type	Standard	Notes
IO_##	I/O	3.3V CMOS	Direct Interface to MityDSP Spartan FPGA.
DO_##	O	3.3V CMOS	Digital Output. Update Rate of TBD usec. DO_CLK provides sampling clock – outputs should be sampled on rising edge.
DI_##	I	3.3V CMOS	Digital Input. Sampling interval < 2 usec.
DAC_1 DAC_2 DAC_3 DAC_4	O	0-4.096 V	12 Bit.
ADC_1 ADC_2 ADC_3 ADC_4	I	0-2 V	12 Bit. 10 Khz R/C filtering.

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

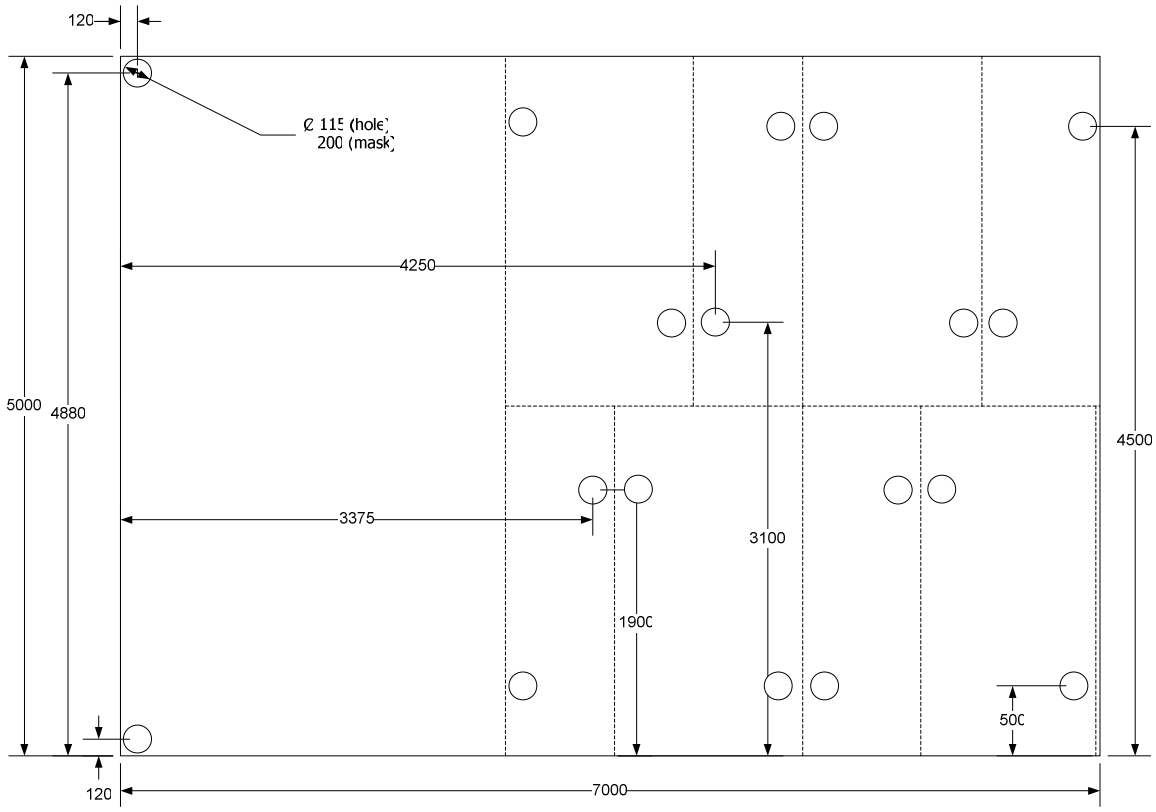


Figure 8 MDK-MB PCB Outline and Mounting Hole Locations (Top View, mils)

Daughter Card Interface / Mounting

Mechanical outlines for each of the MDK-4 and MDK-8 form factors are shown in Figure 9 and Figure 10, respectively. For larger MDK-12, MDK-16, and MDK-24 form factors, a 1/8th inch gap (125 mils) is required between each of the board outlines. Figure 12 illustrates and MDK-16 form factor board with the necessary spacing.

In the vertical dimension, the base board to board spacing is 7 mm. The MDK-MB includes components underneath the area used by the MDK daughter boards. 4.5 mm has been reserved for use by these components. Therefore, MDK daughter boards must be designed requiring no more than 2.5 mm of clearance for bottom side mounted components. This is illustrated in Figure 13.

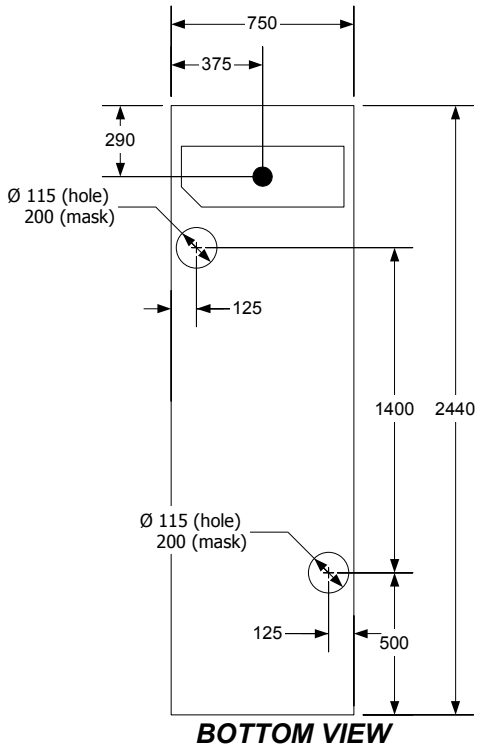


Figure 9 MDK-4 Mounting Hole, Size, and Hirose Connector location (units in mils)

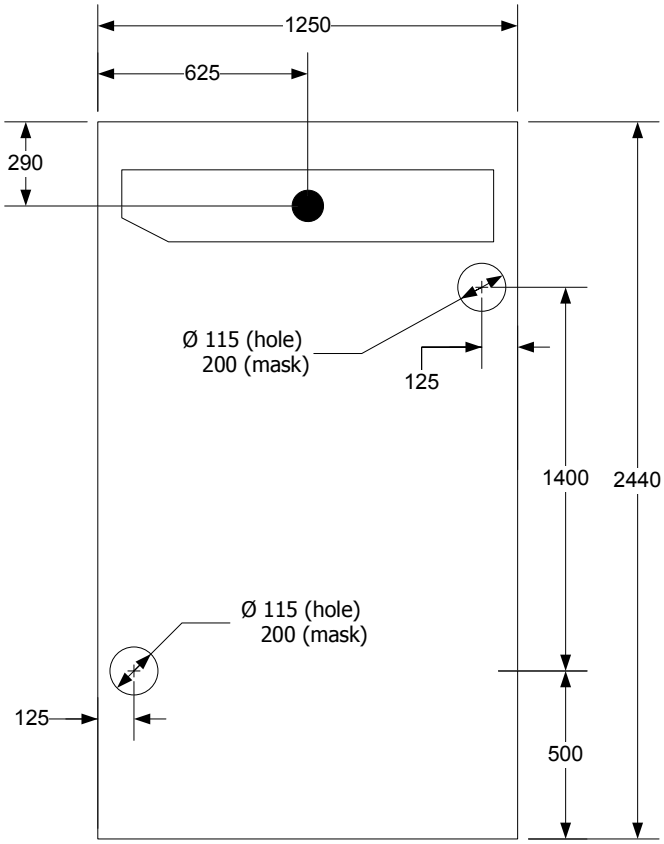
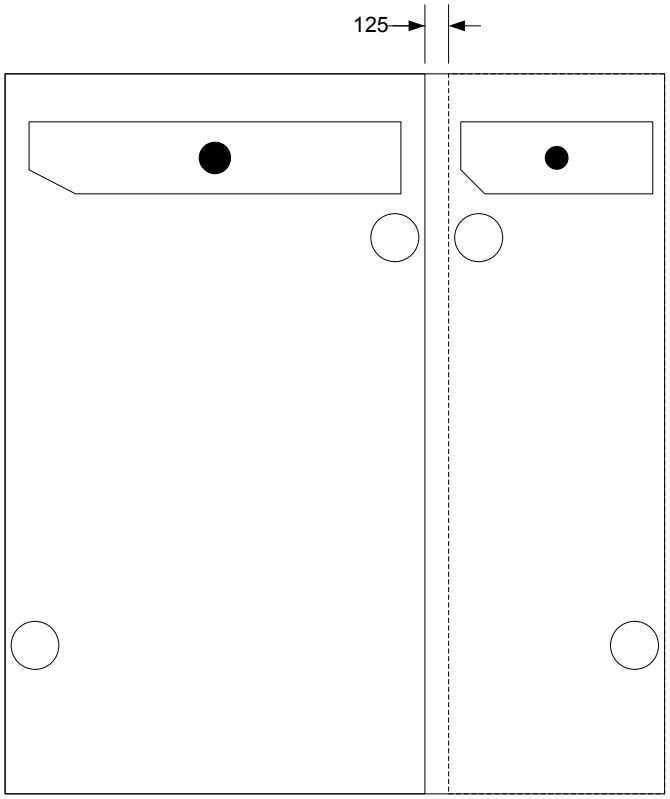
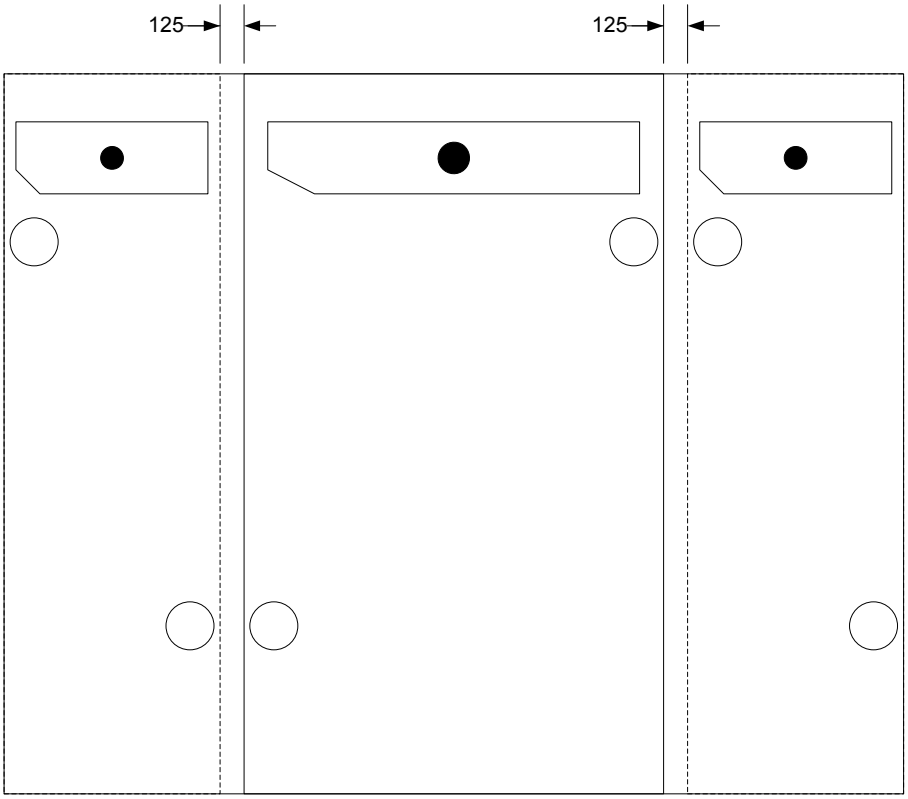


Figure 10 MDK-8 Mounting Hole, Size, and Hirose Connector location (units in mils)



BOTTOM VIEW

Figure 11 MDK-12 Alignment (MDK-4 and MDK-8 footprints separated by 125 mils)



BOTTOM VIEW

Figure 12 MDK-16 Alignment (MDK-4 and MDK-8 footprints separated by 125 mils)

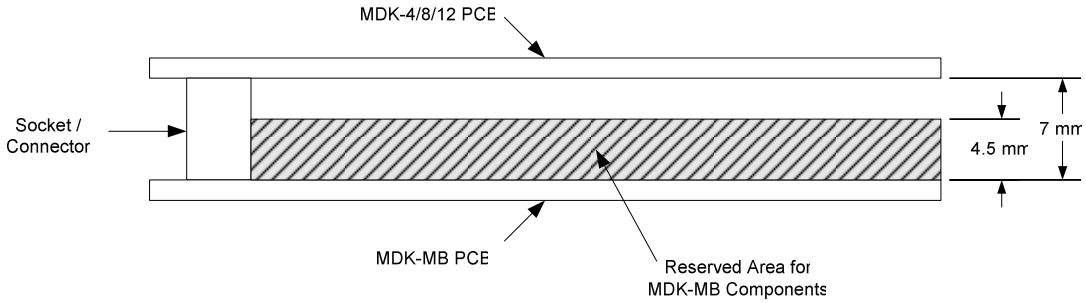


Figure 13 Required Bottom Clearance, MDK board designs

MityDSP Interface

Table 11 MityDSP/SO-DIMM Connector Assignments

Pin	Signal	Pin	Pin	Signal	Pin	Signal	Signal
A1		A37		B1		B37	
A2		A38		B2		B38	
A3		A39		B3		B39	
A4		A40		B4		B40	
A5		A41		B5		B41	
A6		A42		B6		B42	
A7		A43		B7		B43	
A8		A44		B8		B44	
A9		A45		B9		B45	
A10		A46		B10		B46	
A11		A47		B11		B47	
A12		A48		B12		B48	
A13		A49		B13		B49	
A14		A50		B14		B50	
A15		A51		B15		B51	
A16		A52		B16		B52	
A17		A53		B17		B53	
A18		A54		B18		B54	
A19		A55		B19		B55	
A20		A56		B20		B56	
A21		A57		B21		B57	
A22		A58		B22		B58	
A23		A59		B23		B59	
A24		A60		B24		B60	
A25		A61		B25		B61	
A26		A62		B26		B62	
A27		A63		B27		B63	
A28		A64		B28		B64	
A29		A65		B29		B65	
A30		A66		B30		B66	
A31		A67		B31		B67	
A32		A68		B32		B68	
A33		A69		B33		B69	
A34		A70		B34		B70	
A35		A71		B35		B71	
A36		A72		B36		B72	

MDK Interface Cards

Table 12 MDK Off-The-Shelf Interface Cards (see www.mitydsp.com for latest list)

Card Number	Description / Features	MDK-4	MDK-8	MDK-12	MDK-16	MDK-24	Other
MDK4-RS232	RS-232 Interface Card w/hardware flow control lines, no modem control or dual RS-232 Interface with no flow control.	X					
MDK4-RS485	RS-485 Interface Card supporting 2 outputs and 2 input signaling lines.	X					
MDK4-SD	SD-FLASH interface card controller, SPIO mode.	X					
MDK4-TSA	Touch Screen Adaptor	X					
MDK8-ADS8239	1 Msps 16 bit Analog to Digital Converter utilizing ADS8239.		X				
MDK8-ADS8344	8 channel 16 bit 100 Msps Analog to Digital Converter utilizing ADS8344.		X				
MDK8-DIGIOISO	TTL Discrete Input/Output Interface Card, isolated inputs/outputs.		X				
MDK8-A3967	Independent dual axis stepper motor controller, micro-stepping down to 1/8 step size.		X				
MDK12-TTLIO	TTL Discrete Input/Output Interface Card			X			
MDK16-AWG	Analog Waveform Generator, dual summed 14 bit DACs, 100 Msps.				X		
MDK-QVGA-TBD	Quarter VGA LVDS Display Adaptor, LCD part number TBD						X