LatticeXP2 Family

Instant-On, Secure, Single-Chip FPGA with Complete Development Platform

LatticeXP2™ is an instant-on, secure, small-form-factor FPGA with a versatile development platform for quick launch of design initiatives and rapid time-to-market.

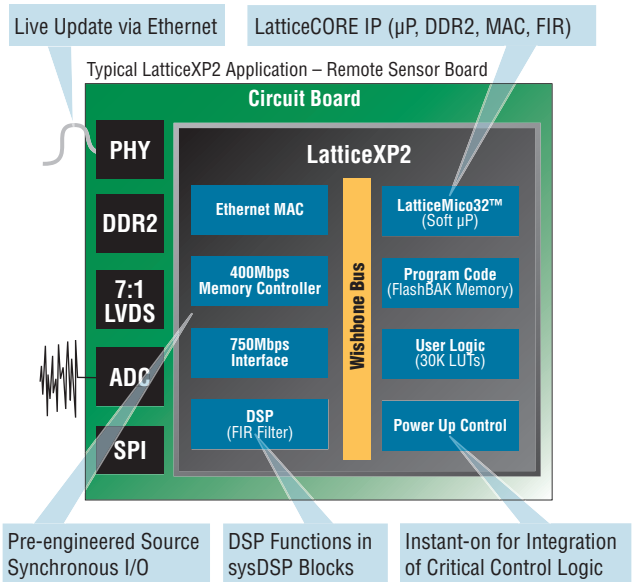
LatticeXP2 offers twice as many logic and signal processing resources for seamless design upgrades from highly popular MachXO devices. The high-speed 7:1 LVDS interface enables rapid image data transfer in video applications. The LatticeMico32™ soft processor allows the LatticeXP2 to be used even as a microcontroller.

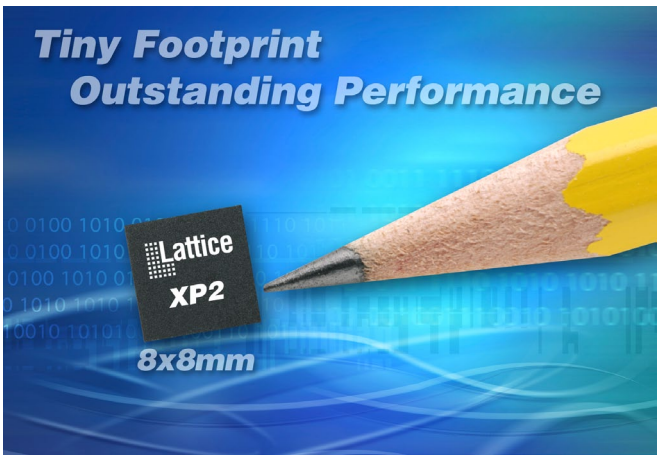
LatticeXP2 devices are based on Lattice's unique flexiFLASH™ architecture that combines a 4-input Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells for on-chip storage of design data. The flexiFLASH architecture provides distributed and embedded memory, enhanced sysDSP™ blocks, Phase Locked Loops (PLLs), pre-engineered source synchronous I/Os. The versatile I/Os support DDR/DDR2 & 7:1 LVDS.

In addition, the LatticeXP2 devices have access to general-purpose Serial TAG memory, inherent design security, 128-bit AES bitstream encryption, Live Update field reconfiguration with TransFR™, and Dual Boot technologies.

The Lattice ispLEVER® design tool allows complex designs to be efficiently implemented using the LatticeXP2 family of FPGAs. The ispLEVER tool is complemented by pre-designed IP (Intellectual Property) modules for the LatticeXP2 family. By using these standardized IP blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Complete Non-Volatile System-on-Chip





Key Features and Benefits

- **flexiFLASH Architecture**
  - Instant-on (1ms), single chip integration
  - High logic-to-I/O ratio
  - Embedded & distributed memory
  - Flexible, high performance I/Os
- **Live Update Technology**
  - TransFR technology – update logic configuration while equipment continues to operate
  - Dual Boot with external SPI Flash improves reliability
  - Secure updates with 128 bit AES bitstream encryption
- **Optimized FPGA Architecture**
  - Densities from 5K to 40K 4-input Look-up Tables (LUTs)
  - Up to 885 Kbits sysMEM™ block RAM
  - Up to 83 Kbits distributed RAM
  - Low cost TQFP, PQFP and BGA packaging
- **High Performance sysDSP Block**
  - Three to eight blocks with multiply and accumulate
  - 12 to 32 18x18 multipliers
- **Flexible sysIO™ Buffer Supports:**
  - LVCMOS 3.3/2.5/1.8/1.5/1.2; LVTTL
  - SSTL 18 class I, II; SSTL 3/2 class I, II
  - HSTL15 class I; HSTL18 class I, II
  - PCI
  - LVDS, Bus-LVDS, LVPECL
- **Pre-engineered Source Synchronous Interfaces**
  - DDR / DDR2 up to 200MHz/400Mbps
  - 7:1 LVDS up to 600Mbps
  - Generic up to 750Mbps
- **Up to 4 sysCLOCK™ PLLs**
- **System Level Support**
  - SPI/JTAG interface for device programming
  - IEEE Standard 1149.1 Boundary Scan
  - On-board oscillator for initialization & general use
  - Soft Error Detect (SED) logic
  - 1.2V power supply core voltage

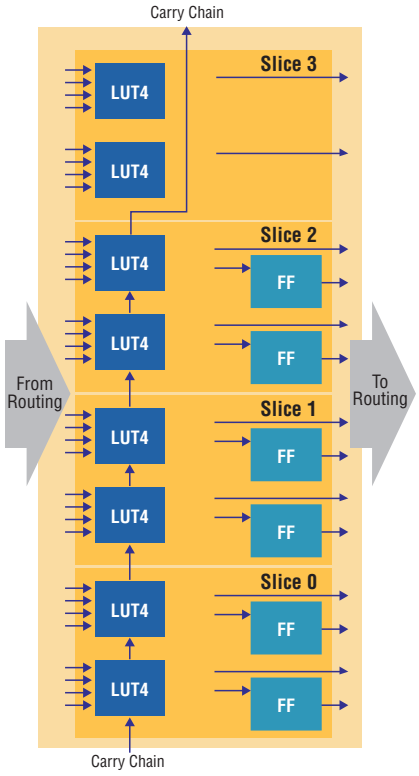
LatticeXP2 Architecture

Architecture Overview

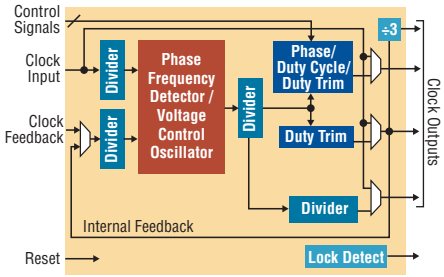
LatticeXP2 FPGAs combine on-chip Flash memory with SRAM programmable LUTs and interconnect to provide an optimized low cost architecture that delivers high performance sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers, and more.

LatticeXP2 FPGAs offer the best of both worlds, with the instant-on, non-volatility of Flash and the reconfigurability of SRAM – all in one chip.

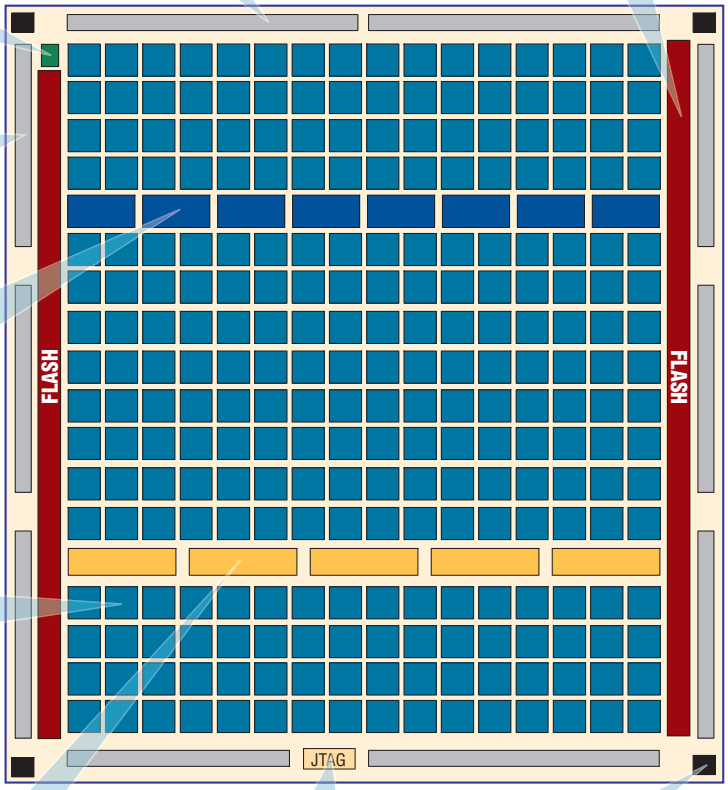
PFU BLOCK DIAGRAM



sysCLOCK PLL BLOCK DIAGRAM



LatticeXP2 Block Diagram



Pre-Engineered Source Synchronous I/O supports DDR/DDR2 & 7:1 LVDS.

flexiFLASH architecture offers a secure, instant-on, single chip solution.

On-chip Oscillator

sysIO Buffers support LVCMOS, HSTL, SSTL, LVDS, and more.

sysMEM Embedded Block RAM (EBR) provides up to 885 Kbits with speeds up to 350MHz.

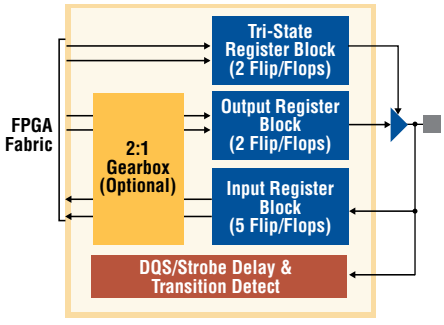
Programmable Function Units (PFUs) provide up to 40K LUTs and speeds up to 350MHz.

sysDSP Blocks include multiply and accumulate, up to 32 18x18 multipliers, and speeds up to 325MHz.

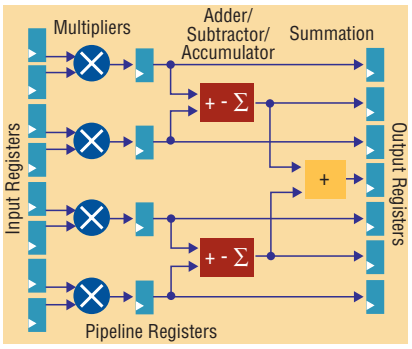
JTAG and SPI Ports with **Live Update** technology.

sysCLOCK PLLs for clock management. Up to 4 per device.

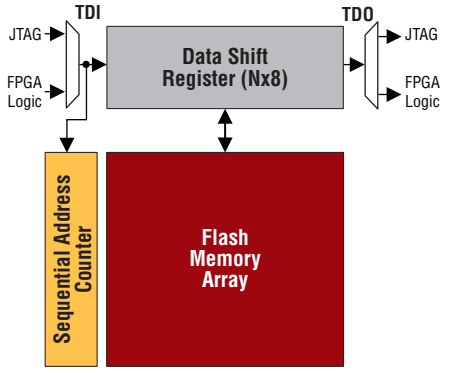
sysIO BLOCK DIAGRAM



sysDSP BLOCK DIAGRAM



Serial TAG Memory



Brevia Development Kit

Introduction

The LatticeXP2 Brevia Development Kit is an easy-to-use, low-cost platform for evaluating and designing with LatticeXP2 FPGAs. The kit offers free design tools, reference designs, readymade SoC demos, and a small form factor evaluation board with LatticeXP2 LFXP2-5E device.

ispLEVER Starter Development Tools FREE

Lattice's free ispLEVER development tools offer a comprehensive design environment for the LatticeXP2 architecture. It includes tools for design entry, synthesis, map, place & route, I/O planning, simulation, and device programming. Download ispLever Starter at: www.latticesemi.com/products/designsoftware/isplever/ispleverstarter

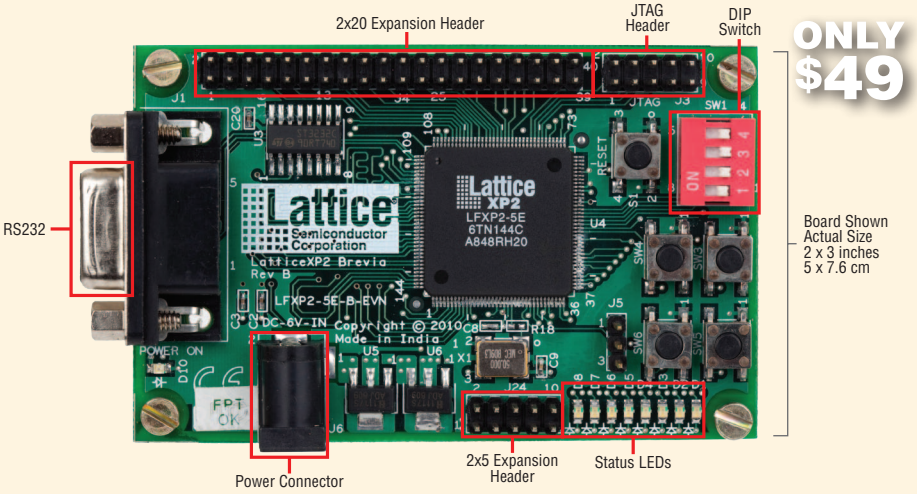
Reference Designs FREE

Lattice offers an expanding portfolio of IP cores and reference designs. Optimized for the LatticeXP2 architecture, available reference designs include popular protocol and connectivity standards such as I²C, SPI, UART, and PCI. The reference designs, source codes, and documentation can be downloaded free from the Lattice website. For more information, please go to www.latticesemi.com/ip.

Quick Time-to-Market with Brevia SoC Designs FREE

The Brevia evaluation board comes with LatticeXP2 FPGA pre-programmed with a comprehensive system-on-chip (Brevia SoC). The Brevia SoC demo integrates multiple Lattice reference designs including the LatticeMico8™ (LM8) microcontroller, WISHBONE interconnect, and peripheral controllers for SPI and SRAM. The board can be controlled with switches and a menu-driven interface via a Windows or Linux terminal program over an RS-232/USB link. For complete documentation on the Brevia Development Kit, please go to www.latticesemi.com/latticexp2-brevia.

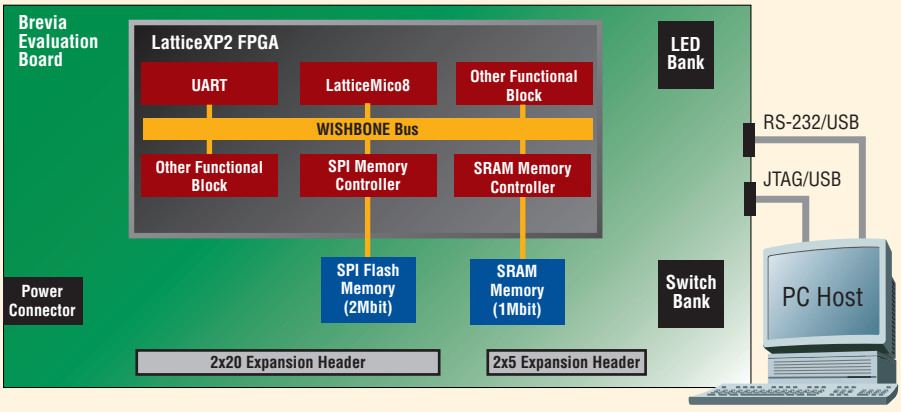
LatticeXP2 Brevia Evaluation Board – Top View



Key Features

- LatticeXP2 LFXP2-5E-6TN144C Device
- 2 Mb SPI Flash
- 1 Mb SRAM Memory
- Programmed via Standard Parallel or USB Cable
- RS-232 Interface
- JTAG Interface
- 2x20 and 2X5 Expansion Headers
- Push-buttons for General Purpose I/O and Reset
- 4-bit DIP Switch
- 8 Status LEDs
- QuickSTART Guide
- Marked for CE, China RoHS Environment-Friendly Use Period (EFUP) and Waste Electrical and Electronic Equipment (WEEE) Directives

Brevia Evaluation Board Block Diagram

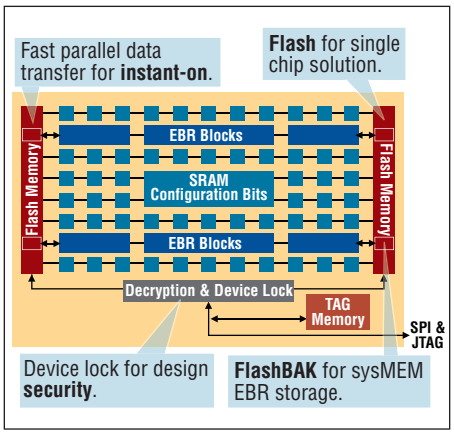


Ordering Information

Product	Description	Ordering Part #
LatticeXP2 Brevia Development Kit	LatticeXP2 Brevia Evaluation Board with LFXP2-5E-6TN144C device, parallel cables, QuickSTART Guide, and demonstration design	LFXP2-5E-B-EVN

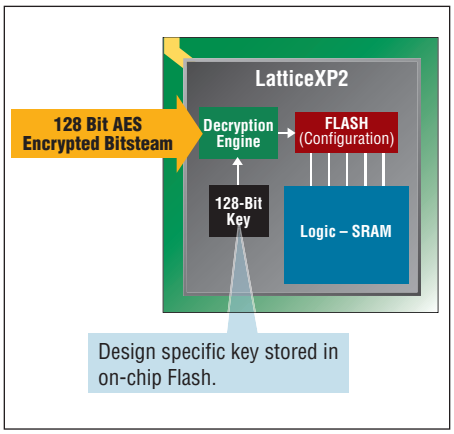
Advantages of the LatticeXP2 Platform

flexiFLASH Architecture



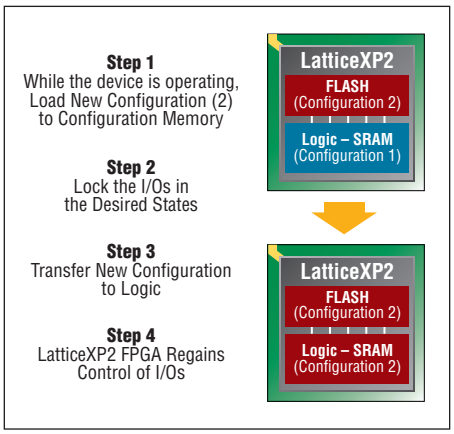
Instant-on (1ms), small-form-factor chip with support for high-speed 7:1 LVDS (840 Mbps) interface.

128-Bit AES Bitstream Encryption



Design security ensured by a robust 128-bit AES bitstream encryption and design-specific key.

TransFR Technology



TransFR technology enables the LatticeXP2 FPGAs to be re-programmed while your system continues to operate.

Device Selection Guide

Parameter	LFXP2-5	LFXP2-8	LFXP2-17	LFXP2-30	LFXP2-40
LUTs (K)	5	8	17	29	40
sysMEM EBR RAM Blocks	9	12	15	21	48
Embedded Memory (Kbits)	166	221	276	387	885
Distributed Memory (Kbits)	10	18	35	56	83
sysDSP Blocks	3	4	5	7	8
Number of 18x18 Multipliers	12	16	20	28	32
Number of PLLs	2	2	4	4	4
Vcc Voltage (V)	1.2	1.2	1.2	1.2	1.2
Packages & I/O Combinations					
132-ball csBGA (8 x 8 mm)[1]	86	86			
144-pin TQFP (20 x 20 mm)[1]	100	100			
208-pin PQFP (28 x 28 mm)[1]	146	146	146		
256-ball ftBGA (17 x 17 mm)[1]	172	201	201	201	
484-ball fpBGA (23 x 23 mm)			358	363	363
672-ball fpBGA (27 x 27 mm)				472	540

1. Available as automotive temperature range-qualified packages, except for LatticeXP2-30. All packages are available in standard commercial or industrial temperature ranges.

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Lattice Semiconductor Corporation

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