AN3392
Application note

Designing with SPV1020, interleaved boost converter with MPPT algorithm

Introduction

SPV1020 is a monolithic DC-DC boost converter designed to maximize the power generated by photovoltaic panels independently of temperature and amount of solar radiation. The optimization of the power conversion is obtained with an embedded logic which performs the MPPT (max power point tracking) algorithm on the PV cells connected to the converter.

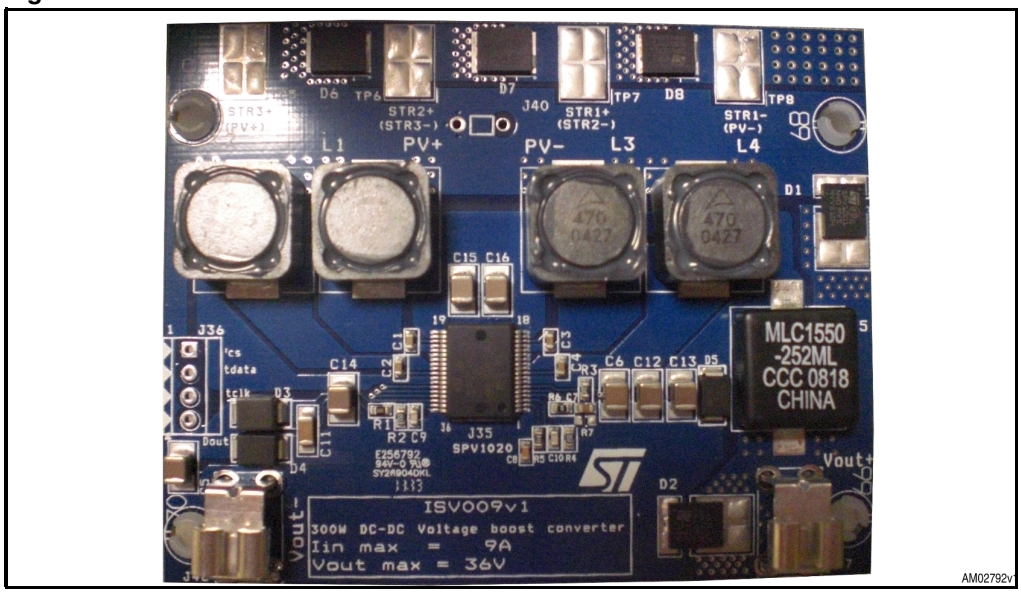
One or more converters can be housed in the connection box of PV panels, replacing the bypass diodes, and thanks to the fact that the maximum power point is locally computed, the efficiency at system level will be higher than the one of conventional topologies, where the MPP is computed in the main centralized inverter.

For a cost effective application solution and miniaturization needs, SPV1020 embeds the power MOSFETs for active switches and synchronous rectification, minimizing the number of external devices. Furthermore, the 4 phase interleaved topology of the DC-DC converter allows to avoid the use electrolytic capacitors, which would severely limit the lifetime.

It works at fixed frequency in PWM mode, where the duty cycle is controlled by the embedded logic running a Perturb&Observe MPPT algorithm. The switching frequency, internally generated and set by default at 100 kHz, is externally tunable, while the duty cycle can range from 5% to 90% with a step of 0.2%.

Safety of the application is guaranteed by stopping the drivers in case of output over-voltage or overtemperature.

Figure 1. ISV009v1 demonstration board



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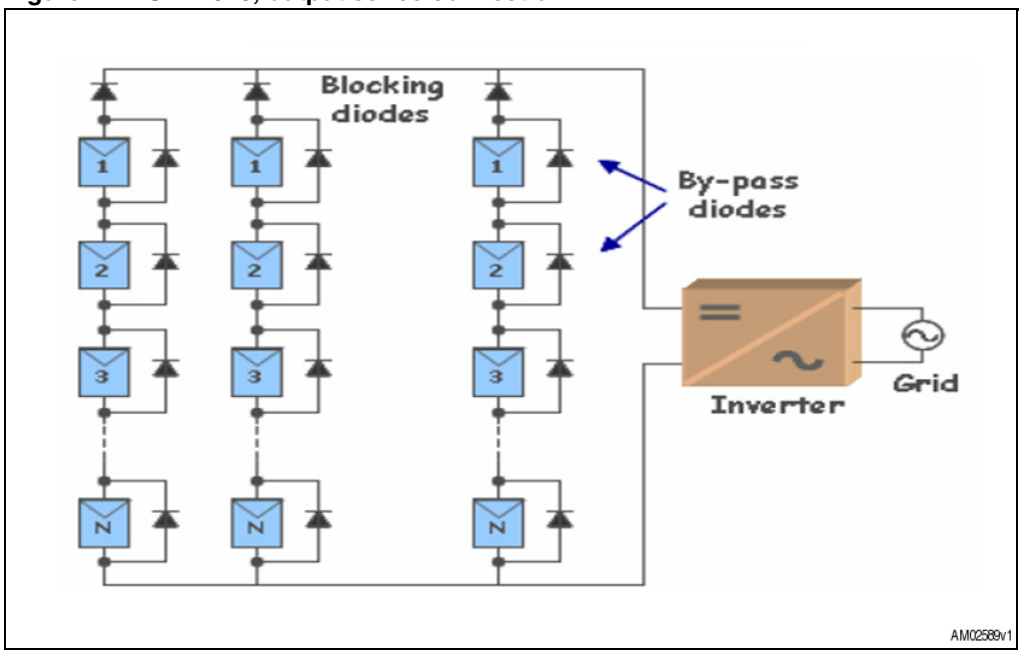
1 Application overview

Following picture shows the typical architecture of a photovoltaic system for grid connected application and composed by the photovoltaic field and the electronic part:

Figure 2. SPV1020, output series connection



Photovoltaic field is composed by PV panels. Some PV panels are connected in series to make a PV string. Each string is connected in parallel to the others and then connected to the electronic part of the system, the “inverter”, having the role of adapting the produced power to the characteristics of the public electrical grid.

Other electronic components are the bypass diodes and the blocking diodes.

Each bypass diode protects the panel to which it’s applied providing an alternative path to the current flow generated by other panels. These diodes guarantee both the panel protection and the whole system functionality in case of damaged or shaded panels.

Blocking diodes (or “cut-off” diodes) protect the whole string from current reflow from other strings due to a lower voltage on the string typically caused by shadow on a part of the string.

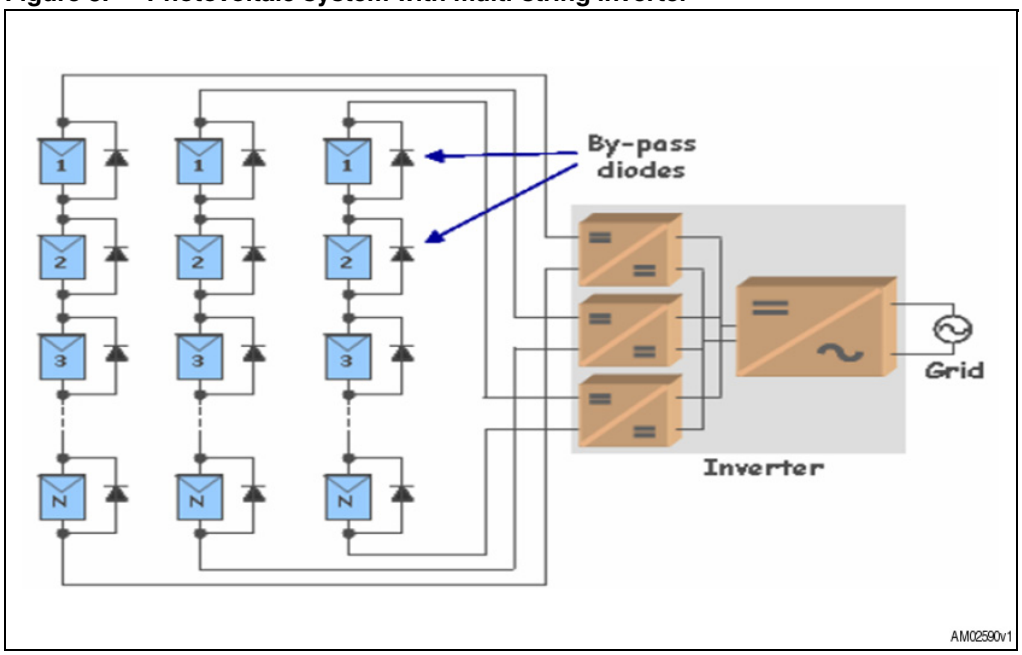
Inverters are complex systems normally including 3 functions (DC-DC conversion, DC-AC conversion and Anti-Islanding) managed by a main controller typically implemented by a microcontroller or a DSP and executing following actions:

- Anti-island control, a safety control forcing the system disconnection from the grid when this is off for maintenance.
- Inverter control, for transforming the DC power generated by the system in the AC power compatible (in terms of voltage and current amplitude, frequency and phase) with the power on the public grid.
- The MPPT (Maximum Power Point Tracking) control, allowing extracting the maximum power as possible from the PV field in order to maximize the power sourced to the grid.

A limitation of the architecture in *Figure 2* is that the MPPT control performs properly just when the PV field is irradiated uniformly.

A first evolution of the above architecture is the following one (string-distributed), where the inverter includes more DC/DC converter sub-blocks implementing its own MPPT control:

Figure 3. Photovoltaic system with multi-string inverter

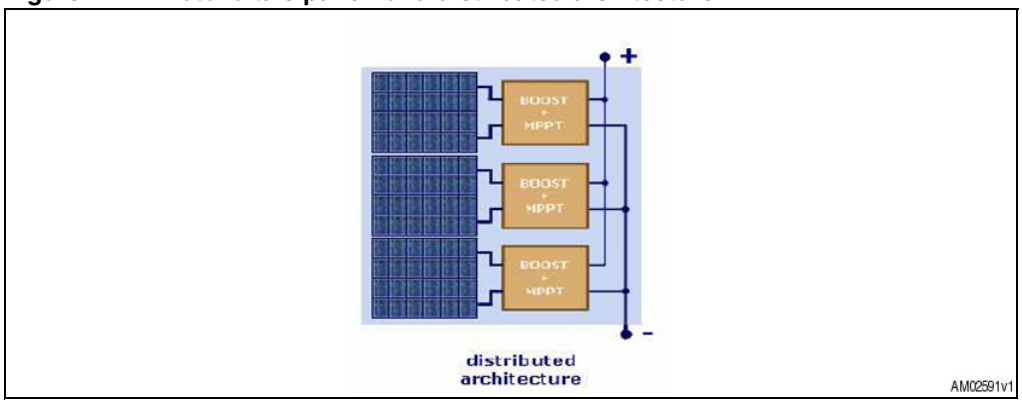


Even if this architecture faces the different shadow on the strings, it doesn't solve the problem of the partial shading on each panel.

A real solution to this matter is to place the DC/DC and related MPPT control on each panel. This approach implies the inverter architecture simplification that doesn't require anymore the DC/DC block and related controller.

Furthermore, in order to minimize the impact of partially shading on each panel, it's possible to force the concept having a DC/DC for each cell of the panel. As compromise between costs and performance the following approach could be followed, where a panel is split into 3 different sub-strings:

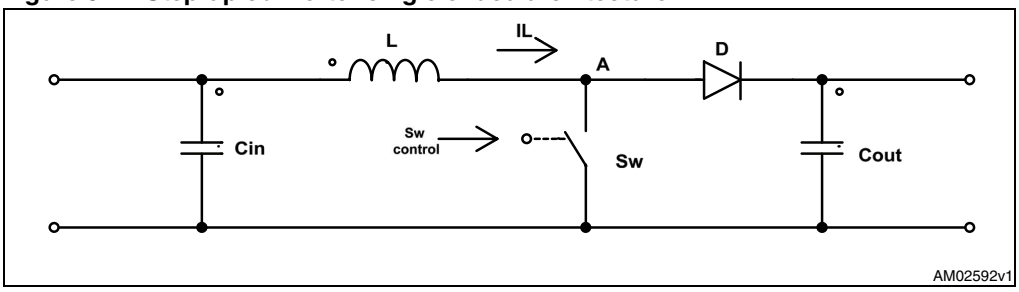
Figure 4. Photovoltaic panel for a distributed architecture



2 Application information

A step-up (or boost) converter is a switching DC-DC converter able to generate an output voltage higher than (or at least equal to) the input voltage.

Figure 5. Step-up converter single ended architecture



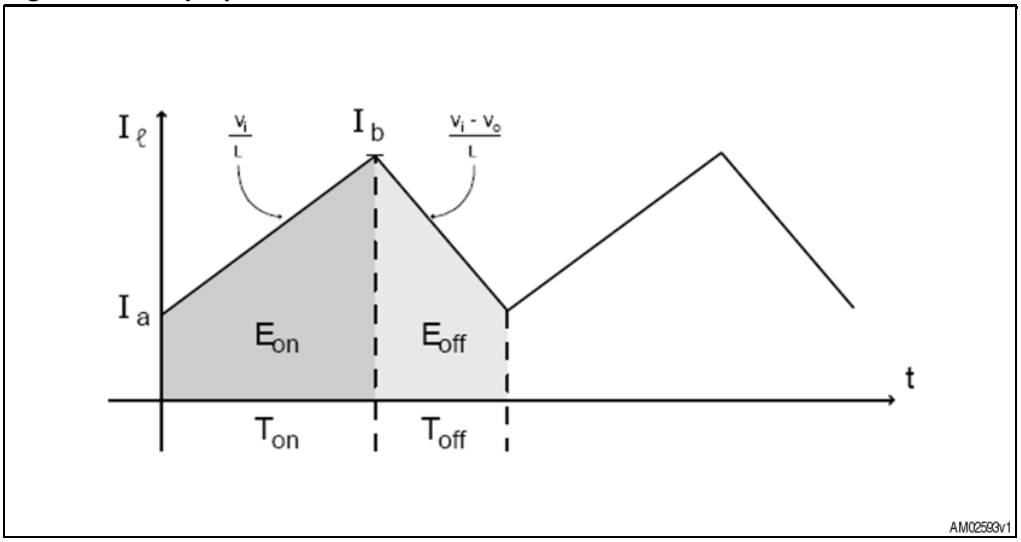
The switching element (Sw) is typically driven by a fixed frequency squared waveform generated by a PWM controller.

When Sw is closed (T_{on}) the inductor stores energy and its current increases with a slope depending on the voltage across the inductor and its inductance value. During this time the output voltage is sustained by C_{out} and the diode doesn't allow any charge transfer from output to input stages.

When Sw is open (T_{off}) the current in the inductor is forced flowing toward the output until voltage on node "A" is higher than output voltage. During this phase the current in the inductor decreases while the output voltage increases.

Following figure shows the behavior of the current on the inductor.

Figure 6. Step-up converter in continuous mode



Comparing the energy stored in the inductor during T_{on} and the energy released during T_{off}, the relation between V_{out} and V_{in} is:

$$\frac{Vout}{Vin} = \frac{1}{1-D}$$

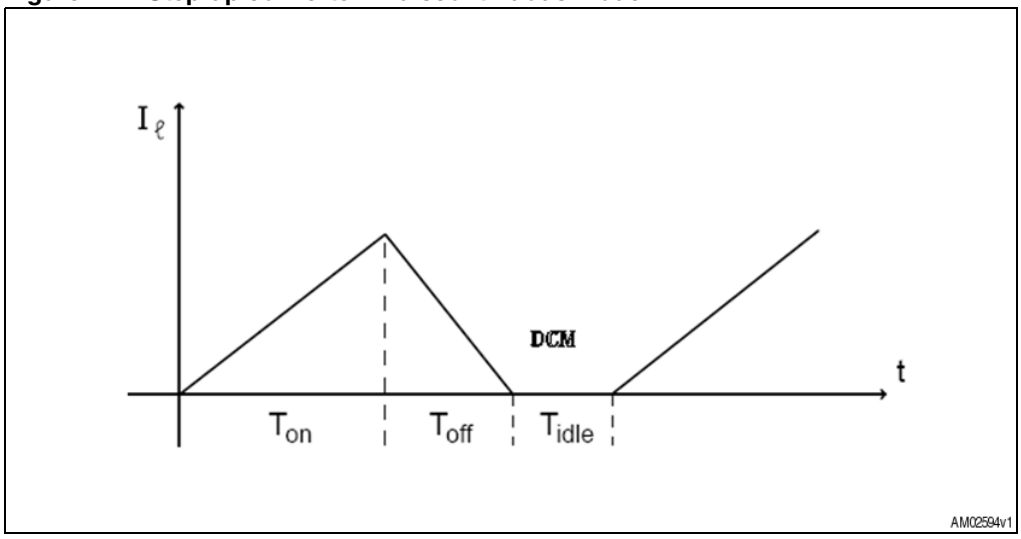
Where “D” is the duty cycle [$T_{on}/(T_{on}+T_{off})$] of the squared waveform driving the switching element.

Boost applications can work in two main cases:

- Continuous Mode (CM) and;
- Discontinuous Mode (DCM);

depending if the current on inductor becomes null (DCM), or not (CM), within the switching period.

Figure 7. Step-up converter in discontinuous mode



Even if a boost converter can work both in CM and DCM, the efficiency is normally higher when it works in CM, if the switching frequency is maintained constant.

Inductance and switching frequency (F_{sw}) impact the working mode. In fact, in order to have the system working in CM following rule should be used:

$$L > \frac{Vout^2}{Pin} * \frac{(D * (1-D))^2}{2 * Fsw}$$

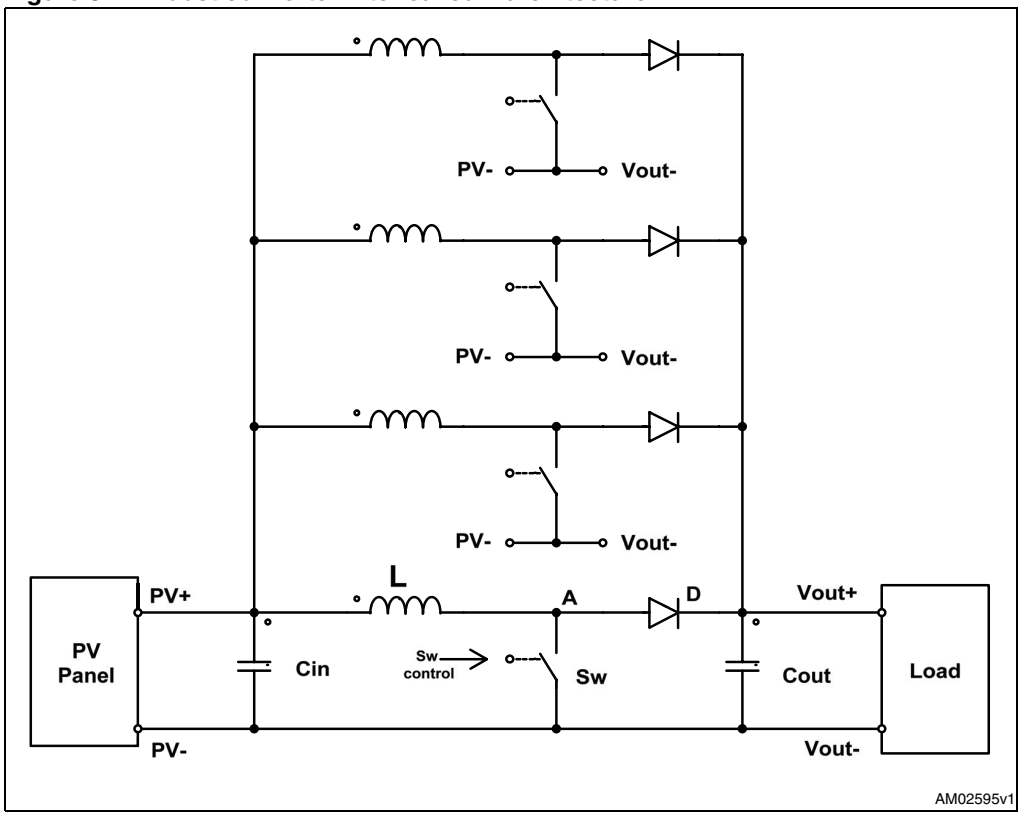
Worst case for L is the above formula is D = 50%.

3 SPV1020 description

SPV1020 is an IC designed to control a boost with a 4 phases interleaved topology supplied by photovoltaic panels.

In a 4-phases topology the inductor-switch-diode branch is cloned 3 times and the resulting 4 branches are connected in parallel. The resulting scheme is showed below:

Figure 8. Boost converter Interleaved 4 architecture

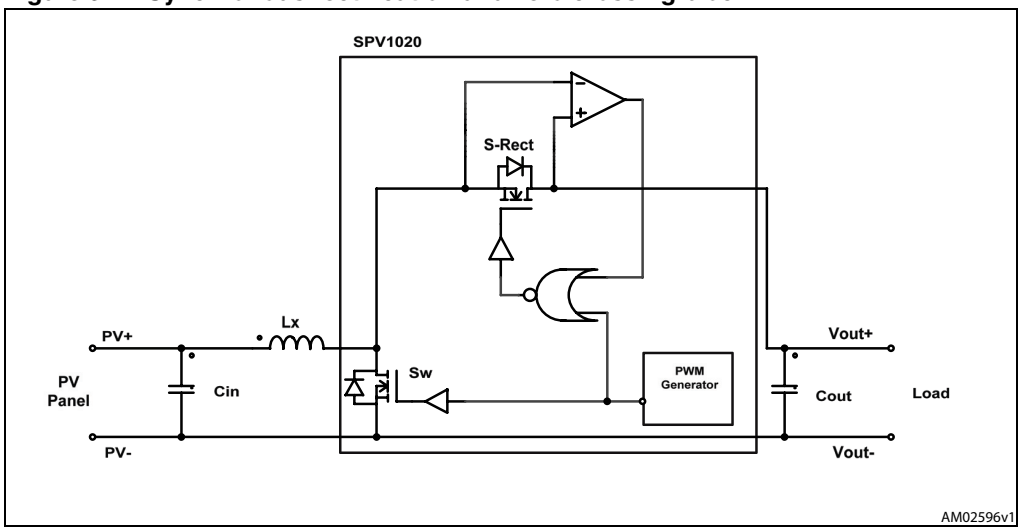


SPV1020 drives the 4 switching elements with the same waveform but shifted of $T_{SW}/4$.

In order to increase the application efficiency each diode can be replaced by a switching element driven complementary respect to the correspondent switch. Furthermore, these 4 more switching elements (synchronous rectifiers) must be driven in order to avoid any current flow from output toward input.

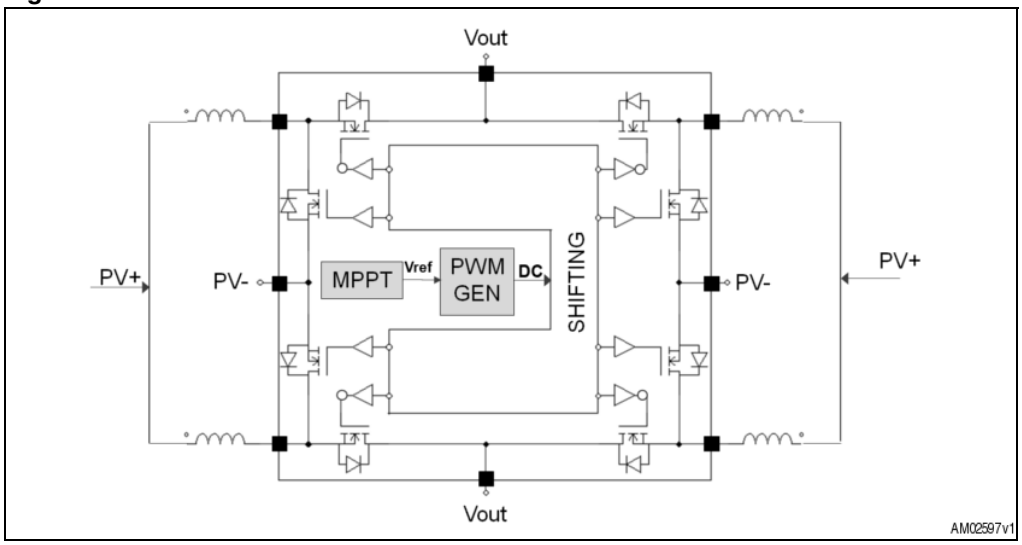
SPV1020 integrates 4 Zero Crossing Blocks, one for each branch. Their role is turn off the related synchronous rectifier to prevent reverse current flow from output.

Figure 9. Synchronous rectification and zero crossing block



Finally, in order to reduce the whole BOM, SPV1020 integrates the 8 switching elements.

Figure 10. Boost IL-4 and SPV1020



Even if the interleaved topology increases the BOM and the routing of the final PCB, it is preferable to the single ended especially in high power application.

In fact, output voltage ripple and efficiency are critical parameters for boost application.

Here follows a brief description of a boost IL-4.

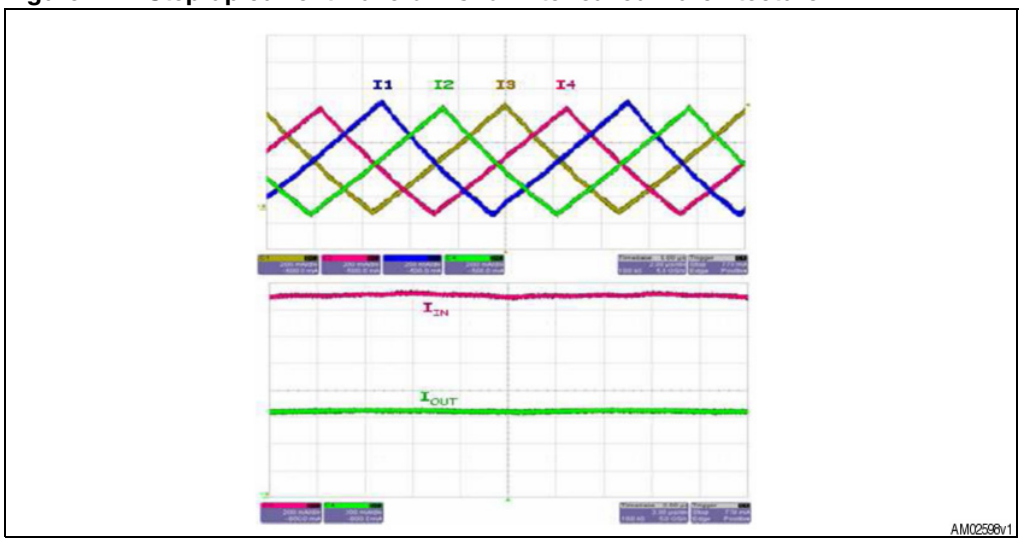
4 Output voltage ripple

Assuming a resistive load, the output voltage ripple is directly tied to the output current ripple.

In a single ended architecture, the output current is the current flowing on the inductor when it re-circulates through the rectifiers. Referring to *Figure 6: Step-up converter in continuous mode on page 9*, higher is the inductance of the inductor, smaller is the current ripple (I_b-I_a).

In IL-4 architecture, output current is the sum of the 4 current flowing on each inductor. Even if the current on each branch is the same as in the single ended architecture, the $T_{SW}/4$ shift between the driving signals implies that output current has tiny ripple. Following figure shows both the current on each branch and the final I_{OUT}.

Figure 11. Step-up current waveforms for Interleaved 4 architecture



Respect to single ended architecture, input and output current ripple are reduced a lot due both to the split of the incoming current in the 4 branches and the related shift.

5 Application efficiency

Designing a boost application a typical constraint is the maximum output current ripple. Once frequency, input and output voltage are defined, this constraint directly affects the inductance value to place in the application:

$$I_{ripple} = I_{L\,max} - I_{L\,min} = \frac{Vin}{L} * \frac{D}{Fsw}$$

Inductance value can be designed for a single ended architecture and then divided by 4 in case of IL-4 architecture.

Each inductor, due to its internal resistance (R_L), could affect a lot the whole system efficiency. For high current application, inductor with a compact geometry risks to miss the efficiency requirements.

In fact, using the same ferromagnetic material, higher inductance can be achieved by increasing the inductor geometry, or by increasing the number of spins but using a thinner wire.

In order to save space and cost, the latter solution is preferred but impacts the internal resistance (increases) and the saturation current (reduces) of the inductor.

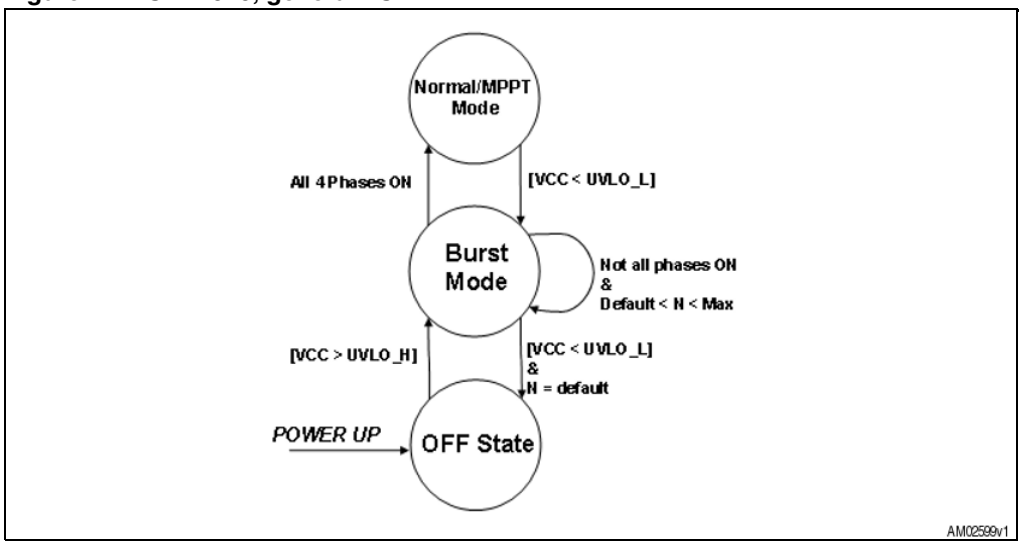
6 SPV1020 functionalities

Operating modes

SPV1020 works among 3 main operating modes/states, depending on the voltage provided by the supply source and by the previous mode/state:

- OFF state,
- BURST mode,
- Normal (or MPPT) mode.

Figure 12. SPV1020, general FSM



7 OFF state

SPV1020 has a UVLO (under voltage lockout) with hysteresis of 500mV. The two thresholds are 6.5 V (UVLO_H) for turning on and 6.0 V for turning off (UVLO_L).

At power up, until the supply source provides a voltage lower than the UVLO_H, the SPV1020 stays in OFF State. In this state, no switching is applied to the switching elements and all the amount of current provided by PV panel (supply source) is directly transferred to the output node through the intrinsic diode of the synchronous rectifiers.

When the applied voltage reaches UVLO_H level, SPV1020 goes in Burst Mode. Burst Mode guarantees a soft start-up and shutdown. When in Burst Mode, SPV1020 update an internal counter according with the comparison between sampled supply voltage and UVLO thresholds. SPV1020 goes back in OFF state when the internal counter returns to its default value. Further details about Burst Mode are available in next session.

8 Burst mode

This mode guarantees a correct start-up for SPV1020, avoiding voltage oscillation. After the power supply connection, the converter starts to work when input voltage becomes higher than 6.5 V (ULVO_H).

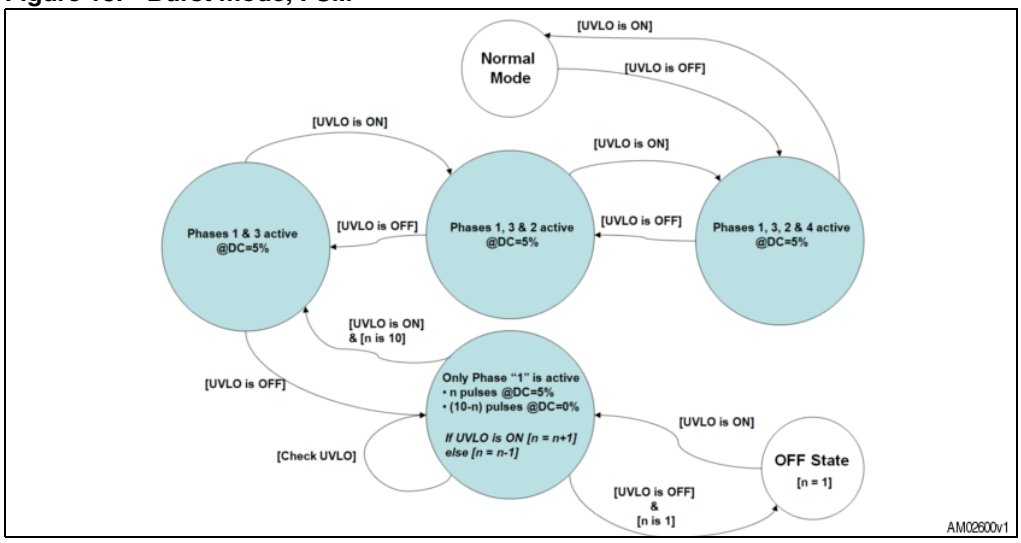
Burst Mode contains 4 internal states, which guarantees to activate gradually phase “1” and sequentially the four phases. Following diagram shows the FSM of the burst mode (grey circles are the states of the burst mode).

Each phase is driven with set of 10 “pulses”. Each pulse can be “ON”, driving the phase with a signal at minimum PWM (DC = 5%), or “OFF”, driving signal completely low.

When activated, a phase is driven with 1 pulse “ON” and 9 “OFF”. Number of “ON” pulses can be increased up to 10 (in this case, another phase is activated), or decreased up to 0 (the phase is always off).

Increasing or decreasing “ON” pulses depends on the status of the ULVO signal that checks if input voltage is greater the minimum threshold or not.

Figure 13. Burst mode, FSM



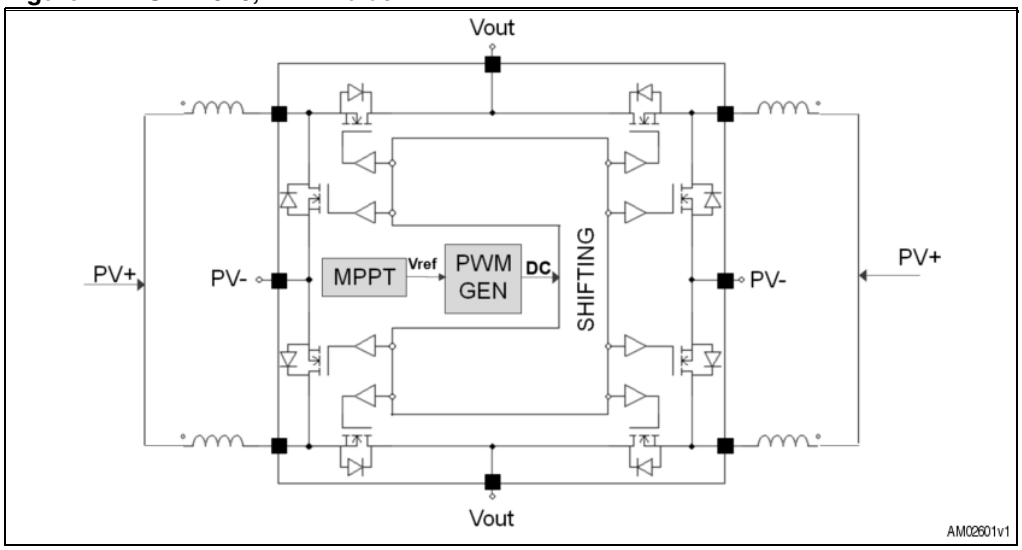
When all the 4 phases are active the system enters the Normal (or MPPT) mode.

9 Normal/MPPT mode

This mode guarantees the maximum power extraction from a photovoltaic input supply by executing an MPPT algorithm.

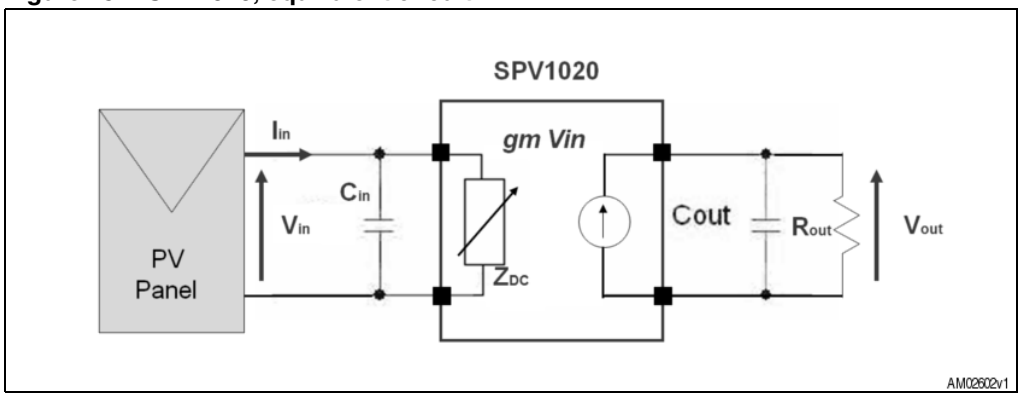
MPPT algorithm generates a voltage reference (Vref) for a PWM generator. The resulting waveform (which Duty Cycle is proportional to Vref) drives the 8 internal switching elements.

Figure 14. SPV1020, MPPT block



The whole application can be assumed equivalent to impedance between input source and output load and which impedance value (Z) depends on the DC set by SPV1020.

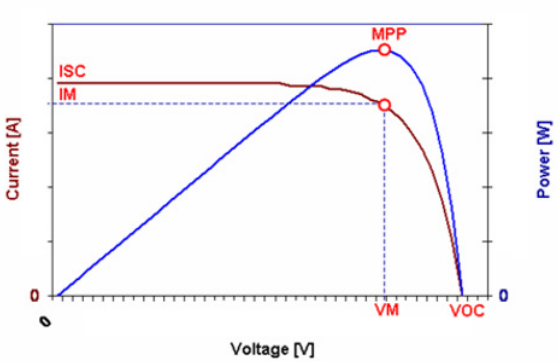
Figure 15. SPV1020, equivalent circuit



Each Z affects power transfer between input source and output load and for each Z an input voltage (V_{in}) and current (I_{in}) can be measured. Purpose of MPPT algorithm is to regulate the proper DC in order to guarantee $Z = Z_M$, assuming Z_M as the impedance value for which the power extracted from the supply source ($P_{in} = Vi_n * I_{in}$) is maximum ($P_M = V_M * I_M$).

Following figure shows both the typical curves Power- Voltage and Voltage-Current of a photovoltaic panel.

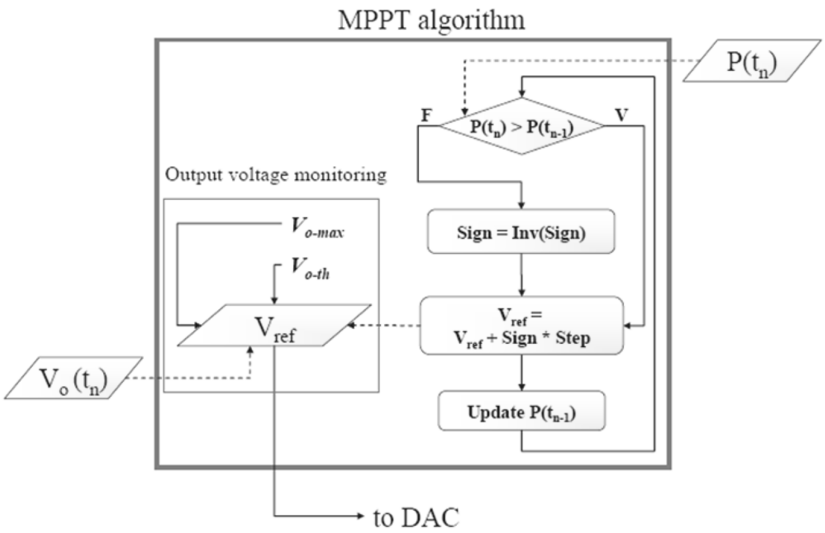
Figure 16. PV panels, voltage-power and voltage-current curves



The Voltage-Current curve shows all the available working point of the PV panel at a given solar irradiation. The Power- Voltage curve is derived by the Voltage-Current curve, plotting the product V*I for each voltage applied.

Following figure shows the dataflow diagram of the MPPT algorithm implemented by SPV1020:

Figure 17. MPPT data flow diagram



Voltage reference generated by the MPPT is always limited by the Over Voltage ($V_{o\text{-}max}$) and Voltage regulation ($V_{o\text{-}th}$) control of the output (see next session for details).

This algorithm approach is defined as perturb & observe because the system is excited (perturbed) with a certain duty cycle (DC), then power is monitored (observed) and then perturbed with a new DC depending on the monitoring result.

SPV1020 executes the MPPT algorithm with a period that is 256 times the switching period (switching period is 10us, by default) that is 2.56ms. This time is required for the application to reach the new steady state (voltages and currents) after the perturbation of the DC, which is 0.2% in most of the range.

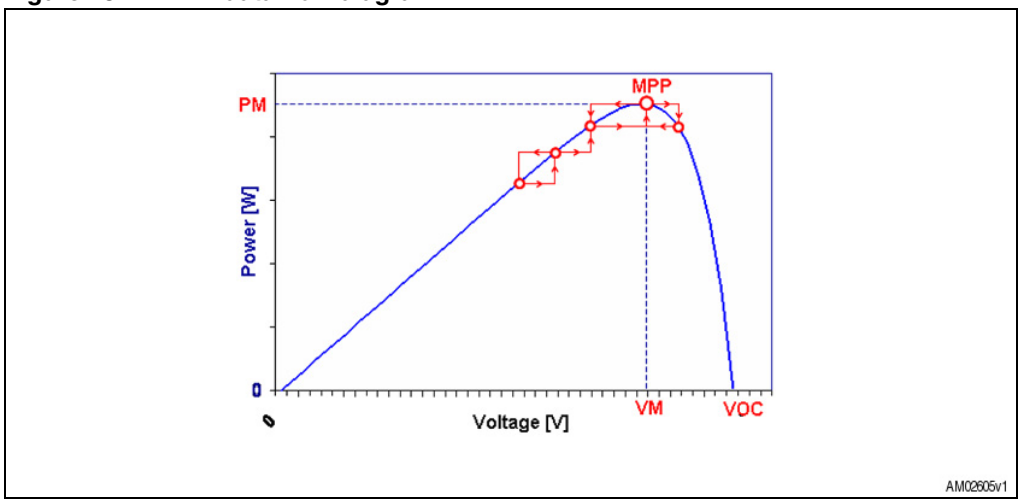
Increasing or decreasing DC depends on the update done in previous step (Sign) and by the trend of the input power.

In fact, MPPT algorithm compares the current input power (P_{tn}) with the input power computed in the previous step (P_{tn-1}). If power is growing then the update is same of the previous step, otherwise the update is swapped (from increasing to decreasing or vice-versa).

When system is at the MPPT, user can see the duty cycle oscillating between 3 values within a time window of 256*3=768 times the switching period (7.68 ms).

Following figure shows the sampling/working points (by red circles) set by the SPV1020 and how they change (by red arrows) during the normal operating mode.

Figure 18. MPPT data flow diagram

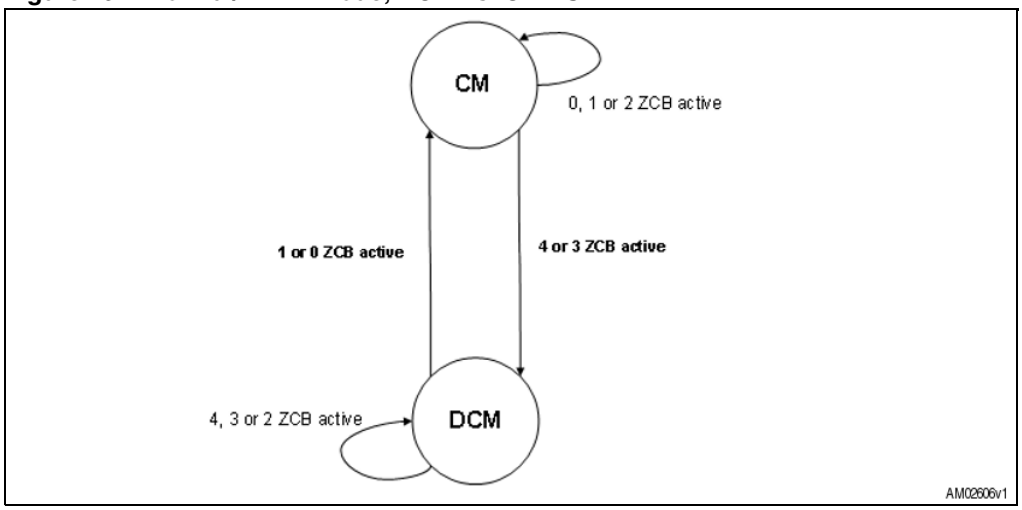


Input for the MPPT algorithm is the incoming power but its computation depends on the working mode of the application: DCM or CM.

SPV1020 discriminates between DCM and CM by the zero crossing blocks (ZCB, refer to zero crossing section for details).

SPV1020 moves between DCM and CM states implementing a sort of hysteresis, depending on how many of the 4 ZCB have its own output activated. Following figure shows the related FSM implemented within the Normal/MPPT mode:

Figure 19. Normal/MPPT mode, DCM vs. CM FSM



In case of DCM, input current could be negligible and its sampled value could be strongly affected by the noises caused by the switching elements. So, input power is computed as follow, avoiding the use of the input current:

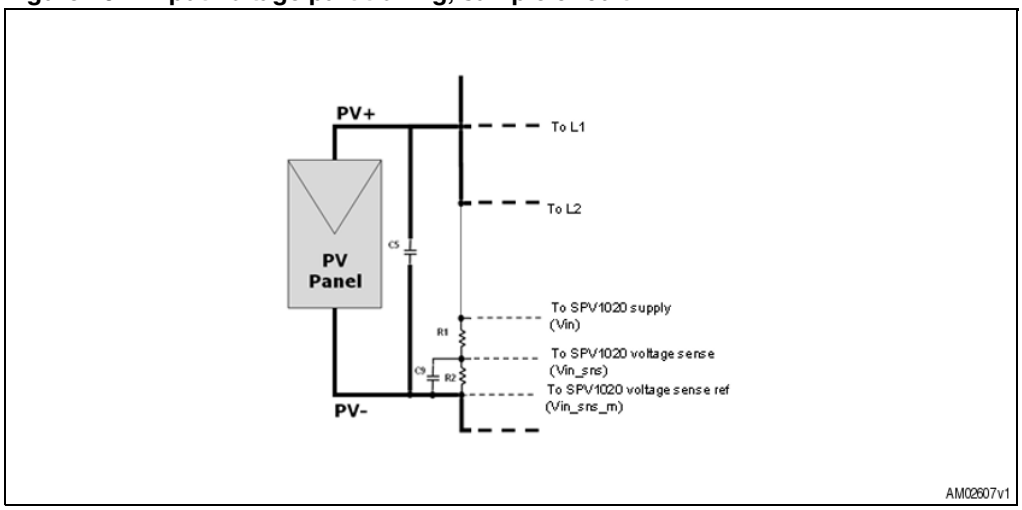
$$P(tn) = V^2 * Don * (Don + D_{off})$$

In case of CM input power is computed by multiplying the sampled voltage and the sampled current:

$$P(tn) = V * I$$

Input voltage is sampled by an external resistive partitioning, while the input current is sampled internally to reduce the number of external components on the application. Here follows a simple schematic of the input voltage sensing circuitry (see *Chapter 13: External component selection on page 30* for values of the showed components).

Figure 20. Input voltage partitioning, sample circuit



10 Voltage regulation

In order to protect both the device itself and the load, SPV1020 implements a dual control on the output voltage (Vout).

Control on Vout is done through Vout_sns pin, connected to Vout by a resistive partitioning (see *Chapter 13: External component selection on page 30* for resistances values). Control consists of comparing Vout_sns with the 2 internal thresholds:

1.00V, for Voltage Regulation and

1.04V, for Over-Voltage Protection

When V_{OUT_SNS} increases up to 1V the output feedback loop enters regulation, limiting the output voltage. Limitation consists generating an upper limit for the DC generated by the MPPT algorithm.

The stability of the loop must be externally regulated connecting a resistor and a capacitor (pole-zero compensation) between the PZ_OUT pin and SGND pin (see *Chapter 13* for resistances values).

10.1 Overvoltage protection

If the Vout_sns exceeds 1.04V a fault signal is generated and transmitted to the fault controller which stops the drivers and produces a fault, setting the bit OVV in the status register. This information is accessible through SPI interface by Read Status command (op code 0x07). When VOUT_SNS falls down to 1.04 V the DC-DC switched ON again and the converter restarts the MPP research from the minimum duty cycle (5%).

10.2 Overcurrent protection

To guarantee the safety of the whole application, SPV1020 implements an over current protection on the low side power switches. Indeed, when Lx is accidentally shorted to VIN or VOUT or when the current flowing through the inductor exceed the peak current limit (4.5A), the related low side power switch is immediately turned OFF and the linked synchronous rectifier is enabled to turn ON. The low side power switch is turned ON again at the next PWM cycle.

In case of overcurrent on branch x [x = 1..4] the related OVC bit of the status register is set. This information is accessible through SPI interface by Read Status command (op code 0x07).

10.3 Currents balance

Different parasitic resistance between the 4 branches of the IL-4 architecture can be the root cause of a unbalanced current flow between the 4 branches. This event should be avoided because could imply lower efficiency or damages on the application components (such as the inductors) and/or on the SPV1020 itself.

A general recommendation is realizing a PCB layout with symmetric paths on the 4 branches and using high matching inductors of the same production lot.

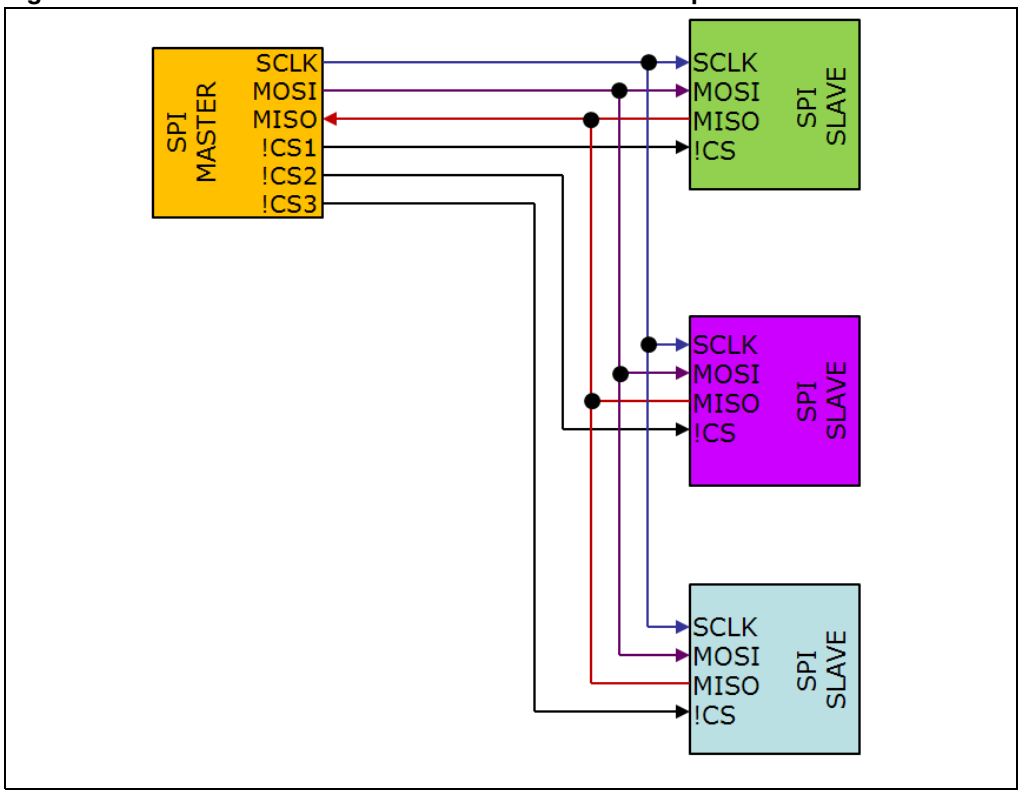
SPV1020 implements an internal control guaranteeing the current balance among the 4 branches, monitoring the current flowing on each branch with a maximum offset of 350mA.

10.4 SPI, serial peripheral interface

The SPV1020 embeds a 4-pin compatible SPI interface. The SPI allows full duplex, synchronous, serial communication between a host controller (the master) and the SPV1020 peripheral device (the slave). SPV1020 provides the following 4 pins:

- XCS (or SS),
- SPI_CLOCK (or SCLK),
- SPI_DATA_IN (or MOSI),
- SPI_DATA_OUT (or MISO).

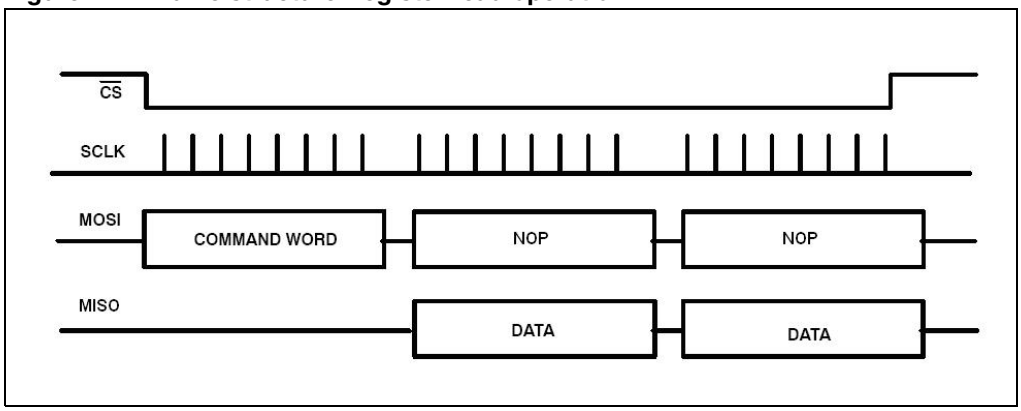
Figure 21. SPI interface: master slaves connection example



The SPI master selects one of the slaves and provides the synchronizing clock and starts all the communications. The idle state of the serial clock for the SPV1020 is high, while data pins are driven on the falling edges of the serial clock and they are sampled on its rising edges (SPI control bits CPOL=1, and CPHA=1). The bit order of each byte is MSB first.

When the master initiates a transmission, a data byte is shifted out through the MOSI pin to the slave, while another data byte is shifted out through the MISO pin to the master; the master controls the serial clock on the SCLK pin. The SS (active low) pin must be driven low by the master during each transmission.

Figure 22. Frame structure: register read operation



The SPV1020 register file is accessible by the host through the SPI bus. Thus, the host can read some register of SPV1020 control parameters. Each data frame includes at least one command byte followed by some data bytes whose direction depends on the type of command. If the command byte requires some data to be read from the register file, those data are transmitted from the slave to the master through the MISO pin; thus the master appends a number of NOPs (0x00) to the command, so that the entire data can be transmitted, *Figure 22*. In other words, the master has to transmit a byte to receive a byte.

If the SS wire goes high before the completion of a command byte in the data frame, the SPV1020 rejects that byte and the frame is closed; then the next data frame is considered as a new one, starting with a command byte.

Some data words can be longer than 8 bits, such as ADC results (10 bits); in such cases, data is first extended to the nearest multiple of one byte (it is right justified), then it is split into bytes, e.g. the ADC result R is formatted as follows:

Table 1. Data format for words longer than 8 bits

	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Byte 1	0	0	0	0	0	0	R9 MSB	R8
Byte 2	R7	R6	R5	R4	R3	R2	R1	R0 LSB

Table 2 shows a list of commands. Each command addresses a memory location of a certain width and sets the direction of the related data.

Table 2. Commands list

Code (Hex)	Name	R/W	Comment
00	Reserved		Reserved
01	NOP		no operation
02	SHUT		Shuts down SPV1020
03	Turn ON		Required only after SHUT command
04	Read current	read	Read 10 bits in 2 bytes (MSB is first received bit)
05	Read vin	Read	Read 10 bits in 2 bytes (MSB is first received bit)
06	Read pwm	Read	Read 9 bits in 2 bytes (MSB is first received bit)
07	Read status	read	read 7 bits: OVC (4bits), OVV (1bit), OVT (1bit), CR (1bit)

For further information about the SPI interface, such as timing diagrams please refer to SPV1020 datasheet.

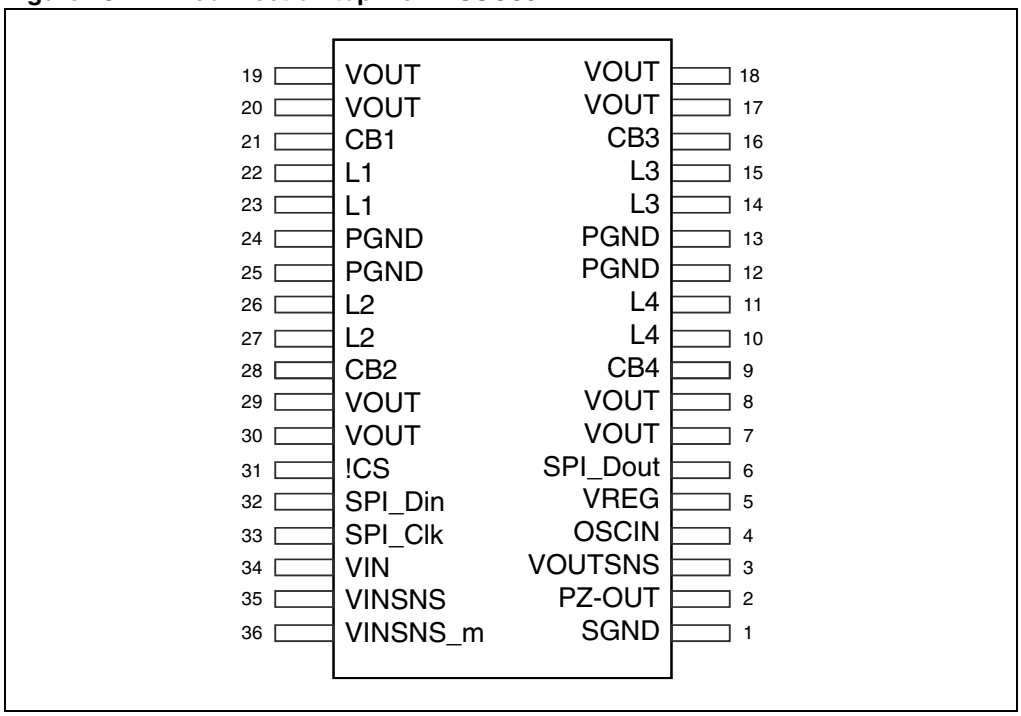
11 Pin description

Table 3. Pin description

Pin (Psso36)	Name	Type	Description
34	VIN	Supply	DC input power supply unit.
7,8,17-20,29,30	VOUT	Supply	Booster output voltage
12,13,24,25	PGND	Ground	Power ground
1	SGND	Ground	Signal ground reference.
10,11,14,15, 22,23,26,26	LX1…4	I	Booster inductor connection.
9,16,21,28	CB1…4	I/O	External bootstrap capacitors have to be connected between these pins and LXi
31	XCS	I	Chip select for SPI interface: XCS = HIGH => SPI device is not active XCS = LOW => SPI device is active If this pin is left floating an internal resistor pulls the XCS pin up switching the SPI off.
32	SPI_DATA_IN	I	Input pin for SPI data flow. If not used, this pin should be connected to ground.
33	SPI_CLK	I	Input pin for SPI clock signal. If not used, this pin should be connected to ground.
35	VIN_SNS	I	Sense pin of input voltage. To be biased with a resistor divider between VIN and SGND
36	VIN_SNS_M	I	Dedicated reference pin for voltage sensing.
2	PZ_OUT	I/O	This pin is used to compensate the feedback loop of the output voltage. A series of resistor and capacitor has to be connected versus SGND.
3	VOUT_SNS	I	Sense pin of output voltage. To be biased with a resistor divider between VOUT and SGND
4	OSC_IN	I	Pin for fine tuning of the switching frequency; to set the default value (100 KHz) this pin has to be tied to VREG, otherwise for fine tuning it has to be biased through a resistor versus SGND.
5	VREG	I/O	Power supply for internal low voltage circuitry; an external thank capacitor has to be connected to this pin versus ground
6	SPI_DATA_OUT	O	Output pin for SPI data flow. If not used, this pin should be left floating.

11.1 Pin connection

Figure 23. Pin connection top view PSSO36



12 Absolute maximum ratings

Table 4. Maximum ratings

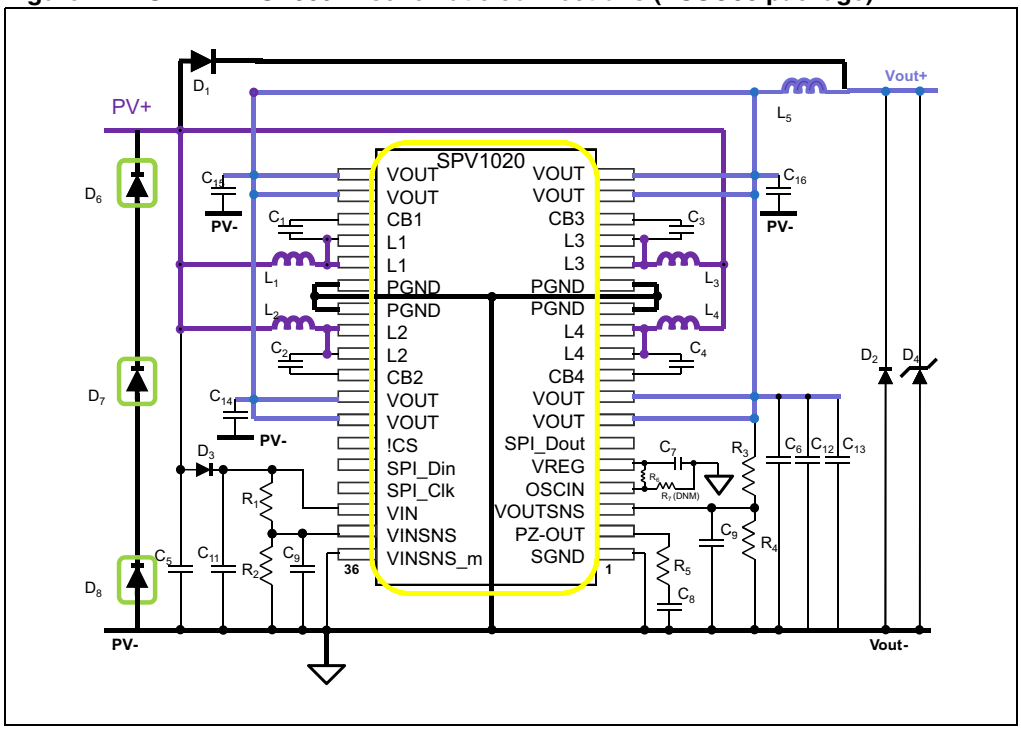
Symbol	Parameter	Range [min, max]	Unit
VIN	Power supply	[-0.3, 40]	V
VOUT	Power supply	[-0.3, 40]	V
PGND	Power ground	0	V
SGND	Signal ground	[-0.3, 0.3]	V
VOUT_SNS	Analog input	[-0.3, VOUT + 0.3]	V
LX1….4	Analog input	[-0.3, VOUT + 0.3]	V
CB1…4	Analog input/output	[Lxi – 0.3, Lxi + 5]	V
VREG	Analog input/output	[-0.3, 6]	V
VIN_SNS	Analog input	[-0.3, VIN + 0.3]	V
XCS	Digital input	[-0.3, VIN + 0.3]	V
OSC_IN	Analog input	[-0.3, VIN + 0.3]	V
PZ_OUT	Analog input/output	[-0.3, VIN + 0.3]	V
SPI_DATA_OUT	Analog output	[-0.3, VIN + 0.3]	V
SPI_CLK	Digital input	[-0.3, VIN + 0.3]	V
SPI_DATA_IN	Digital input	[-0.3, VIN + 0.3]	V
VIN_SNS_M	Dedicated ground	[-0.3, + 0.3]	V

13 External component selection

SPV1020 requires a set of external components and their proper selection guarantees both the best chip functionality and system efficiency.

Following chapters will refer to the connections and component labels showed in the schematic below:

Figure 24. STEVAL-ISV009v1 schematic connections (PSSO36 package)



Please note that dashed connections on OSCIN pin are alternative: if default switching frequency will be used (100kHz), then a short between pins OSCIN and VREG is suggested. Alternatively, if other switching frequency is preferred, a proper resistor has to be placed between OSCIN pin and PV- path and connection between OSCIN and VREG must be avoided.

13.1 Power and thermal considerations

SPV1020 performances are strongly impacted by the power capability of the PWSSO36 package, which depends from the application board as well. According to the technical note TN0054 $R_{TH(j-a)}$ of PwSSO36 can be reduced up 10 °C/W if the package is soldered onto a "2s2p" multi-layer board, thermal vias and metal plate (external heat-sinker).

Starting from this value it is possible to calculate the P_{MAX} .

$$T_J = T_{AMB} + R_{TH(j-a)} \cdot P_D$$

$$P_D = (1 - \eta) \cdot P_{MAX}$$

The SPV1020 efficiency (η) is $\geq$ 98%; the thermal shutdown threshold is 140°C; typical ambient temperature (T_{AMB}) for photovoltaic application is 85°C.

So, the P_{MAX} is:

$$P_D = \frac{T_J - T_{AMB}}{R_{TH(j-a)}} \cdot 5.5W$$

$$P_{MAX} = \frac{P_D}{(1 - \eta)} \cdot 275W$$

If the package is soldered onto a “2s2p” multi-layer board with Thermal vias, the $R_{TH(j-a)}$ is 20°C/W and the P_{MAX} is 138W.

13.2 Inductor selection

Inductor selection is a critical point for this application.

Inductor selection must take into account the following application constraints:

- Maximum input current (i.e. Imp and Isc of the PV panel);
- Maximum input voltage (i.e. Vmp and Voc of the panel)
- Overcurrent threshold of SPV1020.
- Maximum duty cycle of SPV1020 (90%).

Input current from the PV panel will be split between the 4 inductors of each branch, so:

$$I_{Lx}(rms) \cong \frac{I_{mp}}{4} < \frac{Isc}{4}$$

According to *Figure 6*, during charge phase (switch ON), peak current on each inductor will depend on the applied voltage (Vin), on the inductance (Lx) and on the time (Ton).

Considering the maximum duty cycle (90%):

$$I_{Lx}(pk) \cong I_{Lx}(rms) + \frac{1}{2} * \frac{V_{mp}}{Lx} * 9\mu s$$

Taking into account the overcurrent threshold (4.5 A):

$$I_{Lx}(pk) < 4.5A$$

Finally, inductance should be chosen according to the following formula:

$$L_X > \frac{1}{2} * \frac{V_{mp} * 9\mu s}{4.5 - I_{Lx}(rms)} = \frac{1}{2} * \frac{V_{mp} * 9\mu s}{4.5 - \frac{I_{mp}}{4}}$$

A safer choice should replace Vmp by Voc of the panel.

Usually, inductances ranging between 22 µH to 100 µH satisfy most application requirements.

Critical parameters for the inductor choice are inductance (analyzed above), Irms, saturation current and size.

Irms is a quite important parameter because causes the self rising temperature of the inductor, affecting the nominal inductance value. So above constraint (I_{LX}(pk)<4.5 A) could be violated.

At the same size, small inductance value inductors guarantee both faster response to load transients and higher efficiency.

Inductor size also affects the maximum current deliverable to the load. In any case, the saturation current of the choke should be higher than the peak current limit of the input source. So, suggested saturation current should be > 4.5A.

Inductors with low series resistance are suggested to guarantee high efficiency.

13.3 Boost capacitors

C1, C2, C3 and C4 are four capacitors used to guarantee SPV1020 internal functionality. Their role is to maintain the required voltage level on pins CB1, CB2, CB3 and CB4 even during the charging phase of the inductors.

Capacitance value is the same for all of the 4 capacitors and is not application dependant. Suggested value is in the range of 22 nF to 100 nF.

Each capacitor switches synchronously to the related inductor, so at 100 kHz while maximum voltage is fixed by the internal voltage regulator (~5V).

Low-ESR capacitors are good choices to increase the whole system efficiency.

13.4 Internal voltage rail capacitors

C7 is a tank capacitor used to guarantee the voltage level (5 V) of the internal regulated voltage of the SPV1020.

Suggested value is 470 nF and it isn't application dependant.

Same voltage range as for boost capacitors can be used. Maximum voltage must be higher than 5 V.

Low-ESR capacitors are good choices to increase the whole system efficiency.

13.5 Input voltage capacitors

C5 is the input capacitance added at the input in order to reduce the voltage ripple.

Maximum voltage of this capacitor is strictly dependent by the input source (typically between 25 V and 50 V).

Low-ESR capacitors are good choices to increase the whole system efficiency.

Suggested minimum input capacitance is 2 µF.

In order to reduce the ESR effect it is suggested to split input capacitance into 2 capacitors placed in parallel.

Another capacitor (C11) is connected to the supply input pin of the SPV1020 (Vin). Its role is to make as stable as possible the voltage on this pin that could be affected by the ripple of the PV panel voltage.

According with the maximum current (Isc) provided by the PV panel connected at the input, following formula can be used in order to select the proper capacitance value (Cin) for a specified maximum input voltage ripple (Vin_rp_max):

$$Cin \geq \frac{Isc}{Vin\_rp\_\max * Fsw}$$

13.6 Input voltage partitioning

Input voltage must be scaled to the reference voltage level (1.25V) of the ADC integrated in the SPV1020.

R1 and R2 are the 2 resistors used for partitioning the input voltage.

Said V_{OC} voltage at open circuit of the PV panel, then R1 and R2 must be selected according to the following rule:

$$\frac{R1}{R2} = \frac{Voc}{1.25} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R1 and R2, their power dissipation has to be taken into account.

Assuming negligible the current flowing through pin Vin_sns, maximum power dissipation on the series R1+R2 is:

$$P_{vin\_sns} = \frac{(Voc)^2}{R1 + R2}$$

As empiric rule, R1 and R2 should be selected according to:

$$P_{vin\_sns} << 1\%(V_{in\_max} * I_{in\_max})$$

Note: In order to guarantee the proper functionality of pin V_{in_sns} current flowing on the series R1+R2 should be in the range between 20 µA and 200 µA.

13.7 Input voltage sensing capacitor

C9 is placed in parallel to R2 and as close as possible to pin Vin_sns.

Its role is to make as stable as possible the voltage sensed by pin Vin_sns.

Critical parameters for capacitors are: capacitance, maximum voltage and ESR.

Maximum Voltage: if R1 and R2 have been chosen properly, so partitioning Vin to 1.25 V, then maximum voltage of this capacitor can be in the range from 3.3 V or higher.

Capacitance value depends on the time constant (τ_{in}) composed with R1+R2 (τ_{in}= C6*R1//R2) and by the system switching frequency (F_{SSW} = 4*F_{SW}).

Assuming R1 >> R2 (so, R1//R2 ~= R2):

$$\tau_{in} \cong 10 * \frac{1}{Fssw}$$

So,

$$C9 \cong 10 * \frac{1}{Fssw} * \frac{1}{R2}$$

Note: Even if SPV1020 controls each phase at F_{SW} (by default 100 kHz) the whole system switching frequency (F_{SSW}) must be assumed at 4 times the single phase switching frequency (by default 400 kHz).

13.8 Output voltage capacitors

A minimum output capacitance must be added at the output, in order to reduce the voltage ripple.

Critical parameters for capacitors are: capacitance, maximum voltage and ESR.

Maximum voltage of this capacitor is strictly dependent by the output voltage range. SPV1020 can support up to 40 V so, suggested maximum voltage for these capacitors is 50 V, or higher.

Low-ESR capacitors are good choices to increase the whole system efficiency.

Suggested minimum output capacitance is 16 µF.

In order to reduce the ESR effect it is suggested split output capacitance into 3 capacitors placed in parallel.

According with the maximum current (Isc) provided by the PV panel connected at the input, following formula can be used in order to select the proper capacitance value (Cout) for a specified maximum output voltage ripple (Vout_rp_max):

$$Cout \geq \frac{Isc * Vout\_rp\_max}{Fsw}$$

It is suggested to split the capacitance in 4 capacitors, each one to be connected to each of the 4 Vout pins of the SPV1020. This will help in order to balance the impedance of the 4 tracks.

13.9 Output voltage partitioning

R3 and R4 are the 2 resistors used for partitioning the output voltage.

Said VOUT_MAX the maximum output voltage of the load, the R3 and R4 must be selected according to the following rule:

$$\frac{R3}{R4} = \frac{V_{out\_max}}{1.00} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R3 and R4, their power dissipation has to be taken into account.

Assuming negligible the current flowing through pin Vout_sns, maximum power dissipation on the series R3+R4 is:

$$P_{vout\_sns} = \frac{(V_{out\_max})^2}{R3 + R4}$$

As empiric rule, R3 and R4 should be selected according to:

$$P_{vout\_sns} << 1\%(V_{out\_max} * I_{out\_max})$$

Note: In order to guarantee the proper functionality of pin V_{out_sns} current flowing on the series R3+R4 should be in the range between 20 µA and 200 µA.

13.10 Output voltage sensing capacitor

C10 is placed in parallel to R4 and as close as possible to pin Vout_sns.

Its role is to make as stable as possible the voltage sensed by pin Vout_sns.

Maximum Voltage: if R3 and R4 have been chosen properly, so partitioning Vout to 1.25 V, then maximum voltage of this capacitor can be in the range from 3.3 V or higher.

Capacitance value depends on the time constant (τ_{out}) composed with R4 (τ_{out}= C8*R3//R4) and by the system switching frequency (F_{SSW} = 4*F_{SW}).

Assuming R4<<R3 (so, R3//R4 ≅ R4):

$$\tau_{out} \cong 10 * \frac{1}{Fssw}$$

So,

$$C10 \cong 10 * \frac{1}{Fssw} * \frac{1}{R4}$$

Note: Even if SPV1020 controls each phase at F_{SW} (by default 100 kHz) the whole system switching frequency (F_{SSW}) must be assumed at 4 times the single phase switching frequency (by default 400 kHz).

13.11 Internal oscillator frequency

SPV1020 controls the boost application by a PWM signal acting at the default switching frequency of 100 kHz.

Default switching frequency is guaranteed connecting the pin OSCIN to 5 V (VREG pin).

User can change the default value by placing a proper resistor (R6) versus ground.

Internal oscillator works with an integrated resistor of 120 kΩ. Frequency is proportional to the current provided to the oscillator block.

Said F_{switch} the desired switching frequency, R7 must be selected according to the following formula:

$$R7[k\Omega] = \frac{(100) * (120)}{F_{switch}[kHz]}$$

13.12 Diodes selection

SPV1020 requires 3 Schottky diodes: D1, D2 and D3.

D3 (with C11) protects the SPV1020 supply by noise of the whole system switching.

D3 has to be chosen taking care mainly to its low forward voltage in order to impact as less as possible the system efficiency. Maximum forward current will be according to the maximum current sink by SPV1020: a safe choice is around 20 mA. Maximum voltage applied to D3 depends on the PV panel, and anyway can't be > 40 V, due to the technology constraints of SPV1020.

D1 is the alternative path to the current flow when SPV1020 is down and Vin voltage level is higher than Vout.

D2 acts as a typical by-pass diode: it turns on in case of shaded cells and provides an alternative path to the current flowing from other panels.

D1 and D2 are power schottky diodes that must support both:

- Forward current comparable with the maximum current provided by the PV cells. Assuming a PV panel with 6" poly crystalline silicon solar cells, then maximum current will be 9 A.
- Maximum reverse voltage according to the output voltage partitioning. So, at least 40 V, due to the technology constraint of SPV1020.

Furthermore forward voltage and reverse current of D1 and D2 should be lower as possible in order to impact as less as possible the system efficiency.

13.13 Protection devices

SPV1020 demo board mounts a protection transil D4 to avoid the output voltage triggers spikes higher than the safety threshold of 40 V.

This component has to be choice according to the following rules:

VBR > Vout_max;

and

VCL $\leq$ 40 V.

For ISV009v1 mounts D4 which has VBR = 37 V and VCL = 40 V.

13.14 Pole-zero compensation

SPV1020 controls of the whole system stability by an internal loop on Vout_sns.

Transfer function of the loop depends on both output capacitor and load.

Even if the stability can be fine tuned by trimming R5 and C8, their suggested values (R5 = 1 kΩ and C8 = 22 nF) guarantee stability in most applications.

In order to speed-up the system reaction to output voltage changes causing the Over Voltage threshold triggering, C8 can be decreased up to 2.2 nF.

14 Layout guidelines

PCB layout is very important in order to minimize noise, high frequency resonance problems and electromagnetic interference.

Paths between each inductor and relative pin must be designed with the same resistance. Different resistance between the 4 branches can be the root cause of an unbalanced current flow among the 4 branches. Unbalanced currents can imply damages and a bad tracking of the MPPT.

Same approach must be followed for the 4 Vout tracks.

It is essential to keep as small as possible the paths where the high switching current circulates, to reduce radiation and resonance problems.

Large traces for high current paths and an extended ground plane under the metal slug of the package help reduce noise and heat dissipation (which is strongly impacted by the thermal vias as well), furthermore increase the efficiency.

Boost Capacitors must be connected as close as possible to the Lx and CBx pins.

It is also suggested to connect the Boost Capacitor to the Lx track avoiding that its pad is crossed by the high current on flowing on the Lx track.

The output and input capacitors should be very close to the device.

The external resistor dividers, if used, should be as close as possible to the Vin_sns and Vout_sns pins of the device, and as far as possible from the high current circulating paths, to avoid pick-up noise.

For an example of recommended layout see the following evaluation board (dimension expressed in mm):

Figure 25. PCB layout example (top view)

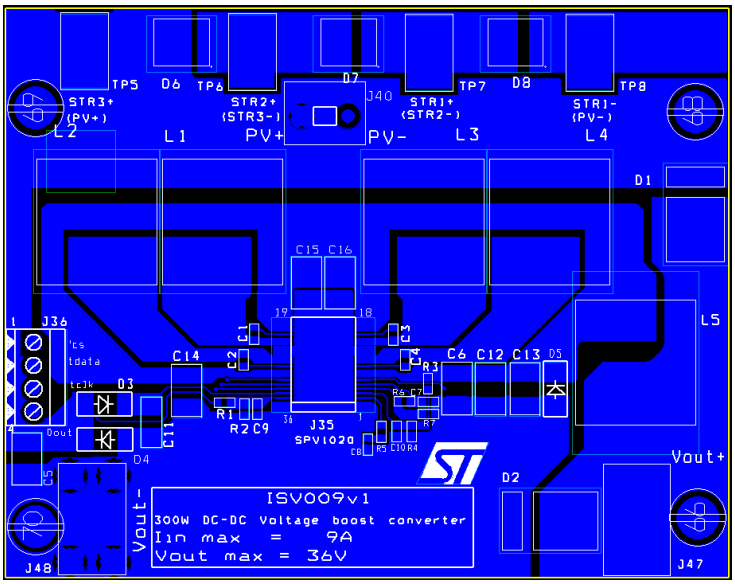
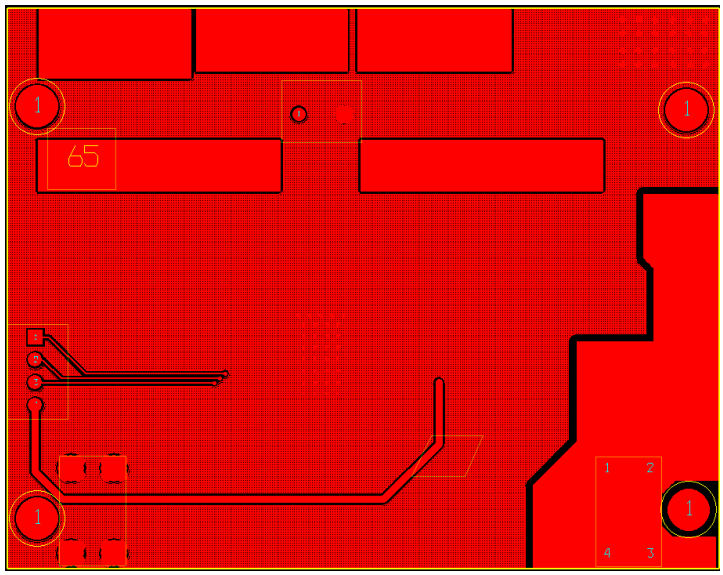


Figure 26. PCB layout example (bottom view)



15 BOM

The following table shows a possible list of external components to configure SPV1020. in an application with Voc = 30 V, Imp = 9 A, Vout_max = 36 V and Fsw = 100 kHz. Of course, suppliers and serial numbers showed are just suggestion and the customer is free to have different choices, according with the rules described in the previous chapters.

Table 5. Bill of material

Component	Name	Value	Supplier	Serial number
C1, C2, C3, C4	Bootstrap capacitors	100nF	MURATA EPCOS	GRM188R71C104KA01 C1608X7R1H104K
C11	Die supply capacitor	1 µF	MURATA EPCOS	GRM31MR71H105KA88 C3216X7R1H105K
C5	PV input capacitor	4.7µF	MURATA EPCOS	GRM31MR71H475KA88 C3216X7R1H475K
C9, C10	Voltage sensing capacitor	220pF	MURATA EPCOS	GRM188R71E221KA01 C1608C0G1H221J
C8	Compensation capacitor	22nF	MURATA EPCOS	GRM188R71C223KA01 C1608X7R1H223K
C7	Internal reference voltage capacitor	470nF	MURATA EPCOS	GRM188R71A474KA61 C1608X7R1C474K
C6, C12, C13, C14, C15, C16	Output capacitor	4.7uF	MURATA EPCOS	GRM32ER71H475KA88K C3225X7R1H475K
D3	Uncoupling on supply pin	STPS160U	ST	STPS160U
R1	Input voltage pertitioning resistor	3.3MΩ	VISHAY	D11/CRCW0603 3.3M
R2	Input voltage pertitioning resistor	110kΩ	CYNTEC	RR0816R-114-DN-11
R3	output voltage partitioning resistor	3.9MΩ	VISHAY	D11/CRCW0603 3.9M 1%
R4	output voltage partitioning resistor	110kΩ	CYNTEC	RR0816R-114-DN-11
R5	Compensation resistor	1kΩ	CYNTEC	RR0816R-102-DN-11
R6	Pull up resistor (Note: R6 must be removed if R7 is soldered)	0Ω		
R7 (optional)	Oscllator resistor (Note: R6 must be removed if R7 is soldered)	Depending on desired Fsw		
L1, L2, L3, L4	Phase x (x=1..4) Inductors	47uH	CYNTEC	PIMB136T-470MS-11
			COILCRAFT	MSS1278T-473ML
			EPCOS	B82477G4473M003
			MURATA	49470SC
D6, D7, D8	PV panel bypass diodes	SPV1001N30	ST	SV1001-N30

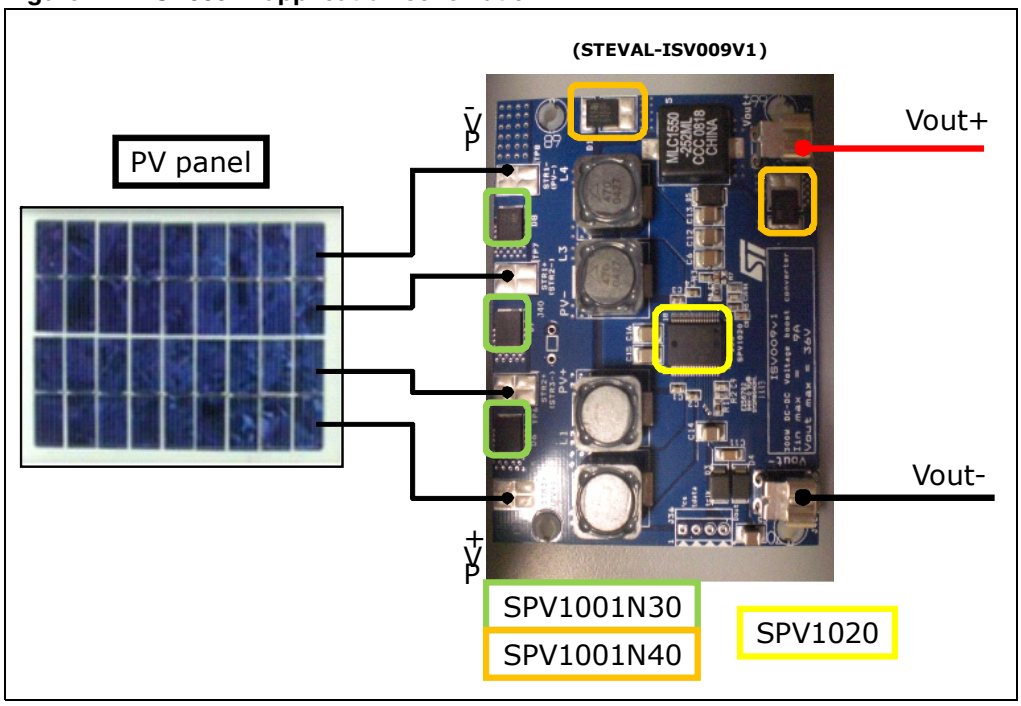
Table 5. Bill of material (continued)

Component	Name	Value	Supplier	Serial number
D1, D2	Controller bypass diodes	SPV1001N40	ST	SPV1001N40
J35	Voltage boost controller	SPV1020	ST	SPV1020
J36	SPI I/F connector	4PIN Connector	Phoenix Contact	1723672
D4	600W, 40V biidirectional protection transil	SMBJ36A	ST	SMBJ36A-TR
J47, J48	Output connector	FASTON CONNECTOR		
J40	Alternative input connector	2PIN connector	Phoenix Contact	
L5	Output current ripple filter	2.5uH	COILRAFT	MLC1550-252ML

Appendix A ISV009v1 application connection

The following figure shows how to connect ISV009V1 to photovoltaic panel.

Figure 27. ISV009v1 application schematic



It is possible to manage a PV string by connecting in series the output stages of the SPV1020 to guarantee the voltage level required by the specific application.

Maximum voltage for ISV009v1 is 36 V, according to R3/R4 partitioning.

For example, if the application requires 400 V (Vout_tot) then the minimum number of ISV009v1 to be connected in series (Ns_min) will be:

$$Ns\_\min \geq \frac{Vout\_tot}{Vout\_\max} = \frac{400}{36} = 12$$

In order to guarantee the performance of the whole PV string (e.g. in case of shaded panels), a minimum of redundancy (10%) on Ns_min is suggested.

Also, considering that SPV1020 is a voltage boost controller it is required that maximum input voltage (Vo of the each PV panel) must be lower than its output voltage. So, maximum number of devices in series is also limited by the following rule:

$$Ns\_\max \leq \frac{Vout\_tot}{Voc}$$

Appendix B SPV1020 parallel and series connection

Output pins of SPV1020s can be connected both in parallel and in series. In both cases the output power (Pout) will depend on light irradiation of each panel (Pin), application efficiency and by the specific constraint of the selected topology.

Objective of this section is to explain how output power is impacted by the selected topology.

Examples with 3 PV panels only will be presented, but conclusion can be extended to a larger number of PV panels.

In case the SPV1020 is on (so light irradiation implying Vin = 6.5V)

$$Poutx = \eta Pinx \ [x = 1..3]$$

In case SPV1020 is off, the system efficiency will depend on the drop of the bypass diode D1 (according to schematic in *Figure 24 on page 30*):

$$Poutx = \eta_{bp} Pinx \ [x = 1..3]$$

Finally, in case of panel completely shaded:

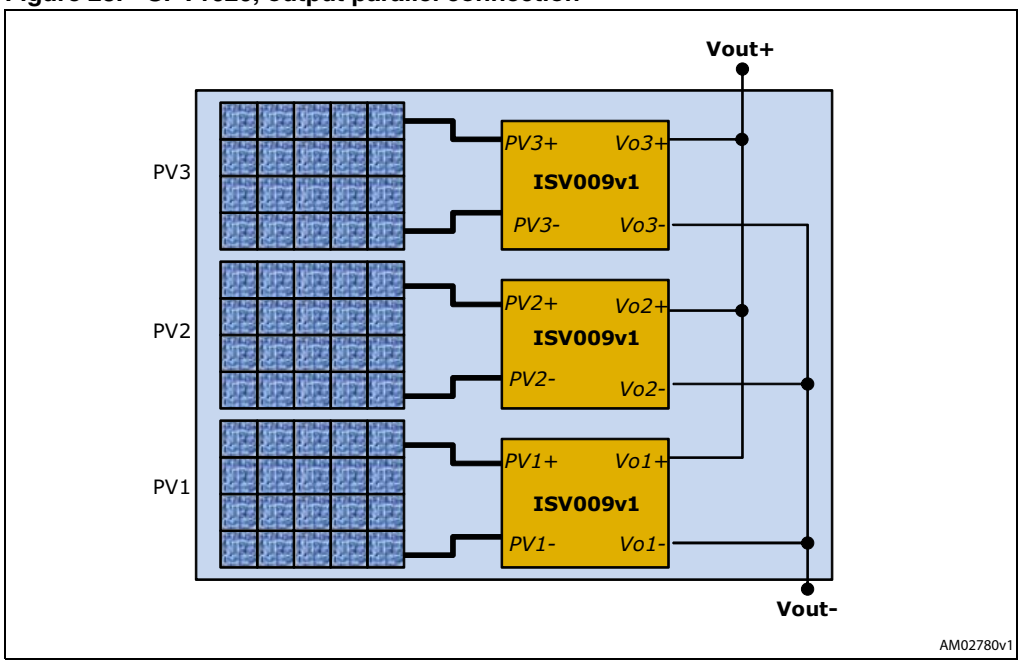
$$Poutx = 0$$

B.1 SPV1020 parallel connection

This topology guarantees the desired output voltage even only one of the panels is irradiated. Of course, the constraint of this topology is that Vout is limited to the SPV1020 technology constraint.

Following figure shows a detail of the parallel connection topology:

Figure 28. SPV1020, output parallel connection



Of course, the output partitioning (R3/R4) of the 3 SPV1020 must be in accord for desired Vout.

According to the topology:

$$Vout = Vout1 = Vout2 = Vout3$$

$$Iout = Iout1 + Iout2 + Iout3$$

According to light irradiation on each panel (Pin) and to the system efficiency (ç), output power is:

$$Pout = Pout1 + Pout2 + Pout3$$

$$Poutx = Voutx * Ioutx \quad [x = 1..3]$$

$$Pinx = Vinx * Iinx \ [x = 1..3]$$

So:

$$Pout = Vout(Iout1 + Iout2 + Iout3) = \eta Pin1 + \eta Pin2 + \eta Pin3$$

Each SPV1020 will contribute to the output power providing Ioutx according to the irradiation of its panel.

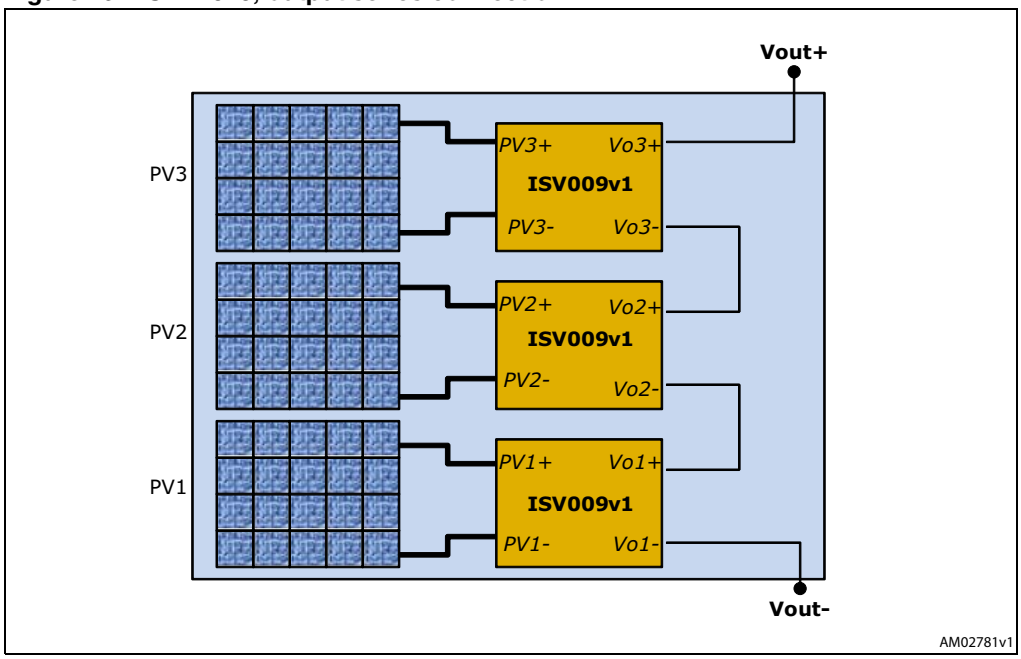
Also, desired Vout will be guaranteed if at least one of the 3 PV panels provides enough power to turn on the related SPV1020.

B.2 SPV1020 series connection

This topology provides an output voltage that is the sum of the output voltages of the SPV1020 connected in series. Following pages explain how the output power is impacted by the topologic constraint.

Following figure shows a detail of the series connection topology:

Figure 29. SPV1020, output series connection



In this case, the topology constraint will imply:

$$Iout = Iout1 = Iout2 = Iout3$$

$$Vout = Vout1 + Vout2 + Vout3$$

In case the irradiation is the same for each panel:

$$Pin1 = Pin2 = Pin3$$

$$Pout = 3 * Poutx \quad [x = 1..3]$$

$$Poutx = \frac{1}{3} Pout$$

$$Poutx = Voutx * Ioutx = Vout1 * Iout$$

So,

$$Voutx = \frac{1}{3} Vout$$

For example, assuming, Pout = 90 W and, if desired Vout = 90 V then

Voutx = 30V.

Lower irradiation for one panel, for example on panel 2, causes lower output power, so lower Vout2 due to the Iout constraint:

$$Voutx = \frac{Poutx}{Iout}$$

Output voltage (Vout) required by the load can be supplied by 1st and 3rd SPV1020 but only up to the limit imposed by their R3/R4 partitioning.

Some examples can help to understand the various scenarios assuming at the following conditions: R3/R4 limiting Voutx = 40V and desired Vout = 90V.

Example 1:

Panel 2 has 75% irradiation than panels 1 and 3:

$$Vout2 = \frac{3}{4} * Vout1 = \frac{3}{4} * Vout3$$

$$Pout1 = Pout2 = 30W$$

$$Pout2 = \frac{3}{4} Pin1 = 22.5W$$

$$Pout = Pout1 + Pout2 + Pout3 = 82.5W$$

$$Iout = \frac{Pout}{Vout} = \frac{82.5}{90} = 0.92A$$

$$Vout1 = Vout3 = \frac{30}{0.92} = 32.6V$$

$$Vout2 = \frac{22.5}{0.92} = 24.45V$$

Two of the SPV1020s (1st and 3rd) supply the voltage drop due to lower irradiation on panel 2.

Note: SPV1020 is a boost controller, so Voutx must be higher than Vinx, otherwise the SPV1020 turns off and the input power is transferred to the output stage trough by pass diode D1 (please, refer to schematic in Figure 24 on page 30).

Example 2:

Panel 2 has 25% irradiation than panels 1 and 3:

$$Vout2 = \frac{1}{4} * Vout1 = \frac{1}{4} * Vout3$$

$$Pout1 = Pout2 = 30W$$

$$Pout2 = \frac{1}{4} Pin1 = 7.5W$$

$$Pout = Pout1 + Pout2 + Pout3 = 67.5W$$

$$Iout = \frac{Pout}{Vout} = \frac{67.5}{90} = 0.75A$$

$$Vout1 = Vout3 = \frac{30}{0.75} = 40V$$

$$Vout2 = \frac{7.5}{0.75} = 10V$$

In this case the system is at the limit, in fact a lower irradiation on will impact Vout1 and/or Vout3 that are anyway at the limit (40V) imposed by R3/R4 partitioning.

Example 3:

Panel 2 completely shaded

In this case the maximum Vout can be 80 V (Vout1+Vout3).

Diode D2 (please, refer to schematic in *Figure 24 on page 30*) on 2nd SPV1020 application board will allow the Iout current flow.

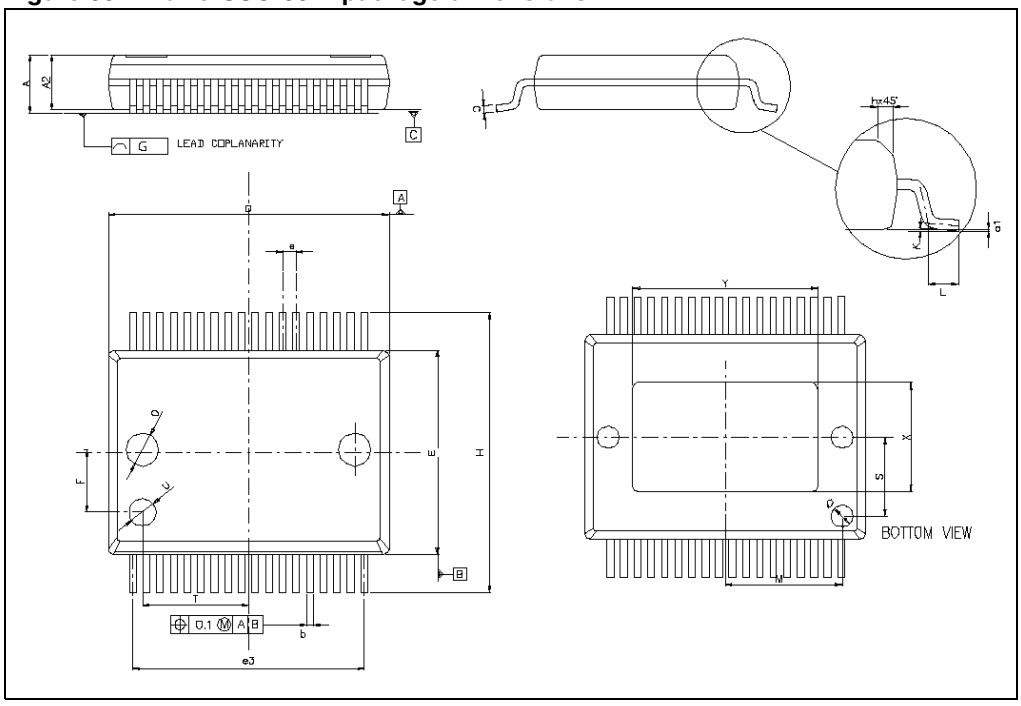
16 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 6. PowerSSO-36™ mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.075
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
M		4.3	
N			10deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X	4.1		4.7
Y	4.9		5.5

Figure 30. PowerSSO-36™ package dimensions



17 Revision history

Table 7. Document revision history

Date	Revision	Changes
02-May-2011	1	Initial release

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