LatticeECP3 PCI Express Solutions Board – Revision A

User's Guide

December 2010
Revision: EB43_01.1

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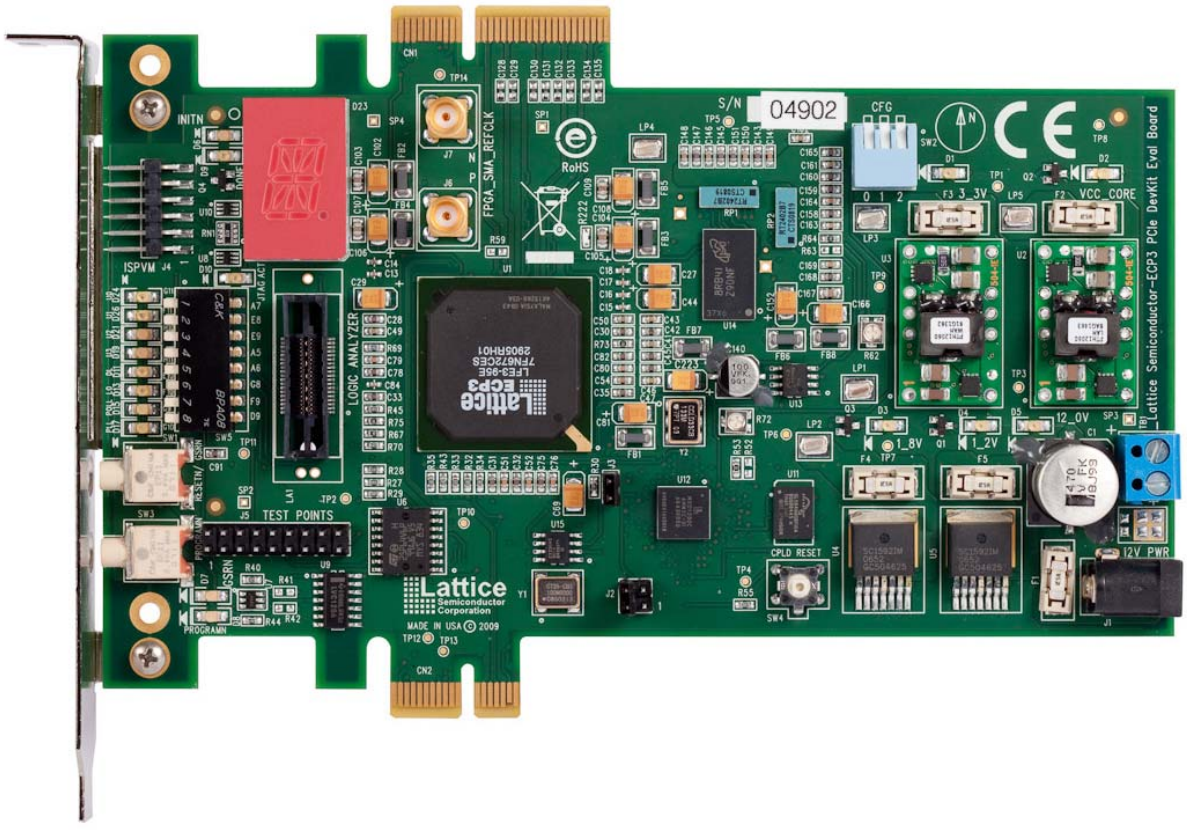
Introduction

As PCI Express applications have emerged, the LatticeECP3™ FPGA family has become a well-suited solution for many system designs. The features of the LatticeECP3 PCI Express Solutions Board can assist engineers with rapid-prototyping and testing their designs. The board is an enhanced form-factor of the PCI Express add-in card specification. It allows for full x1 form-factor compliance and x4 is available for demonstration purposes with some non-standard form-factor issues. The flexibility to use the same board to demonstrate both x1 and x4 configurations is accomplished by simply changing the mounting hardware. The board has several debugging and analyzing features for complete evaluation of the LatticeECP3 device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP3 FPGA.

This user's guide describes the LatticeECP3 PCI Express Solutions Board featuring the LatticeECP3 LFE3-95EA-FN672 FPGA. The stand-alone evaluation board provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to demonstrate PCI Express capabilities using an add-on card form-factor. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 85-ohm for differential traces.

Important: *This document (including the schematics in the appendix) describes LatticeECP3 PCI Express Solutions Boards marked as* ***Rev A****. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.*

Figure 1. LatticeECP3 PCI Express Solutions Board



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Features

- PCI Express x1 and x4 edge connector interfaces
- Allows demonstration of PCI Express (x 1and x4) interfaces
  - x1 is form-factor compliant and will fit a standard PC-equipped PCI Express motherboard socket
  - x4 is non-compliant but will demonstrate x4 functionality by a simple change to the hardware
- Allows control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
- On-board Boot Flash
  - Both Serial SPI Flash and Parallel Flash via MachXO™ programming bridge
- Shows interoperation with a high performance DDR2 memory component
- Includes driver based "run-time" device configuration capability via ORCAstra or PCI Express
- Switches, LEDs, displays for demo purposes
- Input connection for lab-power supply
- Power connections and power sources
- ispVM™ programming support
- On-board and external reference clock sources

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board.

Figure 2. PCI Express Solutions Board Outline Drawing, Top Side

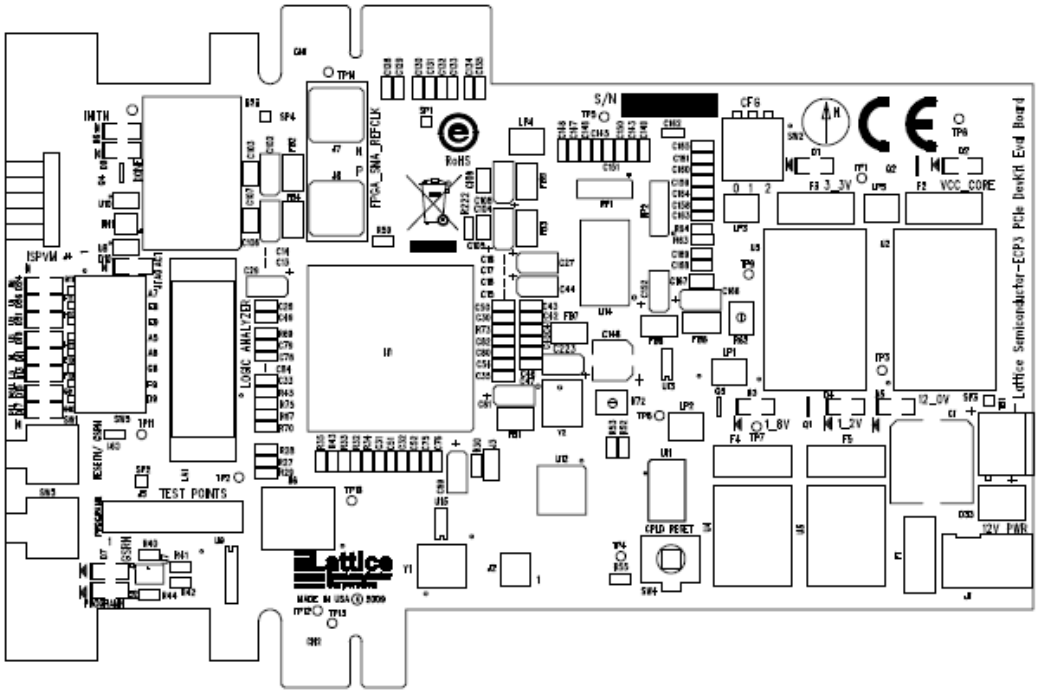

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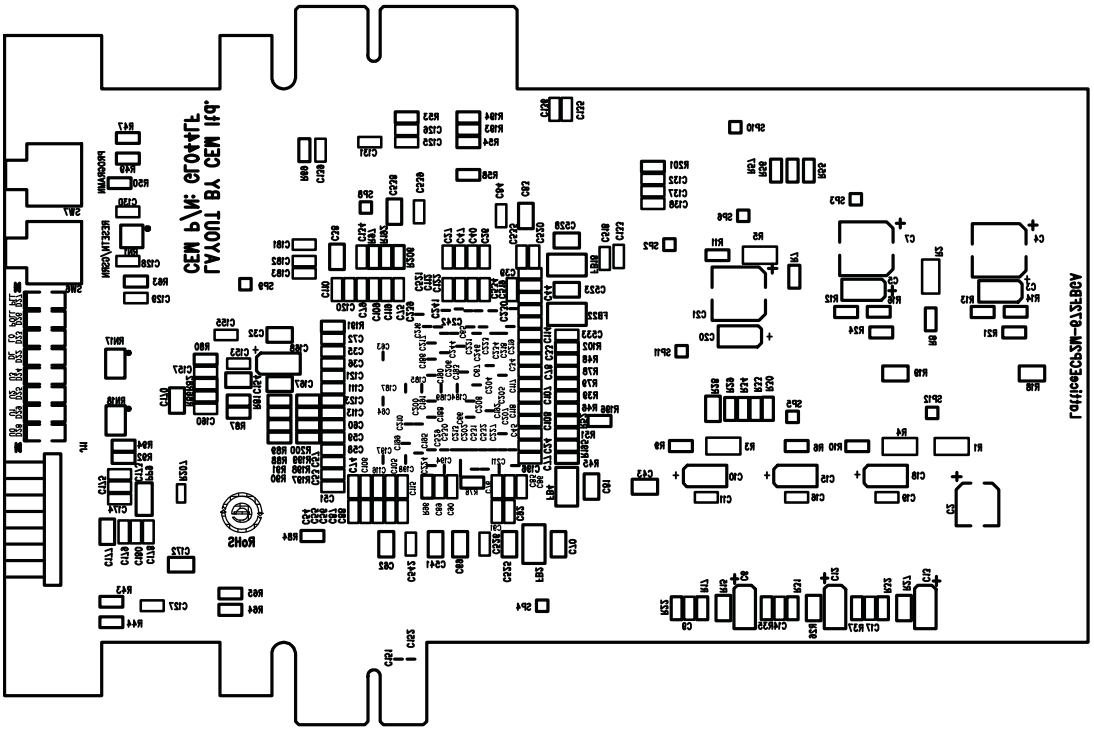
Figure 3. PCI Express Solutions Board Outline Drawing, Bottom Side

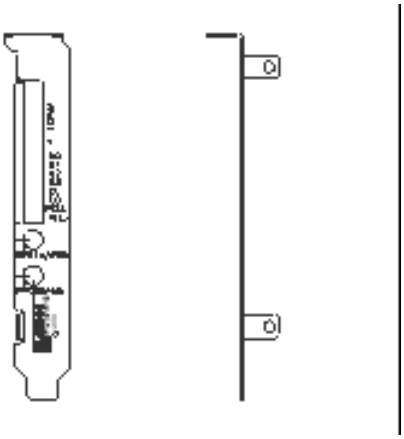


x1 and x4 PCI Express Support

PCI Express x1 and x4 is supported with the same PCB. This add-in PCB is designed to work in both types of motherboard slots. The PCB complies with the width and length dimensions of the PCI Express Card Electromechanical (CEM) Specification Revision 1.1. The only exclusion of the CEM specification is the component and back side of the add-in board may interfere with other boards in a fully-populated motherboard.

This board is easily interchanged from x1 to x4 configurations by removing the back-panel bracket and reinstalling it on the opposite side. This permits plug-in into PCI Express sockets on the motherboard and securing it in the chassis if desired. The back-panel bracket is shown below.

Figure 4. Back Panel Drawing



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LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP3 devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP3 Family Data Sheet on the Lattice website at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFE3-95EA-FN672 device. Available I/Os and associated sysI/O™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeECP3 PCI Express Solutions Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a benchtop supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J1 and plug the wall-transformer into an AC wall-outlet.

Power Supplies

(see Appendix A, Figure 21)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a benchtop supply adjusted to provide a nominal +12V DC.

All input power sources and on-board power supplies are fused with surface-mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses (see Appendix A, Figure 21)

F1	12V Fuse
F2	1.2V Core Fuse
F3	3.3V Fuse
F4	1.8V Fuse
F5	1.2V Analog Supply

Table 2. Board Power Supply Indicators (see Appendix A, Figure 21)

D1	3.3V Source Good Indicator
D2	1.2V VCC Core Source Good Indicator
D3	1.8V Source Good Indicator
D4	1.2V Analog Source Good Indicator
D5	12V Input Good Indicator

External power can be alternatively connected rather than the wall transformer power pack.

Table 3. External Board Supply Input Terminal (see Appendix A, Figure 21)

TB1	Screw terminal for +12V DC Pin1 (square PCB pad): +12V DC Pin2: Ground

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PCI Express Power Interface

Power can be sourced to the board via the PCB edge-fingers (CN1 and CN2). This interface allows the user to provide power from a PCI Express Host board.

Programming/FPGA Configuration

(see Appendix A, Figure 23)

A programming header is provided on the evaluation board, providing access to the LatticeECP3 JTAG port.

ispVM Download Interface

J4 and J8 are 6-pin JTAG connectors used in conjunction with the ispVM USB download cable to program and control the device. These connectors are available through the back-panel bracket as needed for x1 or x4 PCI Express configurations. These connectors are used in conjunction with the ispVM programming cable and software to program the configuration memory or FPGA directly.

Table 4. Standard ispVM Programming Cable Configuration

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	TMS
Pin 5	GND
Pin 6	TCK

After initial board setup, use the following procedure to program the evaluation board. Instructions assume ispVM software has been installed on a local PC.

Connect the ispDOWNLOAD cable rainbow colored flywires to the connector J4.

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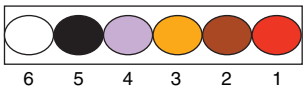
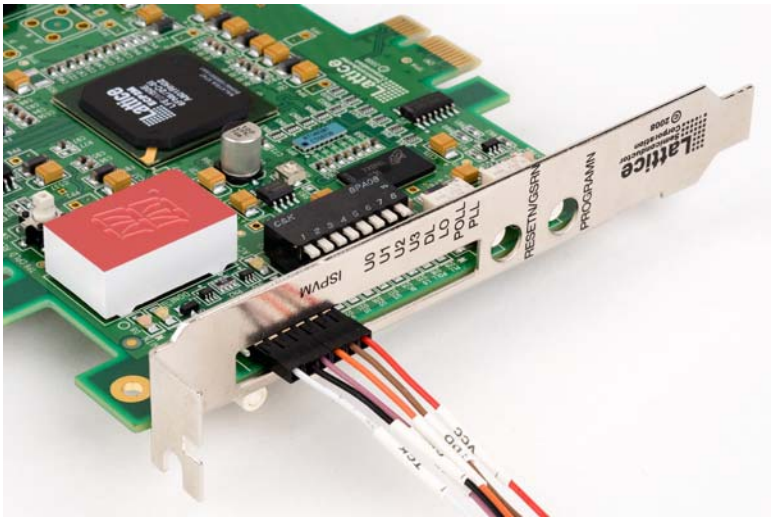
Table 5. ispVM JTAG Connector (see Appendix A, Figure 21)



Note: A dot denotes PIN 1 on the both the PCB or back-panel bracket.

Pin	Function	Color
1	PWR	Red
2	TDO	Brown
3	TDI	Orange
4	TMS	Purple
5	GND	Black
6	TCK	White

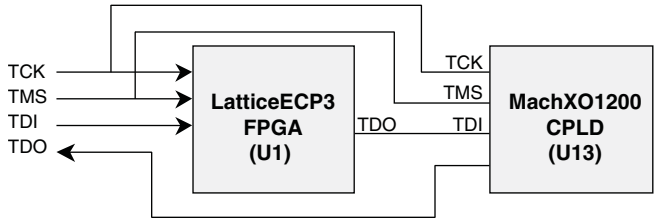
Figure 5. ispVM Programming Cable Connector



Programming the Daisy Chain

This board includes two Lattice Semiconductor programmable (U1=LFE3-95, U12=LCMXO1200) devices that can be programmed in a daisy chain.

Figure 6. JTAG Chain



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Download Procedures

Requirements:

- PC with ispVM System v.17.7 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

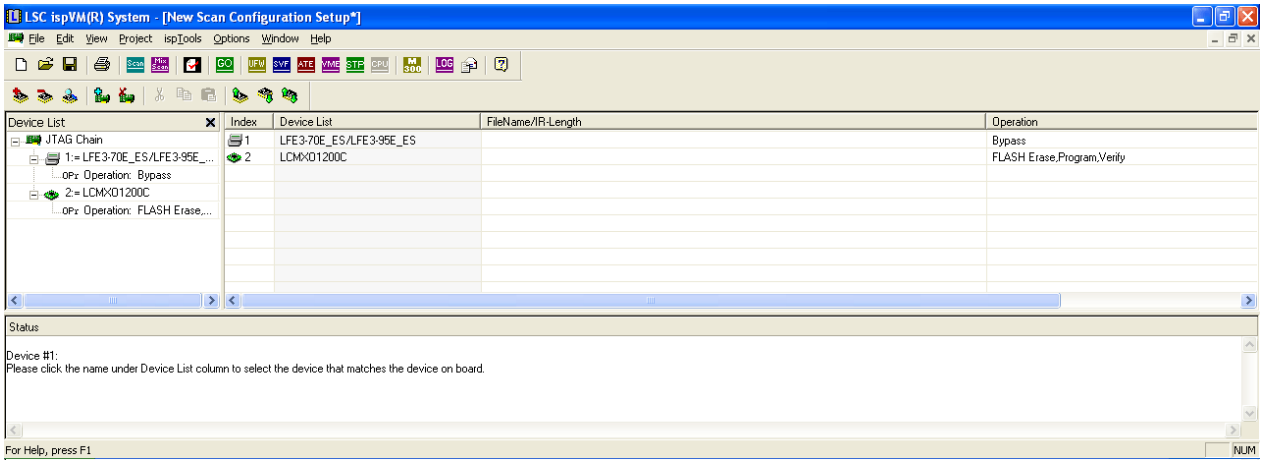
- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeECP3 device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the LatticeECP3 PCI Express Solutions Board to the appropriate power sources and power up board.
2. Connect the ispDOWNLOAD cable to the appropriate header. J4 is used for the 1x6 connection. J8 is used in the same manner for x4 configurations.
3. Start the ispVM System software.
4. Press the **SCAN** button located in the toolbar. The LatticeECP3 and the MachXO1200 devices should be automatically detected.

Figure 7. ispVM Main Window



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.
6. To program only the LatticeECP3-95, place the LCMXO1200C device into **BYPASS** and the LFE3-95 should be in **FAST PROGRAM** mode.

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Figure 8. ispVM Fast Programming Mode

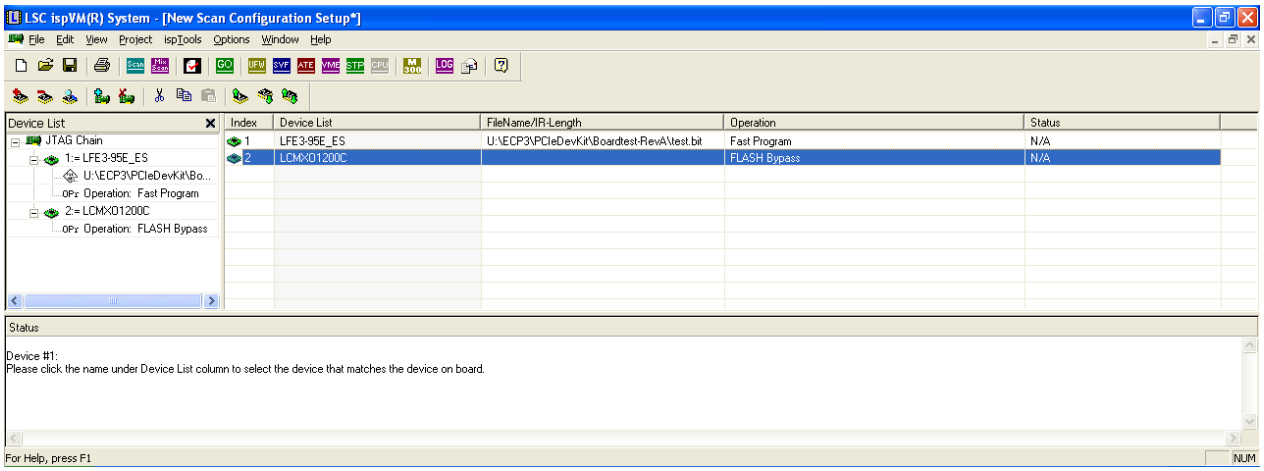
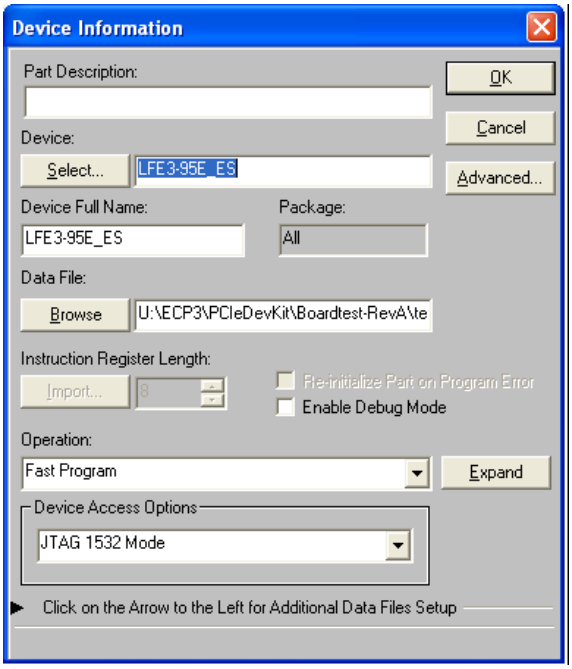


Figure 9. ispVM Device Information Dialog Box



7. Add Data File.
8. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators
(see Appendix A, Figure 23)

These LEDs indicate the status of configuration to the FPGA.

- D6 (red) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.
- D9 (green) is illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.

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- D10 (green) will flash indicating TDI activity.
- D8 (red) illuminated, this indicates that PROGRAMN is low.
- D7 (red) illuminated, this indicates that GSRN is low.

PROGRAMN & GSRN
(see Appendix A, Figure 23)

- These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3 or SW7) and GSRN (SW1 or SW6). Depressing the button drives a logic level "0" to the device.
- These push-buttons are accessible from the back panel if the evaluation board is mounted in a PCI Express slot of a PC.

CFG [2:0]
(see Appendix A, Figure 23)

- The FPGA CFG pins are set on the board for a particular programming mode via the SW2 DIP switch.
- JTAG programming is independent of the MODE pins and is always available to the user.
- Pushing in (depressing) the switch is ON and sets the value to 0.

Table 6. CFG Mode Selections

CFG2	CFG1	CFG0	Configuration Mode
0 (ON)	0 (ON)	0 (ON)	SPI Flash
0 (ON)	1 (OFF)	0 (ON)	SPIm
1 (OFF)	0 (ON)	1 (OFF)	Slave Serial
1 (OFF)	1 (OFF)	1 (OFF)	Slave Parallel
X (don't care)	X (don't care)	X (don't care)	ispJTAG™

On-Board Serial SPI Flash Memory
(see Appendix A, Figure 23)

- One Serial SPI (16-pin tssop 64M) Flash memory device (U6) is on-board for non-volatile configuration memory storage. Either a STMicro M25P64VMF16 or Macronix MX25L6405 device is populated on-board.
- All CFG [2:0] need to be [000] depressed to read the Flash memory at power-up or after toggling the PROGRAMN pin.
- Install jumper across pins 2 and 4 on J2.

Programming Serial SPI Flash Memory
The Serial SPI Flash memory device can be configured easily via its JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

1. Connect the LatticeECP3 PCI Express Solutions Board to the appropriate power sources and power-up board.
2. Connect the ispDOWNLOAD cable to the appropriate header. J4 is used with the cable.
3. Start the ispVM System software.
4. Press the **SCAN** button located in the toolbar. The LFE3-95 and the LCMXO1200C devices should be automatically detected.

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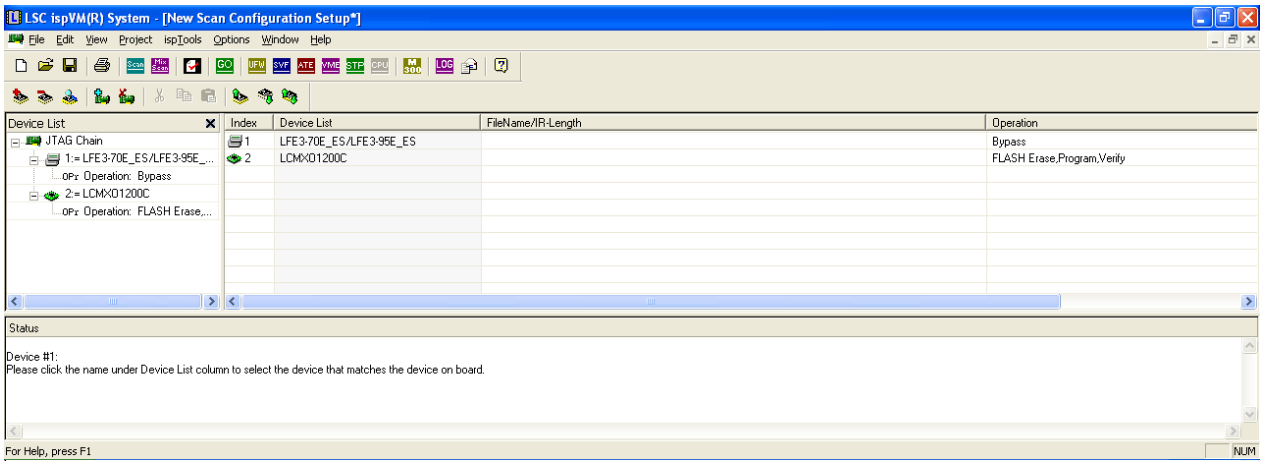
Figure 10. Results of Scanning Board via ispVM



5. Double-click the **Operation** column for the LFE3-95 and the Device Dialog box shown below will open.

6. In the dialog box, select the **SPI Flash Programming** mode in the **Device Access Options** pull-down menu. This will open the SPI Serial Flash Dialog box.

Figure 11. Device Information Dialog Screen

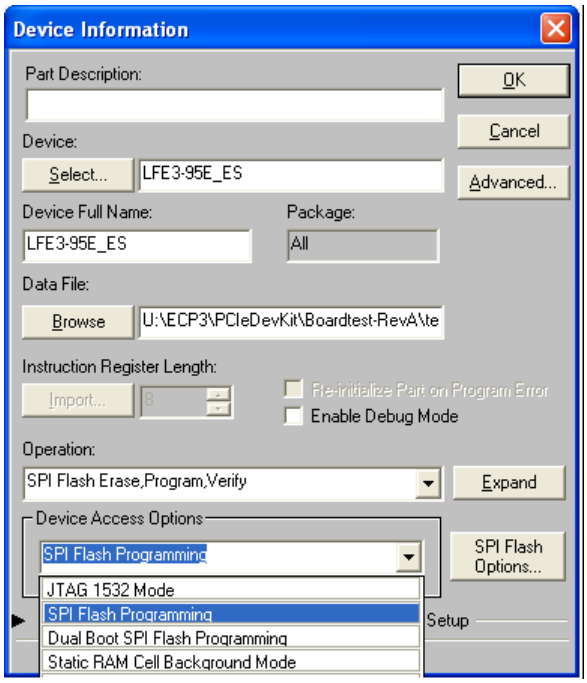


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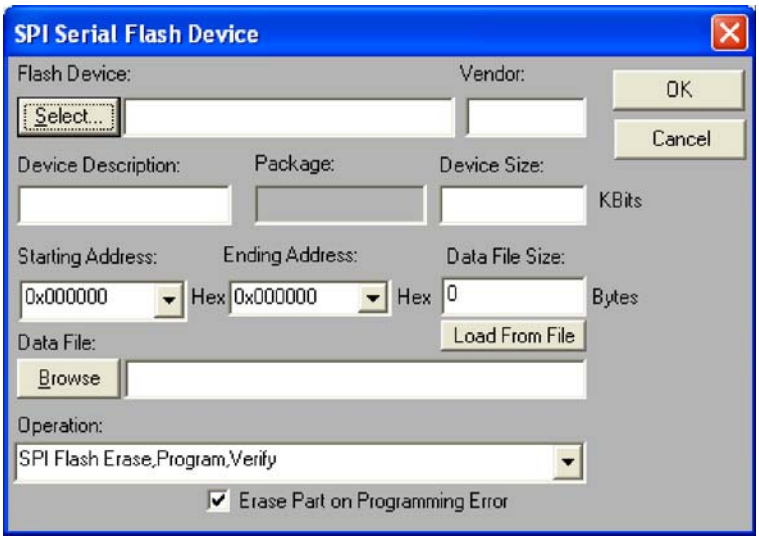
Figure 12. SPI Serial Flash Dialog Screen



7. The SPI Serial Flash Device dialog box will open. In this box select **SPI Flash Erase, Program, Verify** in the **Operation** pull-down menu.

8. Select **SPI Serial Flash** in the **Device Family** pull-down menu, **STMicro** under the **Vendor** pull-down menu, **SPI-M2564** under the **Device** pull-down menu, and **16-lead SOIC** under the **Package** submenu.

Figure 13. Select Device Dialog Box

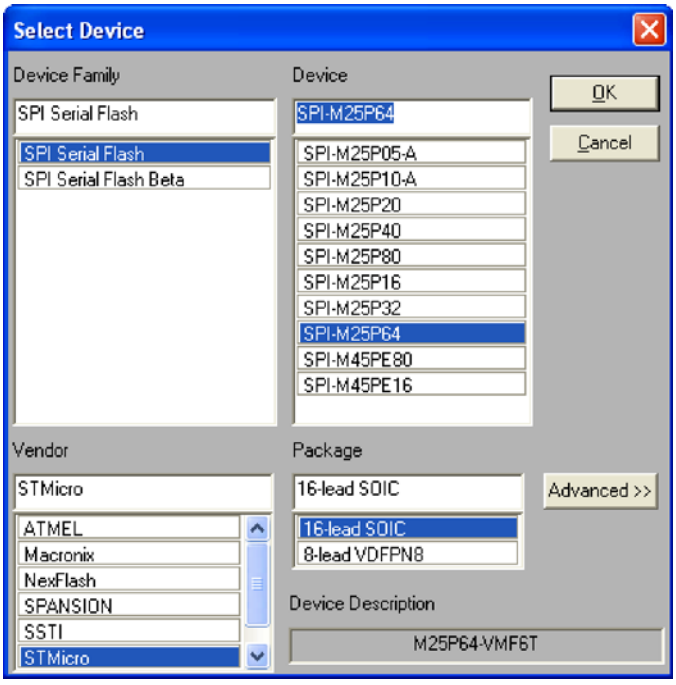


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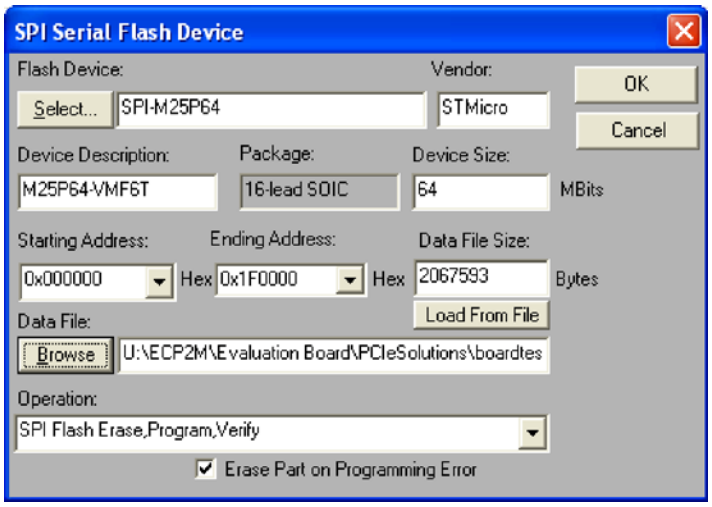
Figure 14. Sample SPI Serial Flash Device Dialog Box



9. Click **OK** in the **SPI Flash Device** dialog box. Then click **OK** in the **Select Device** dialog box. You will then return to the main configuration screen. If you do not desire to load the LCMXO1200C device, this device should be placed in Flash Bypass mode by double-clicking the **Operation** column and selecting the **Bypass** operation shown below.

Figure 15. FLASH Bypass for LCMXO1200C Device

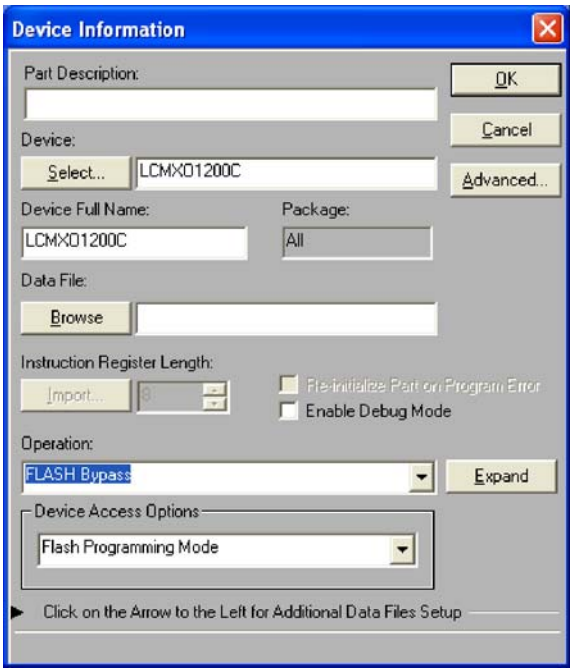


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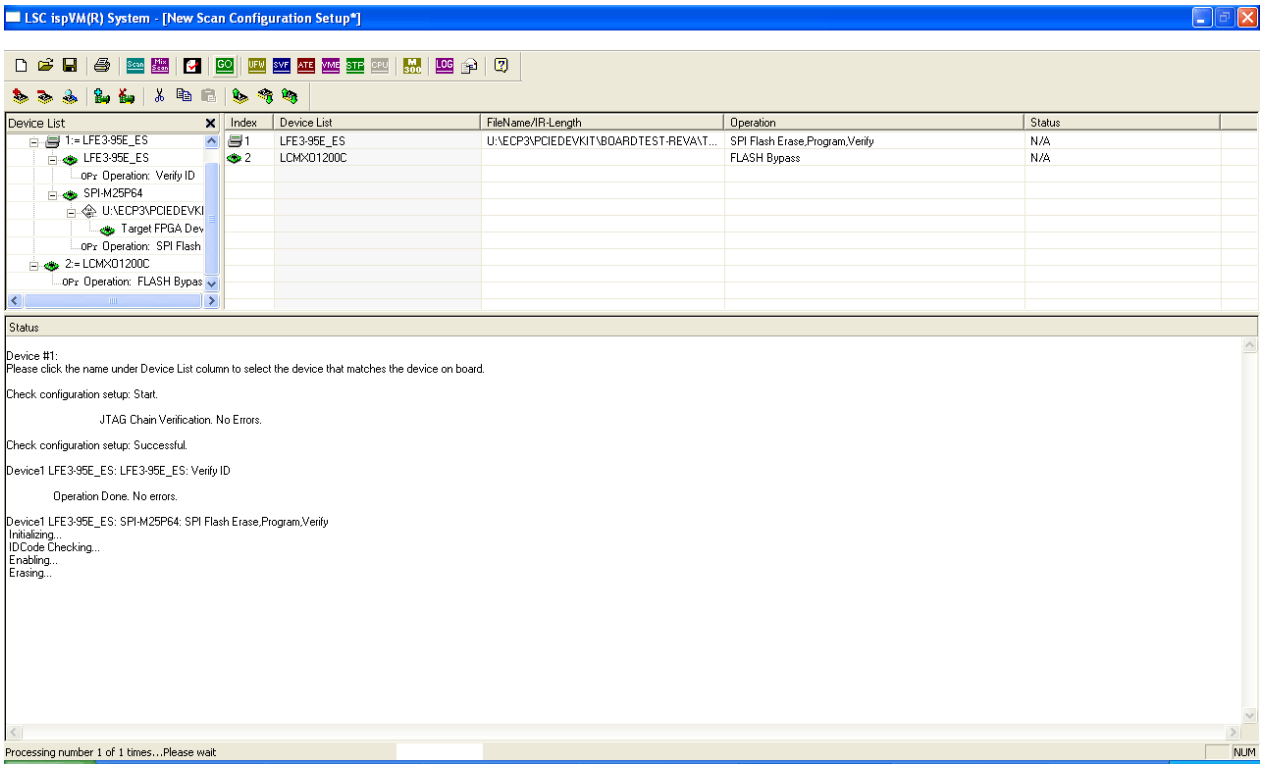
Figure 16. Programming Main Window



10. From the main programming window, select **GO** in the top toolbar. This will begin the SPI Serial Flash programming.

Figure 17. SPI Serial Flash Programming Status Window

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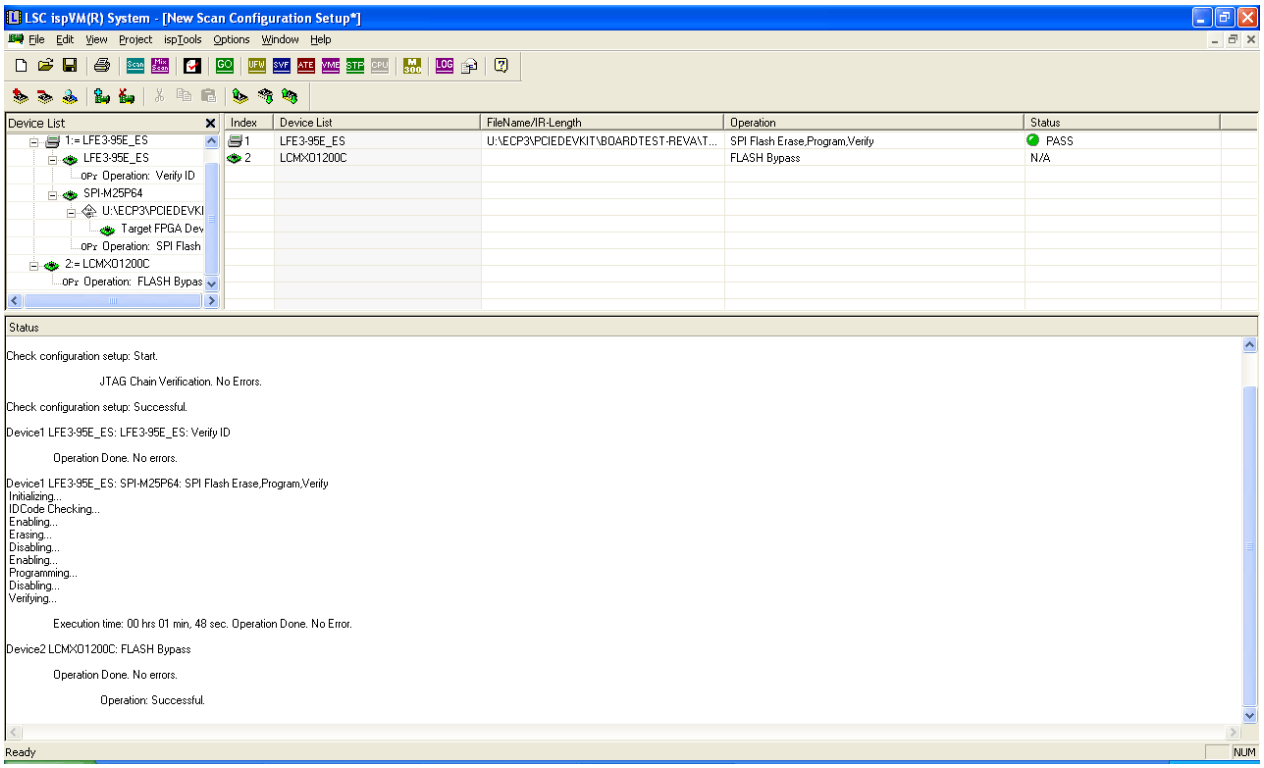
Figure 18. Successful SPI Serial Flash Programming Session



On-Board Parallel SPI Flash Memory

(see Appendix A, Figure 24)

- A 16-bit parallel Flash device is also available. This board uses a Lattice MachXO CPLD device to act as a programming bridge from the Flash device.
- The CFG [2:0] need to be [111], all up.
- Lattice ispVM programming software can be used to program either the serial SPI Flash or the parallel Flash devices. Application note AN8077, *Parallel Flash Programming and FPGA Configuration,* addresses the use of the parallel Flash implementation. *Note: For parallel Flash loading, the board needs the appropriate connections of J2. J2 requires a jumper be installed between pins 1 and 3.*

User-Defined General Purpose Clock Oscillator

(see Appendix A, Figure 27, Y1)

A 100MHz oscillator is included on-board. It is fanned-out to several destinations on the board, as described in Table 7.

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Table 7. 100MHz Clock Destinations

Clock Destination	PCB Designation	Destination Pin
CPLD	U12	A8
FPGA	U1	P21-PCLKT2_0
FPGA	U1	K3-LLUM0-GDLLT_IN
FPGA	U1	M4-PCLKT7_0

SERDES

(see Appendix A, Figure 25)

SERDES/FPGA Reference Clocks

The 50-ohm terminated SMA connectors are optionally provided to supply reference clocks directly to the LatticeECP3 device. Please contact the factory for information to populate the PCB with SMA connectors.

Table 8. SMA Inputs for External Clock Source

Connector	SERDES Signal	FPGA Pin
J6	FPGA_SMA_REFCLKP	V20
J7	FPGA_SMA_REFCLKN	W19

SERDES PCI Express Channels

(see Appendix A, Figure 25)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1 or CN2) that fit directly into a PCI Express host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

Table 9. x1 PCI Express Connections

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSA_HDOUTP_0	AF21	PERp0	A16	Integrated endpoint block transmit pair
PCSA_HDOUTN_0	AF20	PERn0	A17	
PCSA_HDINP_0	AD21	PETp0	B14	Integrated endpoint block receive pair
PCSA_HDINN_0	AD20	PETn0	B15	
PCSA_REFCLKP	AC17	PCIe_CLKp	A13	Integrated endpoint block differential clock pair
PCSA_REFCLKN	AC18	PCIe_CLKn	A14	
PCIE_PERSETN	U20	PERSTN	A11	Fundamental PCI Express reset

Table 10. x4 PCI Express Connections

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSB_HDOUTP_0	AF13	PERp0	A16	Integrated endpoint block transmit pair
PCSB_HDOUTN_0	AF12	PERn0	A17	
PCSB_HDINP_0	AD13	PETp0	B14	Integrated endpoint block receive pair
PCSB_HDINN_0	AD12	PETn0	B15	
PCSB_HDOUTP_1	AF10	PERp1	A21	Integrated endpoint block transmit pair
PCSB_HDOUTN_1	AF11	PERn1	A22	
PCSB_HDINP_1	AD10	PETp1	B19	Integrated endpoint block receive pair
PCSB_HDINN_1	AD11	PETn1	B20	

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Table 10. x4 PCI Express Connections (Continued)

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSB_HDOUTP_2	AF9	PERp2	A25	Integrated endpoint block transmit pair
PCSB_HDOUTN_2	AF8	PERn2	A26	
PCSB_HDINP_2	AD9	PETp2	B23	Integrated endpoint block receive pair
PCSB_HDINN_2	AD8	PETn2	B24	
PCSB_HDOUTP_3	AF6	PERp3	A29	Integrated endpoint block transmit pair
PCSB_HDOUTN_3	AF7	PERn3	A30	
PCSB_HDINP_3	AD6	PETp3	B27	Integrated endpoint block receive pair
PCSB_HDINN_3	AD7	PETn3	B28	
PCSB_REFCLKP	AC9	PCIe_CLKp	A13	Integrated endpoint block differential clock pair
PCSB_REFCLKN	AC10	PCIe_CLKn	A14	
PCIE_PERSETN	U20	PERSTN	A11	Fundamental PCI Express reset

FPGA Test Pins
(see Appendix A, Figure 27)

General Purpose DIP Switch
(see Appendix A, Figure 27, SW5)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to a switch (SW5) which is an SPST side actuated DIP switch. The switch is physically located on the secondary side of the PCB along the back-panel edge. The switches are connected to a logic level 0 when depressed toward the board and a 1 when away from the board. The designated pins are connected according to Table 11.

Table 11. FPGA Test Pins (See Appendix A, Figure 26)

FPGA BGA	SW5 Switch Position
D9	1
F9	2
G8	3
A6	4
A5	5
E9	6
E8	7
A7	8

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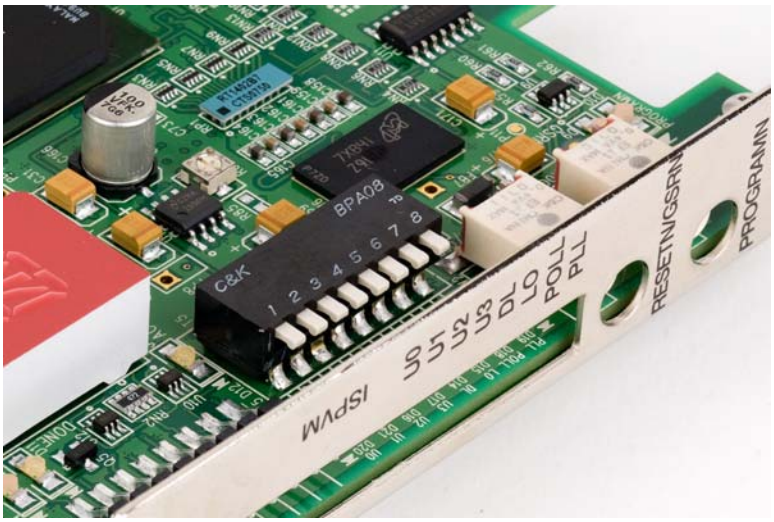
Figure 19. 8-position DIP Switch (SW5) on Secondary PCB Side



General Purpose LEDs
(see Appendix A, Figure 27)

LEDs are provided along the back panel edge of the PCB. These LEDs are connected to general-purpose FPGA I/Os. The LEDs are illuminated by the associated FPGA outputs being driven to a valid LOW level. The use of these LEDs is defined for PCI Express applications to observe the status of the PCI Express link during operation. The LEDs must be included in the FPGA design. These status LEDs are available in both x1 or x4 configurations. The back panel marking reflects PCI Express specific status.

Table 12. LED Definitions

PCI Express x1		PCI Express x4		
FPGA Pin#	**PCB Designator**	**FPGA Pin#**	**PCB Designator**	**Description**
H11	D19	C10	D20	User defined
H10	D21	A9	D22	User defined
F11	D26	A10	D27	User defined
G11	D24	B10	D25	User defined
D10	D11	D10	D12	Data link up active
F10	D13	A8	D14	L0 state active
G9	D15	B8	D16	Polling state inactive
G10	D17	C9	D18	PLL locked

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General-Purpose Header
(see Appendix A, Figure 27, J5)

A 2x9 header (J5) provides a general-purpose connection to communicate with general purpose FPGA I/Os.

Table 13. General Purpose Header Connections

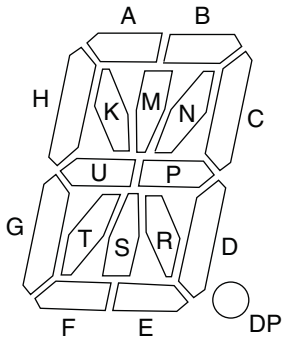
Header Pin	FPGA Pin	Header Pin	FPGA Pin
1	GND	2	GND
3	C15	4	E15
5	B15	6	E14
7	C14	8	A20
9	D14	10	A19
11	B16	12	C17
13	C16	14	B17
15	F13	16	A18
17	F14	18	A17

17-Segment LED Display
(see Appendix A, Figure 27, D13)

General-purpose FPGA pins are connected to a 17-segment display according to Table 14. These pins can be driven low to illuminate the display segments.

Table 14. 17-Segment LED Display

Segment	BGA
A	B7
B	F8
C	F7
D	A4
E	A3
F	H8
G	G7
H	C8
K	D8
M	B4
N	C5
P	C6
R	D6
S	C4
T	D5
U	C7
DP	B6



Logic Analyzer Probe
(see Appendix A, Figure 27, LA1)

An AMP/TYCO 767004 38-position .025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 34 general I/O signals to be observed on a Logic Analyzer probe using Mictor connections such as the Agilent 5346A.

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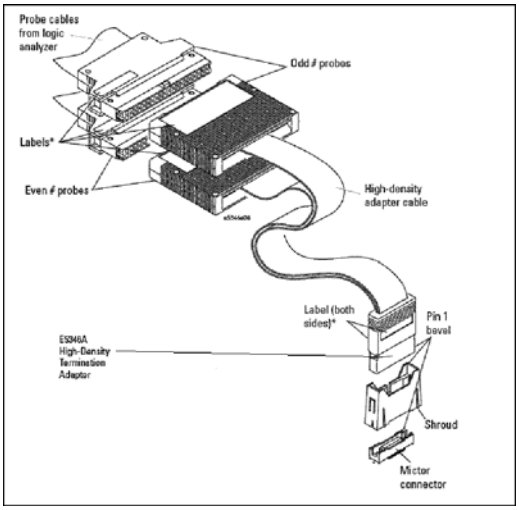
Table 15. Logic Analyzer To FPGA Pin Reference

Signal	FPGA Pin	Signal	FPGA Pin
LA1	AA25	LA2	Y24
LA3	W23	LA4	W22
LA5	AA26	LA6	AB26
LA7	W21	LA8	W20
LA9	AD26	LA10	AD25
LA11	AA24	LA12	AA23
LA13	AC26	LA14	AC25
LA15	Y19	LA16	Y20
LA17	AB24	LA18	AC24
LA19	Y22	LA20	AA22
LA21	AE25	LA22	AF24
LA23	AD24	LA24	AE24
LA25	AD23	LA26	AC23
LA27	AB20	LA28	AB21
LA29	AF23	LA30	AE23
LA31	W17	LA32	AB23
LA33	AB22	LA34	Y21



DDR2 Memory Devices
(see Appendix A, Figure 26, U14)

- The LatticeECP3 PCI Express Solutions Board is equipped with a 84-ball BGA DDR2 SDRAM memory device such as a Micron MT47H16M16BG-3 device.
- The DDR2 memory interfaces include a 16-bit wide device.
- The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP3 device.

CPLD Device
(see Appendix A, Figure 24, U12)

The board includes a Lattice Semiconductor LCMXO-1200C CPLD. This device is used in conjunction with the parallel Flash device for loading the configuration memory of the FPGA. It is also used for general-purpose board management functions. It has several connections to the FPGA and other devices on the PCB. It includes an active high, push-button (SW4) if needed for a user design.

Generic user-defined interconnections are defined in Table 16.

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Table 16. CPLD TO FPGA Interconnections

CPLD Pin	FPGA Pin
M1	B2
P13	B3
P10	D4
N7	E4
N8	C3
P11	D3
N13	G5
N1	G6
N3	E3
N4	F4
P1	H6
M12	J6
M2	C2
M3	D2
M4	K8
M6	J7

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP3 PCI Express Development Kit (Includes LatticeECP3 PCI Express Solutions Board)	LFE3-95EA-PCIE-DKN	

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
March 2010	01.0	Initial release.
December 2010	01.1	LED definitions table, L0 state changed from active to inactive.
		Download Procedures section, changed ispVM requirement from ispVM v.17.4 (or later) to ispVM v.17.7 (or later).

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Appendix A. Schematic

Figure 20. Cover Page

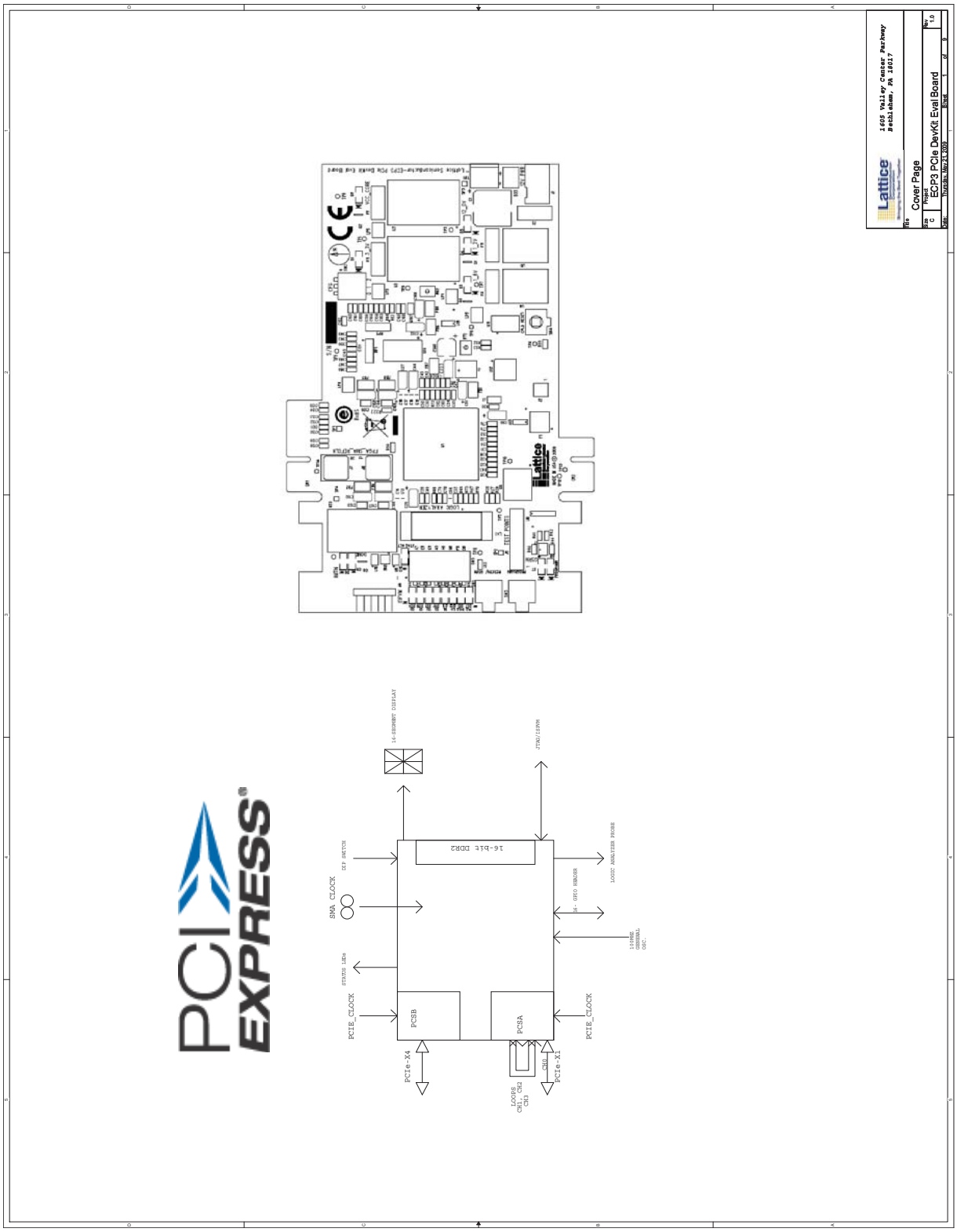

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Figure 21. Power Generation

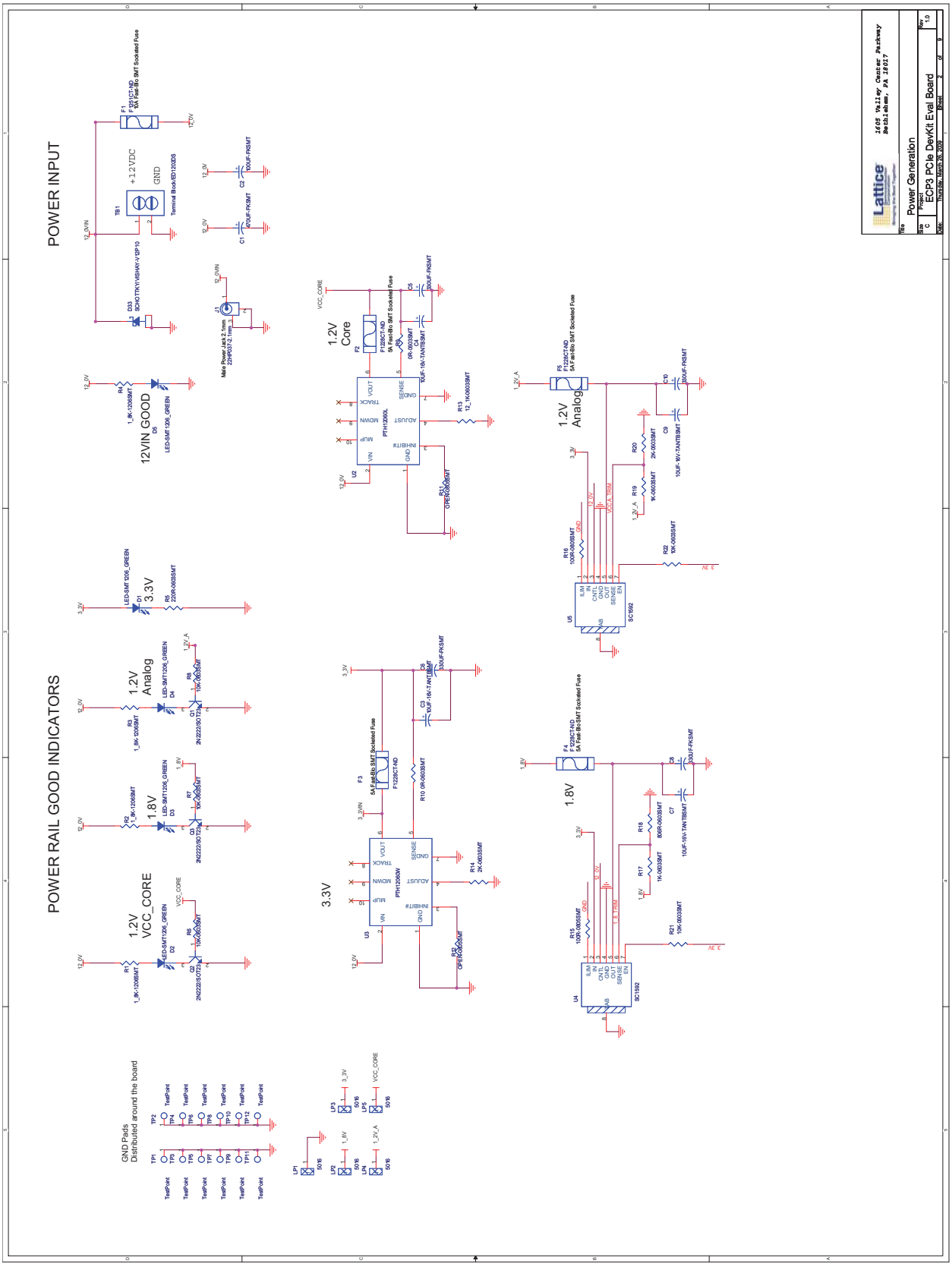

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Figure 22. Power Supplies

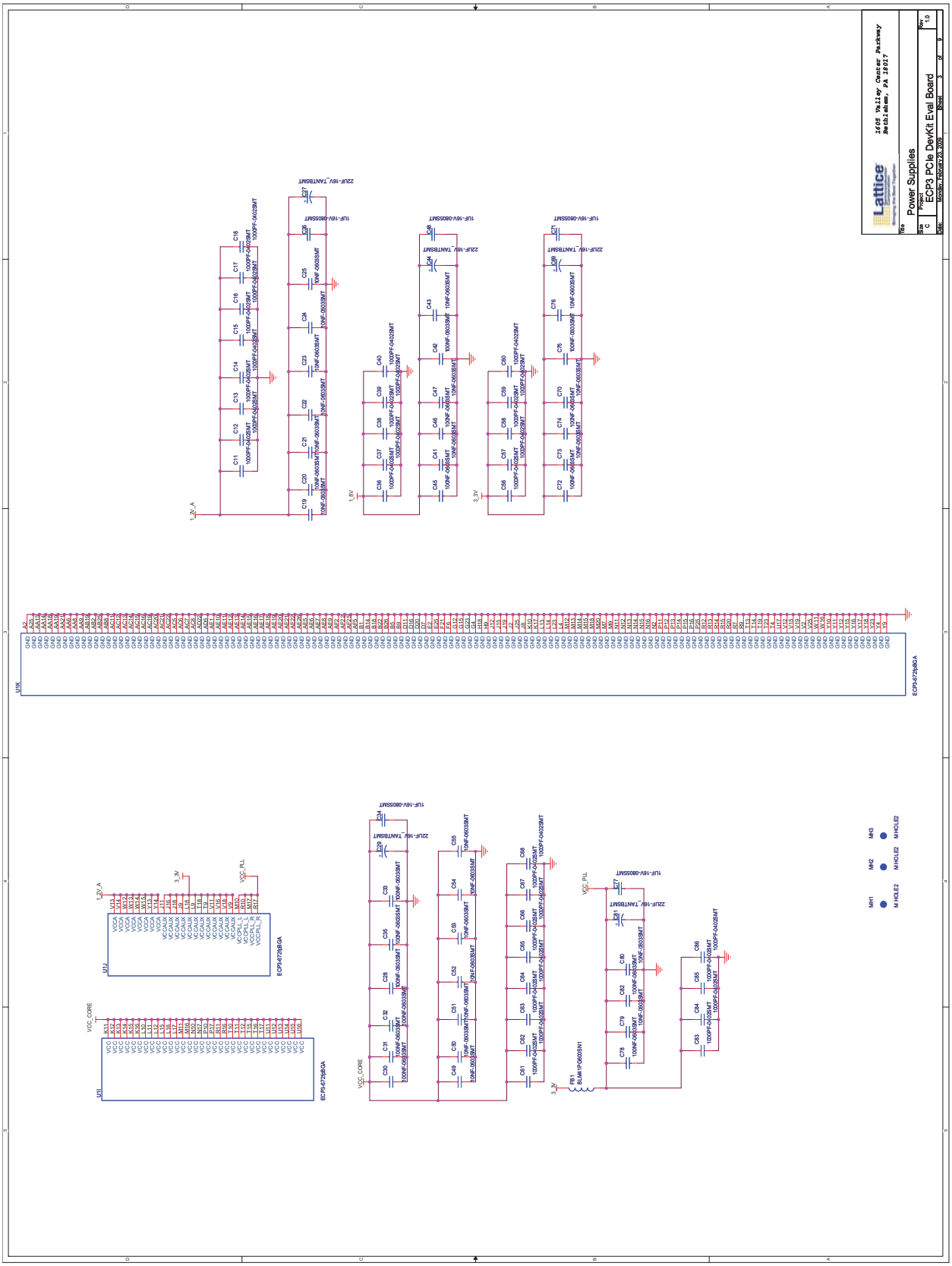

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Figure 23. Programming

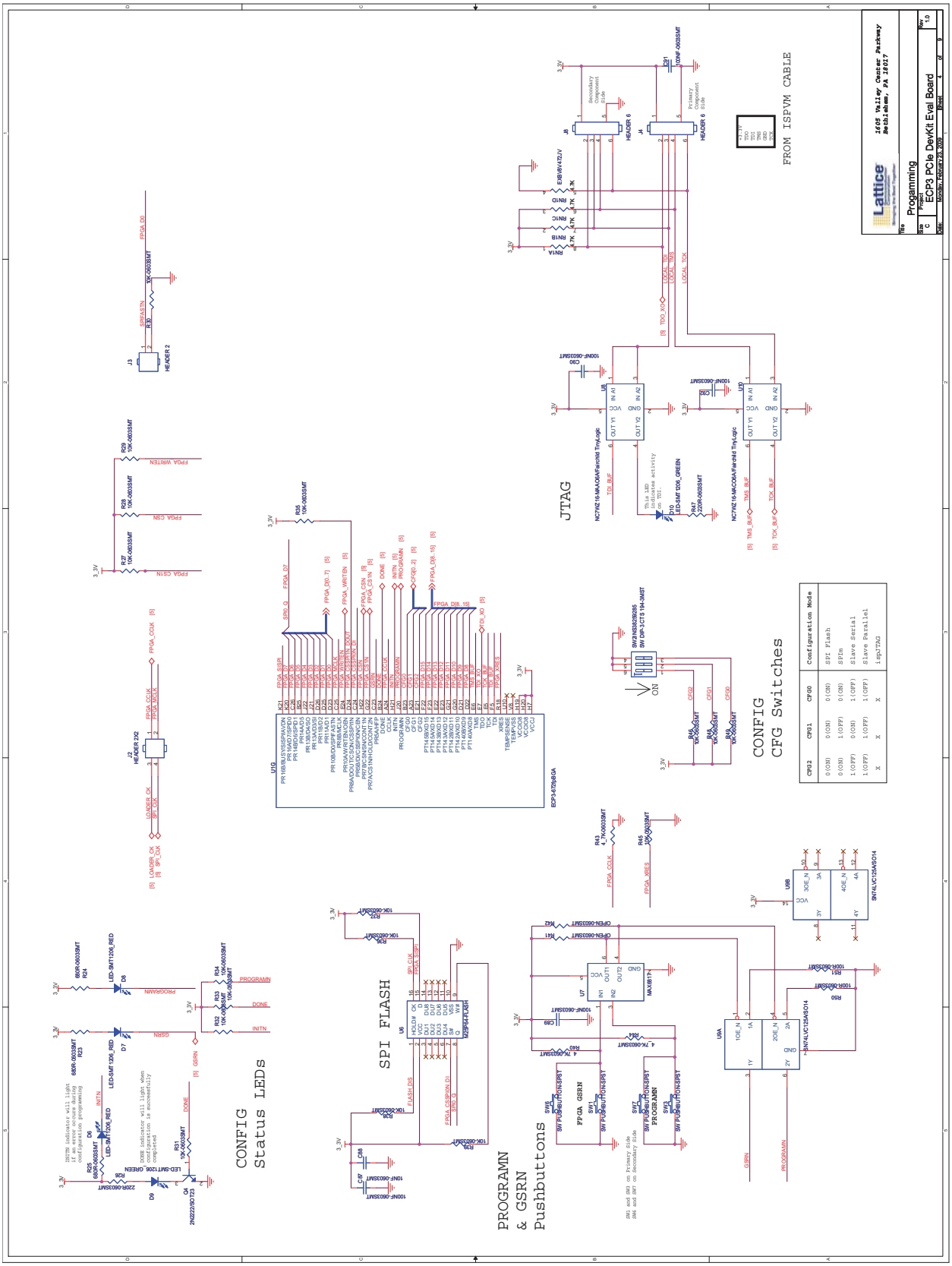

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Figure 24. Parallel FPGA Loader

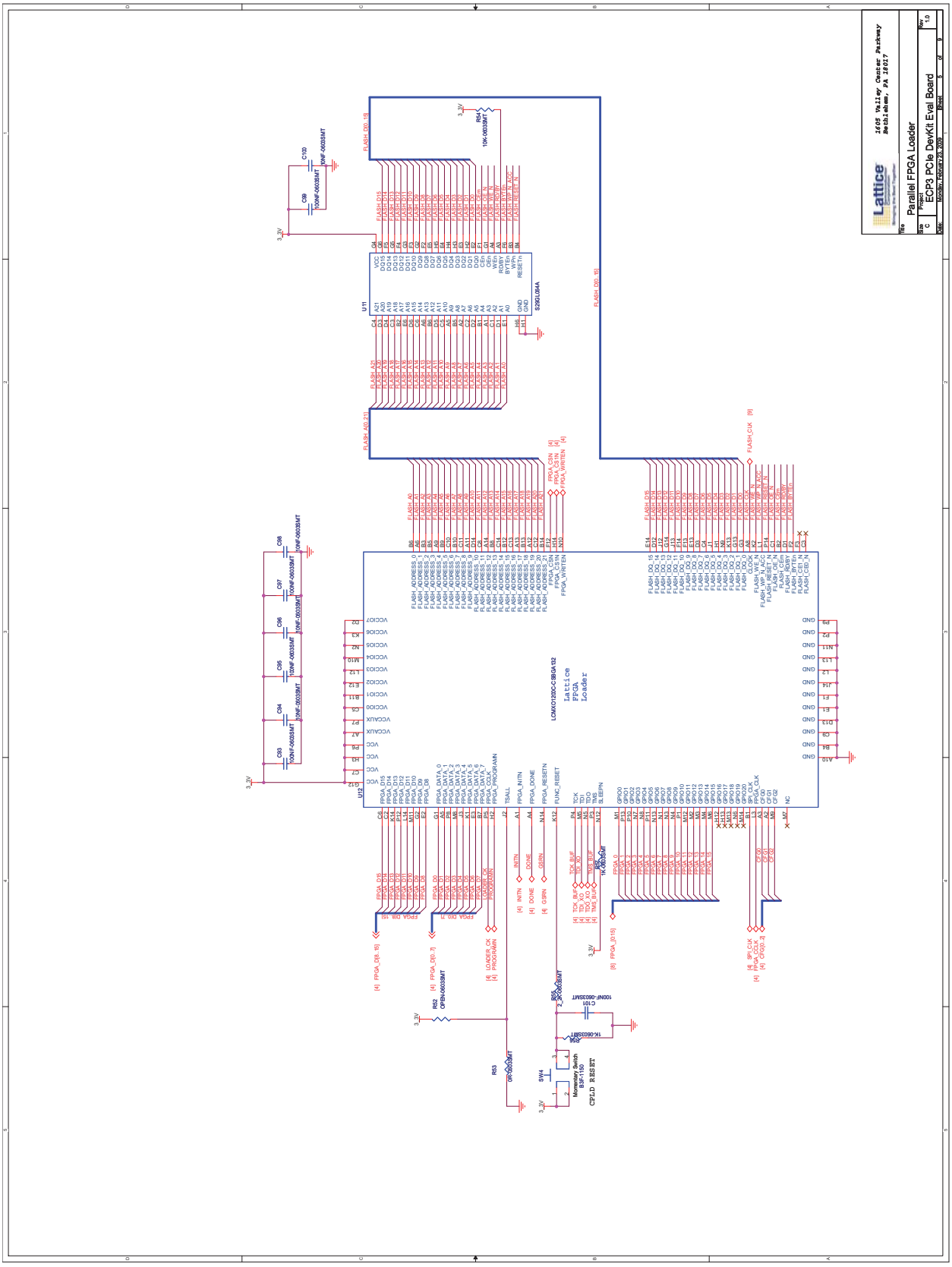

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Figure 25. SERDES

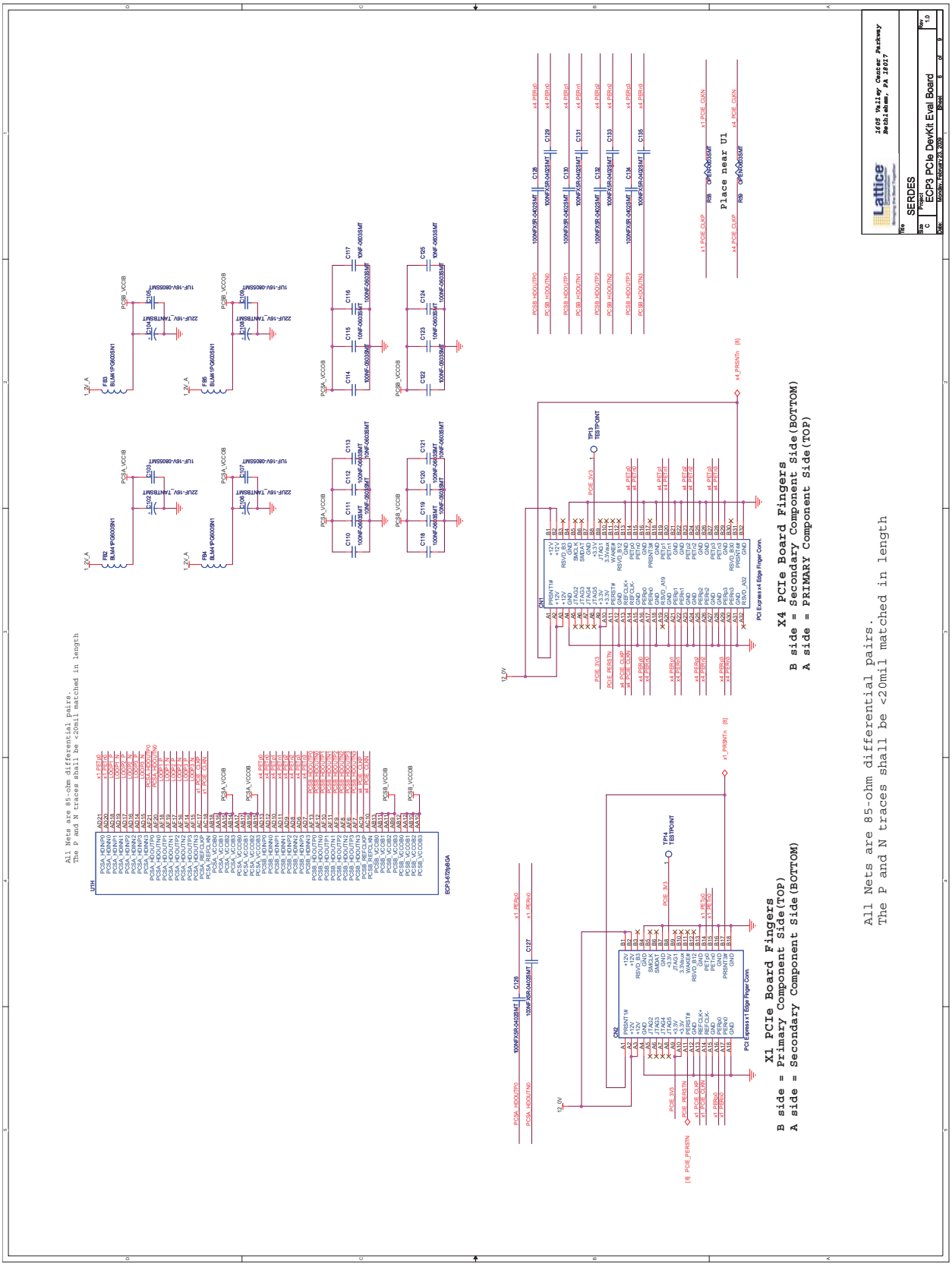

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Figure 26. DDR2 Memory

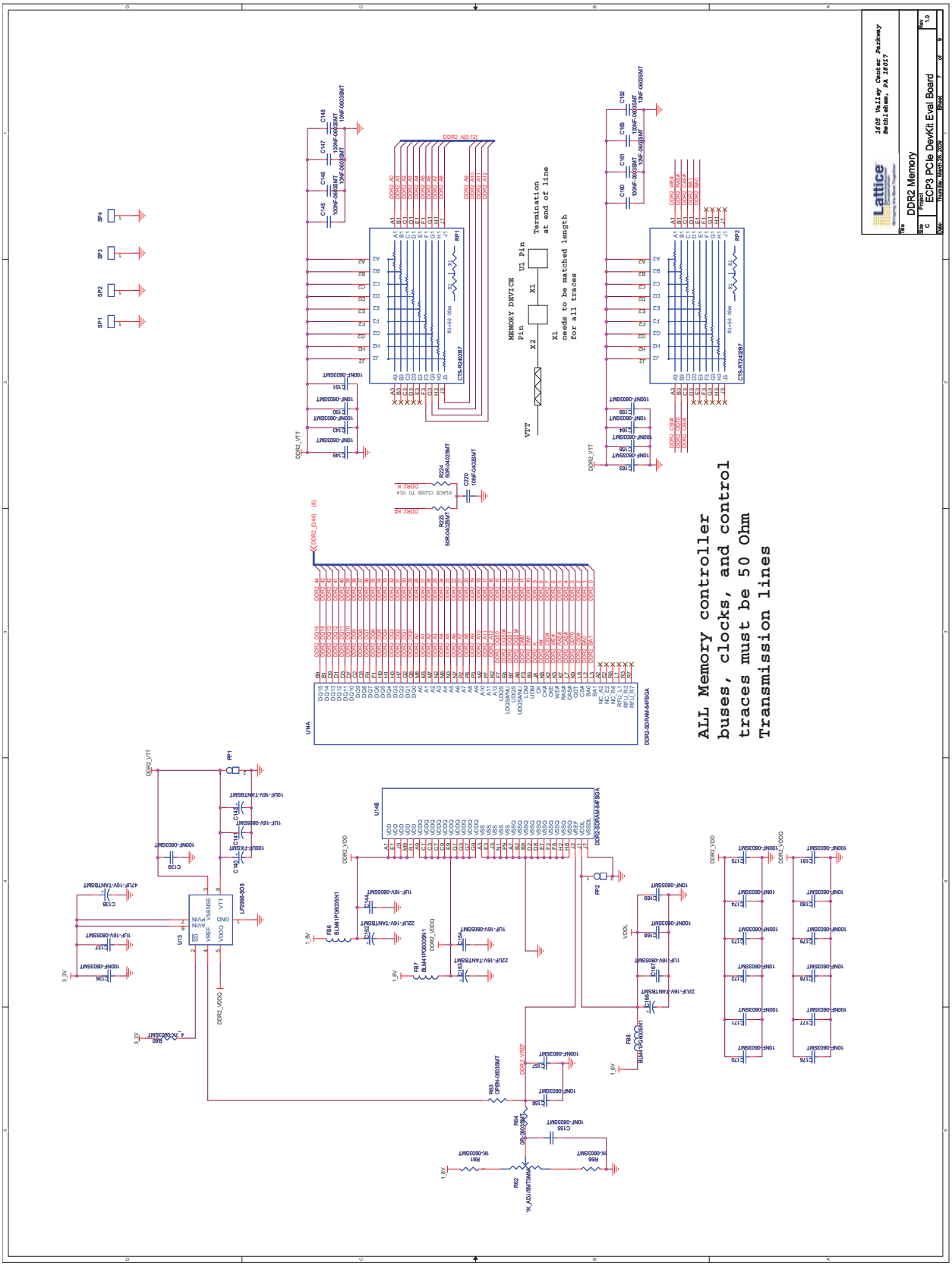

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Figure 27. FPGA Test

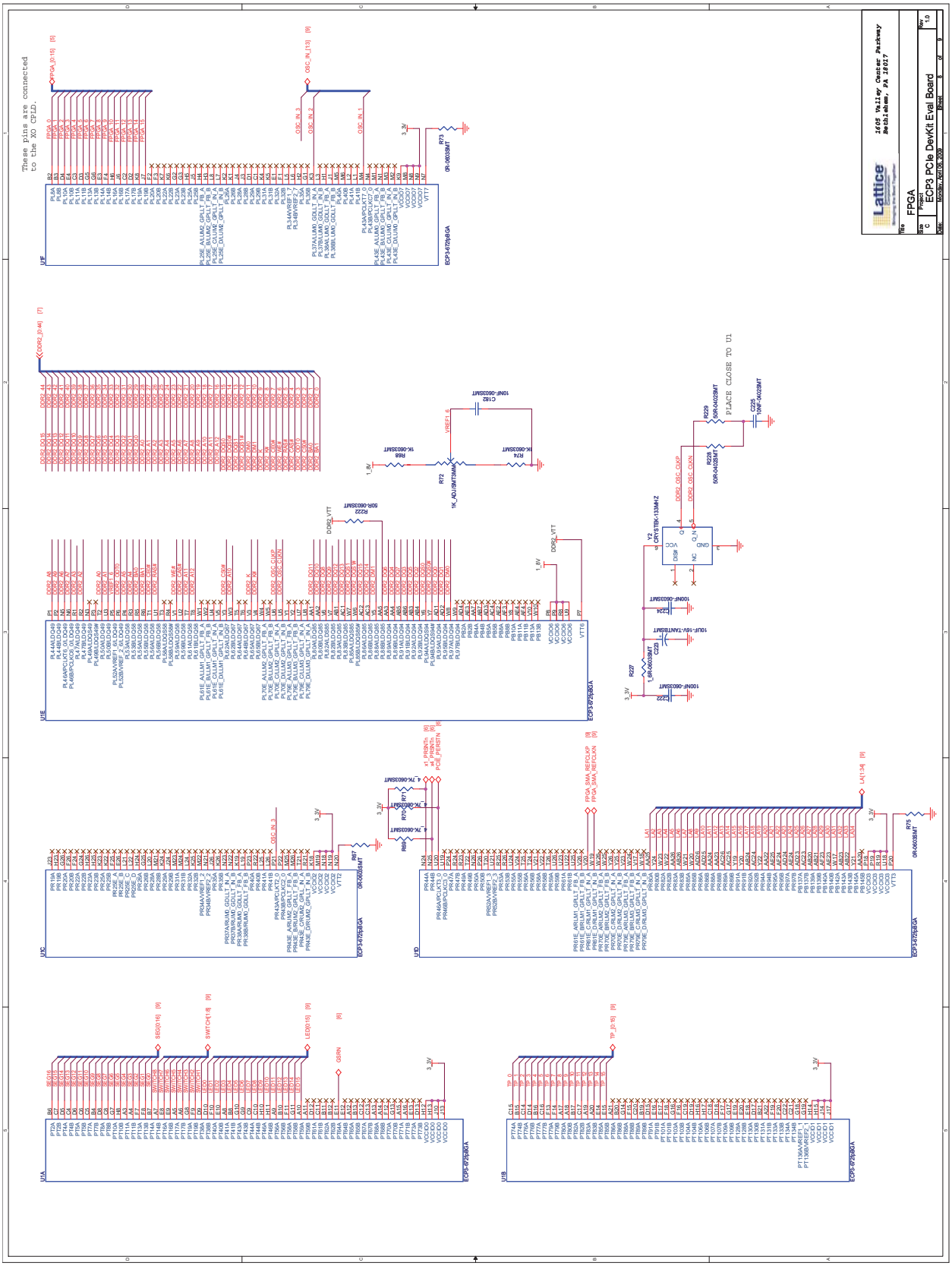

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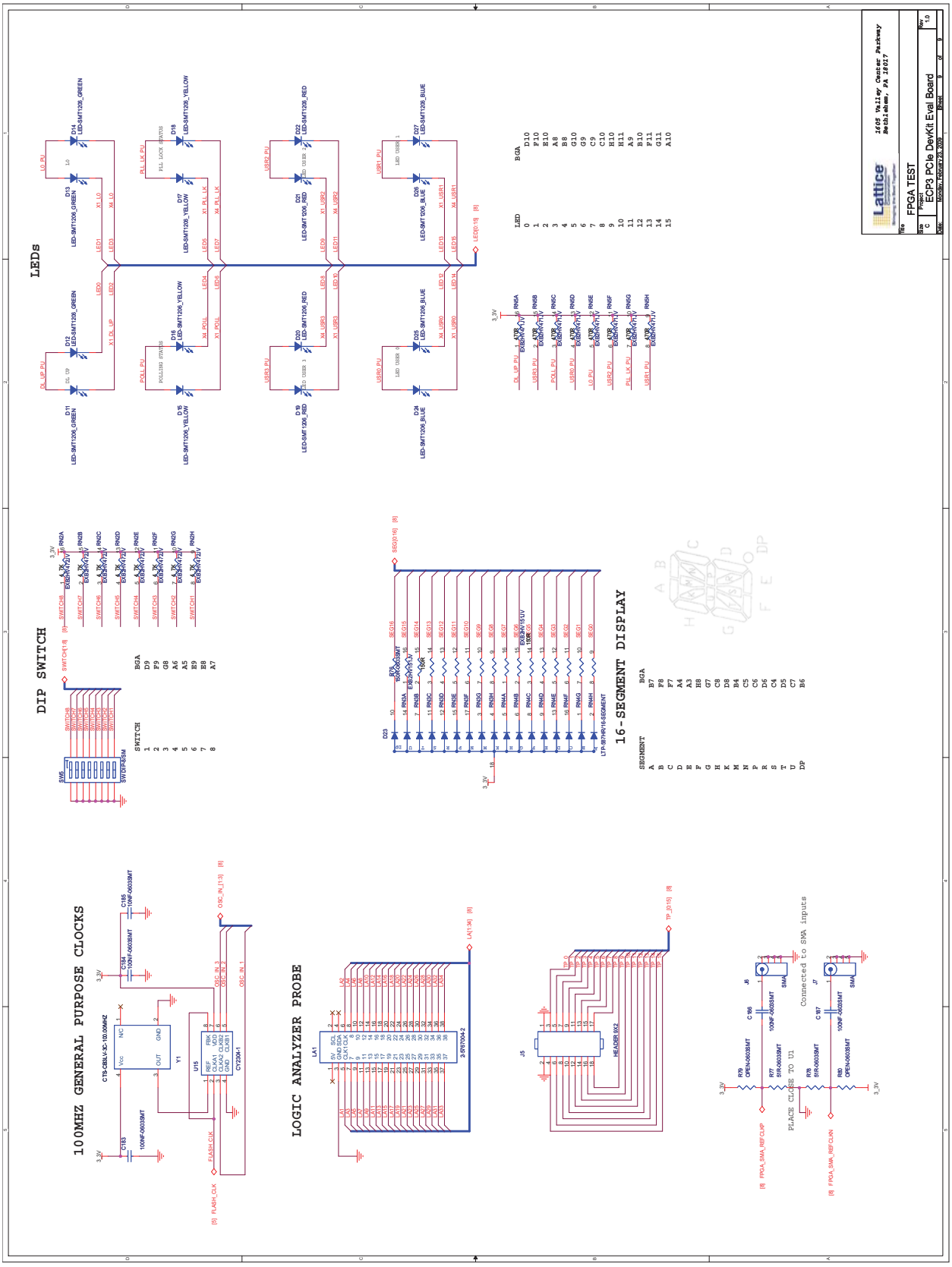
Figure 28. VSS/Decoupling



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Appendix B. Bill of Materials

Table 17. Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
1	1	CN1	PCI Express x4 Edge Finger Conn.			PCB Edge finger
2	1	CN2	PCI Express x1 Edge Finger Conn.			PCB Edge finger
3	1	C1	470UF-FKSMT	Panasonic	EEV-FK1V471Q	CAP 470UF 35V ELECT FK SMD
4	2	C2, C140	100UF-FKSMT	Panasonic	EEEFK1V101XP	CAP 100UF 35V ELECT FK SMD
5	5	C3, C4, C7, C9, C142	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP 10UF 16V TANT B-SIZE
6	4	C5, C6, C8, C10	330UF-FKSMT	Panasonic	EEEFK1C331P	CAP 330UF 16V ELECT FK SMD
7	30	C11, C12, C13, C14, C15, C16, C17, C18, C36, C37, C38, C39, C40, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C83, C84, C85, C86	1000PF-0402SMT	Panasonic	ECJ-0EB1E102K	CAP 1000PF 25V CERAMIC X7R 0402
8	54	C19, C20, C21, C22, C23, C24, C25, C41, C43, C47, C49, C50, C51, C52, C53, C54, C55, C70, C73, C76, C79, C80, C88, C94, C96, C98, C100, C111, C113, C115, C117, C119, C121, C123, C125, C146, C148, C149, C150, C155, C156, C161, C162, C163, C164, C169, C170, C172, C174, C176, C178, C180, C182, C185	10NF-0603SMT	Kemet	C0603C103K5RACTU	CAP .01UF 50V CERAMIC X7R 0603
9	14	C26, C34, C48, C71, C77, C103, C105, C107, C109, C137, C141, C144, C154, C167	1UF-16V-0805SMT	Panasonic	ECJ-2FB1C105K	CAP 1UF 16V CERAMIC 0805 X5R
10	12	C27, C29, C44, C69, C81, C102, C104, C106, C108, C152, C153, C166	22UF-16V_TANTBSMT	Kemet	T491B226M016AT	CAPACITOR TANT 22UF 16V 20% SMD
11	54	C28, C30, C31, C32, C33, C35, C42, C45, C46, C72, C74, C75, C78, C82, C87, C89, C90, C91, C92, C93, C95, C97, C99, C101, C110, C112, C114, C116, C118, C120, C122, C124, C136, C139, C143, C145, C147, C151, C157, C158, C159, C160, C165, C168, C171, C173, C175, C177, C179, C181, C183, C184, C186, C187	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
12	10	C126, C127, C128, C129, C130, C131, C132, C133, C134, C135	100NFX5R-0402SMT	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402
13	1	C138	47UF-10V-TANTBSMT	Kemet	T491B476M010AT	CAPACITOR TANT 47UF 10V 20% SMD
14	11	D1, D2, D3, D4, D5, D9, D10, D11, D12, D13, D14	LED-SMT1206_GREEN	Panasonic	LNJ316C83RA	LED GREEN (UP) W/LENS 1206
15	7	D6, D7, D8, D19, D20, D21, D22	LED-SMT1206_RED	Panasonic	LNJ211R82RA	LED RED (UP) W/LENS 1206
16	4	D15, D16, D17, D18	LED-SMT1206_YELLOW	Panasonic	LNJ411K84RA	LED YELLOW (UP) W/LENS 1206
17	1	D23	LTP-587HR/16-SEGMENT	Lite-On	LTP-587HR	16-segment array
18	4	D24, D25, D26, D27	LED-SMT1206_BLUE	Panasonic	LNJ916C8BRA	LED BLUE (UP) W/LENS 1206
19	8	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8	BLM41PG600SN1	Murata	BLM41PG600SN1L	FERRITE CHIP 60 OHM 6000MA 1806
20	5	F1, F2, F3, F4, F5	F1228CT-ND	Littlefuse	0154005.DR	FUSEBLOCK WITH 5A FUSE SMD
21	1	J1	22HP037-2.1mm	Condor	22HP037-2.1mm	power input
22	1	J2	HEADER 2X2	Samtec	TSW-102-07-T-D	2x2-0.25 Header
23	1	J3	HEADER 2	Samtec	TSW-102-07-T-S	2x1-0.25 Header
24	2	J4, J8	HEADER 6	Samtec	TSM-106-01-T-SH	6x1-0.25 Header-SMT
25	1	J5	HEADER 9X2	Samtec	TSW-109-07-T-D	9x2-0.25 Header

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Table 17. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
26	2	J6, J7	SMA	Molex	73391-0060	CONN JACK SMA STR 50 OHM PCB
27	1	LA1	2_5767004-2	Amp	2_5767004-2	CONN RECEPT 38POS .025 VERT SMD
28	5	LP1, LP2, LP3, LP4, LP5	5016	Keystone Electronics	5016	TEST POINT PC COMPACT SMT
29	3	MH1, MH2, MH3	M HOLE2			
30	2	PP1, PP2	PROBEPOINT			
31	4	Q1, Q2, Q3, Q4	2N2222/SOT23	Diodes Inc.	MMBT2222A-7-F	TRANS NPN 40V 350MW SMD SOT-23
32	1	RN1	EXBV8V472JV	Panasonic	EXBV8V472JV	RES ARRAY 4.7K OHM 5% 4 RES SMD
33	1	RN2	EXB2HV472JV	Panasonic	EXB2HV472JV	RES ARRAY 4.7K OHM 5% 8 RES SMD
34	2	RN3, RN4	EXB2HV151JV	Panasonic	EXB2HV151JV	RES ARRAY 150 OHM 5% 8 RES SMD
35	1	RN5	EXB2HV471JV	Panasonic	EXB2HV471JV	RES ARRAY 470 OHM 5% 8 RES SMD
36	2	RP1, RP2	CTS-R2402B7	CTS Corporation Resistor/ Electrocomponents	CTS-R2402B7TR7	RES NET DDR SDRAM 50 OHM 3X9 BGA
37	4	R1, R2, R3, R4	1_8K-1206SMT	Panasonic	ERJ-8GEYJ182V	RES 1.8K OHM 1/4W 5% 1206 SMD
38	1	R76	150R-0603SMT	Panasonic	ERA-3YEB151V	RES 150 OHM 1/16W .1% 0603 SMD
39	23	R6, R7, R8, R21, R22, R27, R28, R29, R30, R31, R32	10K-0603SMT	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD
		R33, R34, R35, R36, R37, R38, R39, R45, R46, R48, R49, R54				
40	7	R9, R10, R53, R64, R67, R73, R75	0R-0603SMT	Panasonic	ERJ-3GEY0R00V	RES ZERO OHM 1/10W 5% 0603 SMD
41	2	R11, R12	OPEN-0805SMT			
42	1	R13	12_1K-0603SMT	Susumu Co Ltd.	RG1608P-1212-B-T5	RES 12.1K OHM 1/10W .1% 0603 SMD
43	2	R14, R20	2K-0603SMT	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD
44	2	R15, R16	100R-0805SMT	Panasonic	ERJ-6GEYJ101V	RES 100 OHM 1/8W 5% 0805 SMD
45	8	R17, R19, R56, R57, R61, R66, R68, R74	1K-0603SMT	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/16W 1% 0603 SMD
46	1	R18	806R-0603SMT	Panasonic	ERJ-3EKF8060V	RES 806 OHM 1/10W 1% 0603 SMD
47	3	R23, R24, R25	680R-0603SMT	Panasonic	ERJ-3GEYJ681V	RES 680 OHM 1/10W 5% 0603 SMD
48	3	R5, R26, R47	220R-0603SMT	Panasonic	ERJ-3GEYJ221V	RES 220 OHM 1/10W 5% 0603 SMD
49	7	R40, R43, R44, R60, R69, R70, R71	4_7K-0603SMT	Panasonic	ERJ-3GEYJ472V	RES 4.7K OHM 1/10W 5% 0603 SMD
50	8	R41, R42, R52, R58, R59, R63, R79, R80	OPEN-0603SMT			
51	2	R50, R51	100R-0603SMT	Panasonic	ERA-3YEB101V	RES 100 OHM 1/16W .1% 0603 SMD

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Table 17. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
52	1	R55	2_2K-0603SMT	Panasonic	ERJ-3GEYJ222V	RES 2.2K OHM 1/10W 5% 0603 SMD
53	2	R62, R72	1K_ADJ/SMT3MM	Murata	PVG3A102C01R00	POT 1K 3MM CERM SQ S/T SMD
54	0	R65(deleted)	0R-2010SMT	Vishay/Dale	CRCW20100000Z0EF	RES 0.0 OHM1/2W 5% 2010 SMD
55	2	R77, R78	51R-0603SMT	Panasonic	ERJ-3GEYJ510V	RES 51 OHM 1/10W 5% 0603 SMD
56	4	SP1, SP2, SP3, SP4	TEST POINT			
57	4	SW1, SW3, SW6, SW7	SW PUSHBUTTON-SPST	C&K Components	EP11FPD1SAPE	SPST- Momentary RA/SMT
58	1	SW2	SW DIP-3 CTS 194-3MST	CTS Corporation Resistor/Electrocomponents	194-3MST	SWITCH SIDE ACTUATED GOLD 3 SEC
59	1	SW4	B3F-1150	Omron	B3F-1150	SWITCH TACT 6MM 100GF H=7.3MM
60	1	SW5	SW DIP-8/SM	C&K Components	BPA08SB	8-POSITION DIP PACK
61	1	TB1	Terminal Block/ED1202DS	On-Shore Tech.	ED120/2DS	TERMINAL BLOCK 5.08MM VERT 2POS
62	14	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	TESTPOINT			
		TP11, TP12, TP13, TP14				
63	1	U1	ECP3-672fpBGA	LATTICE SUPPLIED		
64	1	U2	PTH12060L	Texas Instruments	PTH12060LAH	MODULE PIP 12VIN 10A ADJ 10-TH
65	1	U3	PTH12060W	Texas Instruments	PTH12060WAH	MODULE PIP 12VIN 10A ADJ 10-TH
66	2	U4, U5	SC1592	Semtech	SC1592IMTRT	IC LDO ADJ REG 3A TO-263-7
67	1	U6	M25P64-FLASH	STMicro	M25P64-VMF6P	IC SRL FLASH 64MBIT 3V 16-SOP Wide(300MIL)
68	1	U7	MAX6817	Maxim	MAX6817-EUT+T	±15kV ESD-Protected, Dual, CMOS Switch Debouncers
69	2	U8,U10	NC7WZ16-MAAO6A/Fairchild TinyLogic	Fairchild	NC7WZ16P6X	IC BUFFER UHS DUAL SC70-6
70	1	U9	SN74LVC125A/SO14	Texas Instruments	SN74LVC125AD	IC QUAD BUS BUFFER GATE 14-SOIC
71	1	U11	S29GL064A	Spansion	S29GL064N90BF1040	48fBGA FLASH-VBN048
72	1	U12	LCMXO1200C-CSBGA132	LATTICE SUPPLIED		
73	1	U13	LP2998-SO8	National Semi	LP2998MA/NOPB	IC DDR TERMINATION REG 8SOIC
74	1	U14	DDR2-SDRAM-84FBGA	Micron	MT47H16M16BG-37E	16-Bit DDR2
75	1	U15	CY2304-1	Cypress Semiconductor	CY2304SXC-1	zero delay buffer
76	1	Y1	CTS-CB3LV-3C-100.00MHZ	CTS-Frequency Controls	CB3LV-3I-100M0000-T	OSC CLOCK 100.000 MHZ 3.3V SMD
77	1	Bracket				
78	2	Screw	4-40 x .250			
79	2	Flat washer	4-40			
80	2	Lock washer	4-40			
81	2	C222, C224	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603

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Table 17. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
82	1	C223	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP 10UF 16V TANT B-SIZE
83	1	R227	1_6R-0603SMT	Panasonic	ERJ-3GEYJ1R6V	RESISTOR 1.6 OHM 1/10W 5% 0603
84	4	R223, R224, R228, R229	50R-0402SMT	Vishay	FC0402E50R0BTBST1	RES 50 OHM 50MW .1% 0402 SMD
85	1	Y2	CRYSTEK_133MHZ	Crystek	CCLD-033-50-133.000	OSC LVDS 133.0 MHZ 3.3V 7mmx5mm SMD
86	2	C220, C225	10NF-0402SMT	Panasonic	ECJ0EB1E103K	CAP .01UF 25V CERAMIC X7R 0402
87	1	R222	50R-0603SMT	Vishay	FC0603E50R0BTBT1	RES 50 OHM 125MW .1% 0603 SMD
88	1	D33	SCHOTTKY/VISHAYV12P10	Vishay	V12P10-E3/87A	TO277 SCHOTTKY DIODE

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