XC-1 Hardware Manual

Version 1.3.2

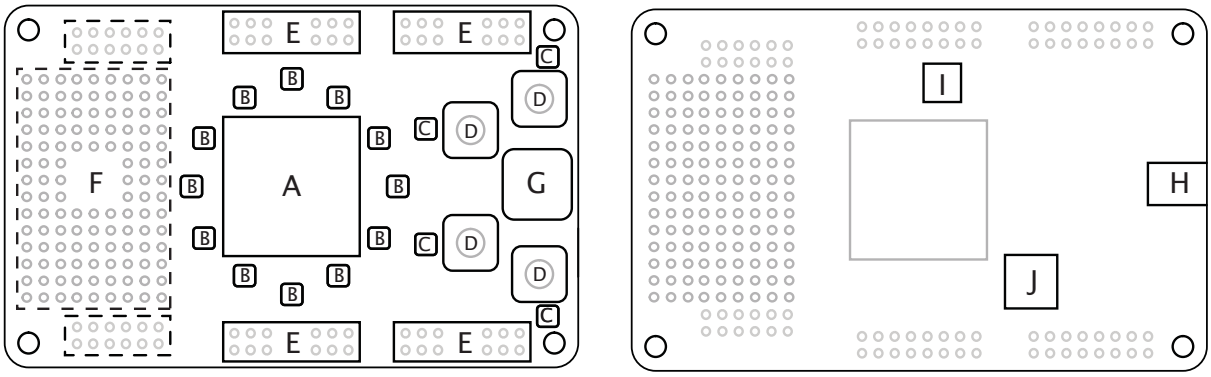
XMOS

Publication Date: 2009/11/12

1 Introduction

The XC-1 is an Event-Driven Processor development board based on the XMOS XS1-G4. It comprises a single XS1-G4, 16 user-configurable LEDs, four push-buttons, a speaker, JTAG and serial interfaces, and a through-hole prototyping area for connecting external components. The XC-1 is powered directly from a host PC using a mini-USB cable.

The diagram below shows the layout of the main components on the card:



A XS1-G4 Device

B Twelve Red/Green User LEDs

C Four Green User LEDs

D Four Push-Button Switches

E Four I/O Expansion Areas

F Prototyping Area

G Speaker

H Mini USB-B Connector

I 20MHz Crystal Oscillator

J USB 2.0 to JTAG

The XC-1 Development Kit also includes a USB cable for powering and booting the device from a PC. The card is fitted with four plastic feet, which are useful for building bigger prototyping systems.

The following sections in this document provide a detailed description of these components.

2 XS1-G4 Device [A]

The XC-1 provides a single four core XS1-G4 device in a 512BGA package. Each XCore is programmable and comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins on XCore0 and XCore2 are brought out of the package and connected to the card's components as follows:

Processor 0

- Twelve red/green and four green LEDs
- Four push-button switches
- Speaker

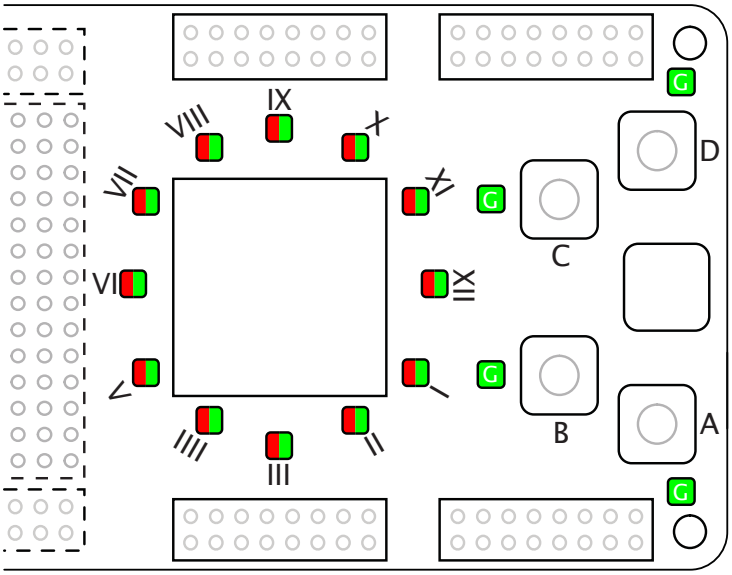
Processor 2

- Three 16-way I/O expansion headers (24 I/O bits)
- One 16-way I/O expansion headers (16 I/O bits)

The processors have ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports with the XC-1 components is provided in a separate tutorial [1].

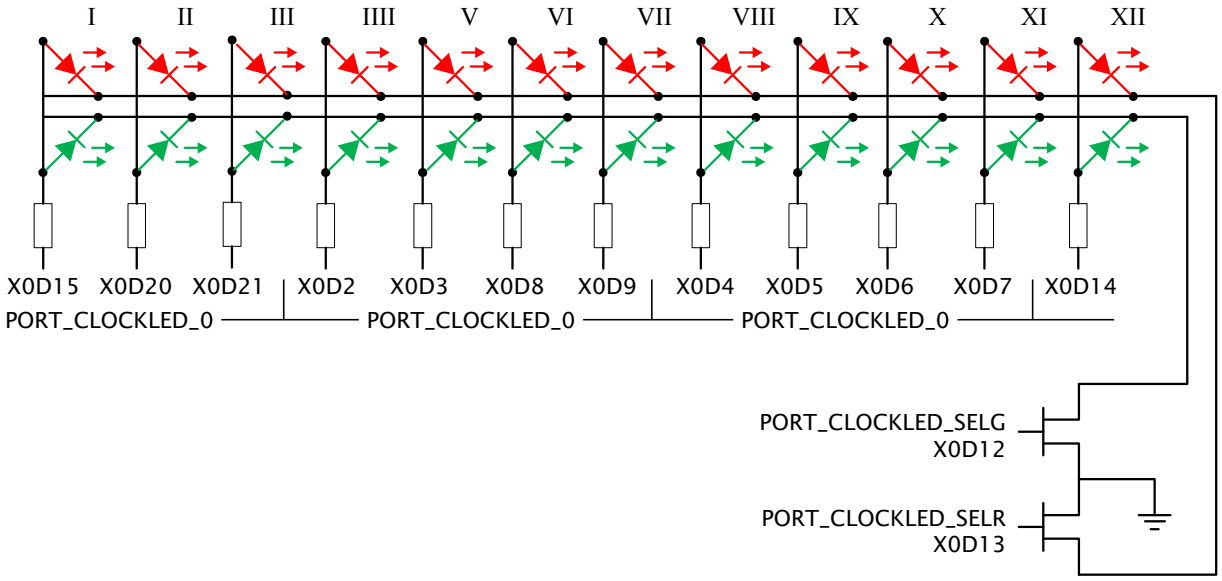
3 User-configurable LEDs [B and C]

The XC-1 has 16 user-configurable LEDs. Four of green LEDs are positioned next to the four push-buttons (collectively referred to as button-LEDs) and contain green diodes. The other 12 LEDs are positioned around the XS1-G4 in a circle (collectively referred to as clock-LEDs) and contain red/green diodes. A Roman numeral is printed next to each LED. Each of the LEDs can be driven by software. The layout of the LEDs is shown on the following page.



To reduce the number of pins required for the 12 clock-LEDs, the LED anodes are connected to three 4-bit ports (4A, 4B and 4C) on processor 0 and the cathodes are connected to two 1-bit ports (1E for green, 1F for red) that are active high.

The schematic for the clock-LEDs is shown below



PORT_CLOCKLED_SELR	PORT_CLOCKLED_SELG	Colour
0	0	Off
0	1	Green
1	0	Red
1	1	Red
To get yellow, alternate green/red in 4:1 ratio		

The clock LED pins are mapped to ports as described in the table below:

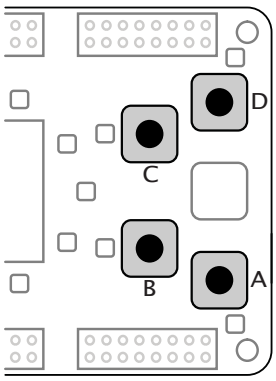
Pin	Port		Processor
	1b	4b	0
X0D2		P4A0	PORT_CLOCKLED_0 [IIII]
X0D3		P4A1	PORT_CLOCKLED_0 [V]
X0D4		P4B0	PORT_CLOCKLED_1 [VIII]
X0D5		P4B1	PORT_CLOCKLED_1 [IX]
X0D6		P4B2	PORT_CLOCKLED_1 [X]
X0D7		P4B3	PORT_CLOCKLED_1 [XI]
X0D8		P4A2	PORT_CLOCKLED_0 [VI]
X0D9		P4A3	PORT_CLOCKLED_0 [VII]
X0D12	P1E0		PORT_CLOCKLED_SELG
X0D13	P1F0		PORT_CLOCKLED_SELR
X0D14		P4C0	PORT_CLOCKLED_2 [XII]
X0D15		P4C1	PORT_CLOCKLED_2 [I]
X0D20		P4C2	PORT_CLOCKLED_2 [II]
X0D21		P4C3	PORT_CLOCKLED_2 [III]

The button LED pins are mapped to ports as described in the table below:

Pin	Port	Processor
	8b	0
X0D40	P8D4	PORT_BUTTON_LED [A]
X0D41	P8D5	PORT_BUTTON_LED [B]
X0D42	P8D6	PORT_BUTTON_LED [C]
X0D43	P8D7	PORT_BUTTON_LED [D]

4 Push-Button Switches [D]

The XC-1 provides four push-button switches whose states can be sampled at any time by software. Pushing a button results in a 0 signal, unpushed the signal is 1. The layout of the push-buttons is shown below.



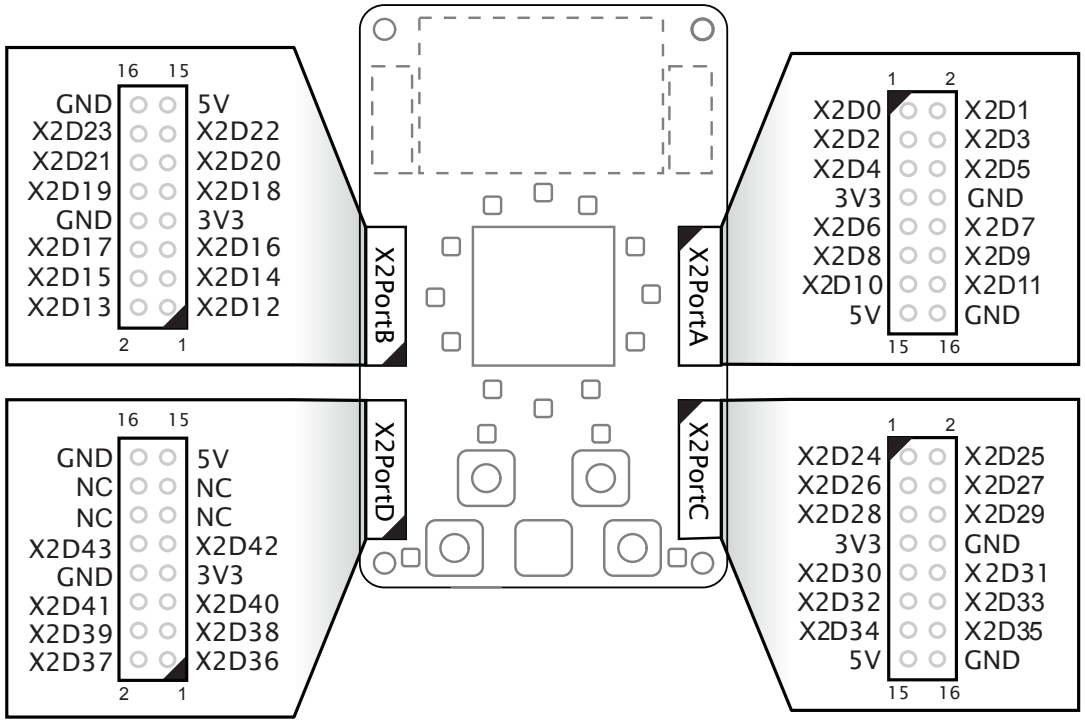
The push buttons are connected to four pins, which are mapped to ports as described in the table below.

Pin	Port		Processor
	4b	8b	0
X0D16	P4D0	P8B2	PORT_BUTTON [A]
X0D17	P4D1	P8B3	PORT_BUTTON [B]
X0D18	P4D2	P8B4	PORT_BUTTON [C]
X0D19	P4D3	P8B5	PORT_BUTTON [D]

Each pin can be configured either as a 4-bit port or an 8-bit port. The configuration is determined by the set of port initialisers used in the software [2].

5 I/O Expansion Areas [E]

The I/O pins of processor 2 are brought out to expansion areas on both sides of the card. These areas have 0.1" pitch plated through holes and are suitable for use with IDC headers. To provide maximum flexibility, no headers are fitted, allowing the most suitable type to be selected depending on the design. The routing of the I/O and power pins in the expansion headers is shown below.



Three of the expansion headers provide a bank of 12 I/O pins, while the fourth provides a bank of eight I/O pins. The pins are mapped to the ports as described in the table on the next page.

Pin	Port				Processor
	1b	4b	8b	16b	2
X2D0	P1A0				X2PortA
X2D1	P1B0				
X2D2		P4A0	P8A0	P16A0	
X2D3		P4A1	P8A1	P16A1	
X2D4		P4B0	P8A2	P16A2	
X2D5		P4B1	P8A3	P16A3	
X2D6		P4B2	P8A4	P16A4	
X2D7		P4B3	P8A5	P16A5	
X2D8		P4A2	P8A6	P16A6	
X2D9		P4A3	P8A7	P16A7	
X2D10	P1C0				
X2D11	P1D0				
X2D12	P1E0				X2PortB
X2D13	P1F0				
X2D14		P4C0	P8B0	P16A8	
X2D15		P4C1	P8B1	P16A9	
X2D16		P4D0	P8B2	P16A10	
X2D17		P4D1	P8B3	P16A11	
X2D18		P4D2	P8B4	P16A12	
X2D19		P4D3	P8B5	P16A13	
X2D20		P4C2	P8B6	P16A14	
X2D21		P4C3	P8B7	P16A15	
X2D22	P1G0				
X2D23	P1H0				
X2D24	P1E0				X2PortC
X2D25	P1F0				
X2D26		P4E0	P8C0	P16B0	
X2D27		P4E1	P8C1	P16B1	
X2D28		P4F0	P8C2	P16B2	
X2D29		P4F1	P8C3	P16B3	
X2D30		P4F2	P8C4	P16B4	
X2D31		P4F3	P8C5	P16B5	
X2D32		P4E2	P8C6	P16B6	
X2D33		P4E3	P8C7	P16B7	
X2D34	P1K0				
X2D35	P1L0				
X2D36	P1M0		P8D0	P16B8	X2PortD
X2D37	P1N0		P8D1	P16B9	
X2D38	P1O0		P8D2	P16B10	
X2D39	P1P0		P8D3	P16B11	
X2D40			P8D4	P16B12	
X2D41			P8D5	P16B13	
X2D42			P8D6	P16B14	
X2D43			P8D7	P16B15	

Eight pins from each bank can be configured as either two 4-bit ports or a single 8-bit port. Two of the expansion headers can alternatively be used together as a single 16-bit port.

5.1 XMOS Link Configuration

Some of the I/O pins on the expansion header can be configured as XMOS Links. The mapping of XMOS Links to the headers is shown in the table below.

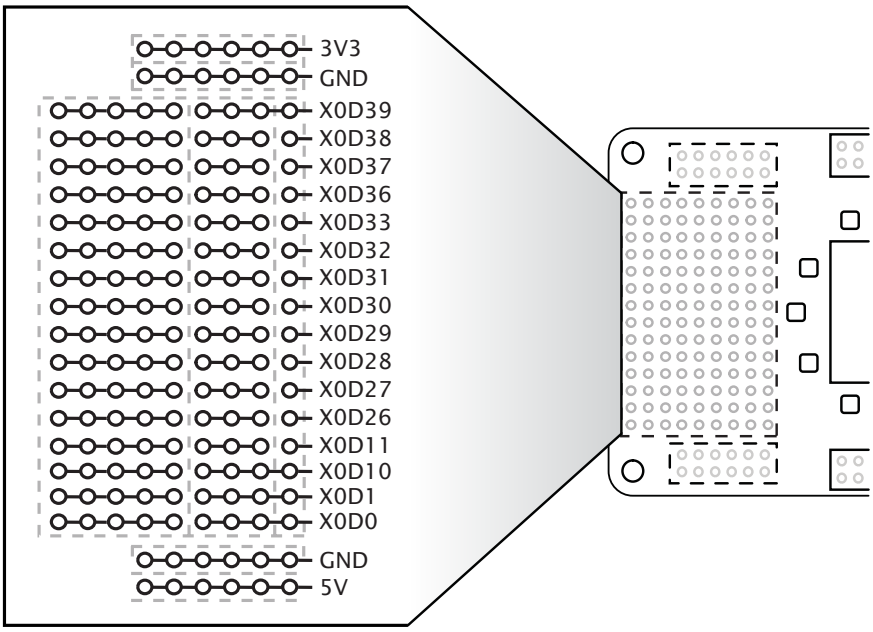
Header 2/A		
Pin	XMOS Link 2	
	2 bit	5 bit
X2D0		
X2D1		XLA4 O
X2D2		XLA3 O
X2D3		XLA2 O
X2D4	XLA1 O	XLA1 O
X2D5	XLA0 O	XLA0 O
X2D6	XLA0 I	XLA0 I
X2D7	XLA1 I	XLA1 I
X2D8		XLA2 I
X2D9		XLA3 I
X2D10		XLA4 I
X2D11		

Header 2/B		
Pin	XMOS Link 2	
	2 bit	5 bit
X2D12		
X2D13		XLB4 O
X2D14		XLB3 O
X2D15		XLB2 O
X2D16	XLB1 O	XLB1 O
X2D17	XLB0 O	XLB0 O
X2D18	XLB0 I	XLB0 I
X2D19	XLB1 I	XLB1 I
X2D20		XLB2 I
X2D21		XLB3 I
X2D22		XLB4 I
X2D23		

6 Prototyping Area [F]

The XC-1 provides a 0.1” pitch plated through hole area for adding components to the card.

The routing of I/O and power pins in the prototyping area is shown below.



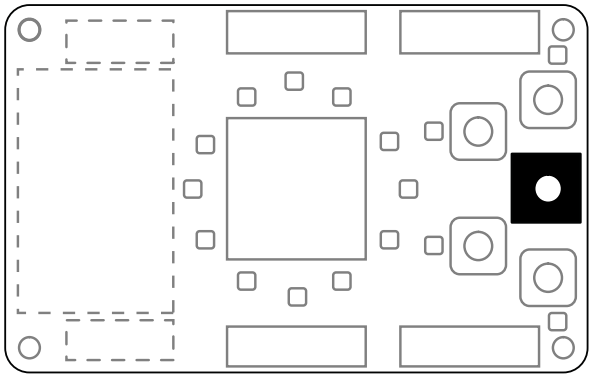
The prototyping area provides a bank of 16 I/O pins, which are mapped to the ports on processor 0 as described in the table on the following page.

Pin	Port			Processor
	1b	4b	8b	0
X0D0	P1A0			Prototyping Area
X0D1	P1B0			
X0D10	P1C0			
X0D11	P1D0			
X0D26		P4E0	P8C0	
X0D27		P4E1	P8C1	
X0D28		P4F0	P8C2	
X0D29		P4F1	P8C3	
X0D30		P4F2	P8C4	
X0D31		P4F3	P8C5	
X0D32		P4E2	P8C6	
X0D33		P4E3	P8C7	
X0D36	P1M0			
X0D37	P1N0			
X0D38	P1O0			
X0D39	P1P0			

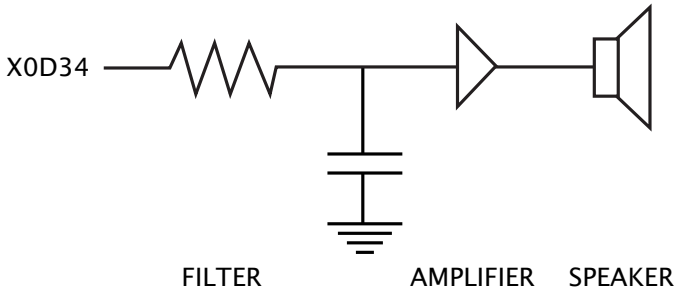
The prototyping area provides access to eight 1-bit ports (1A, 1B, 1C, 1D, 1M, 1N, 1O and 1P) and either two 4-bit ports (4E and 4F) or one 8-bit port (8C).

7 Speaker [G]

The XC-1 has a speaker. The layout of the speaker is shown below.



Audio signals are generated by filtering pulse width modulated (PWM) digital signals to form an analogue waveform, which is amplified and sent to the speaker, as shown below



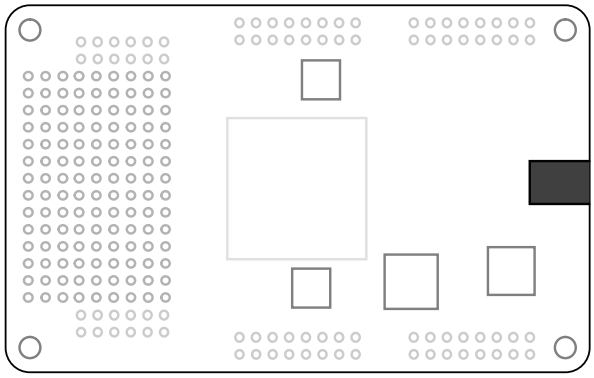
The speaker pin is mapped to a port on processor 0, as shown in the table below.

Pin	Port	Processor
	1b	0
X0D34	P1K0	PORT_SPEAKER

8 USB Connector [H and J]

The XC-1 is powered directly from a host PC using a USB connector. The 5V voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

The USB connector can also be used to load and debug code on all of the XS1-G4's processors. The USB connector provides JTAG control, system reset, processor debug, and two UART links. The layout of the USB connector is shown below.



On power on, the XS1-G4 boots from the on-board flash memory. The XS1-G4 can then be put into JTAG mode by the PC, which then boots another program.

No UART hardware is provided. Instead, two UART pins are mapped to ports, as shown in the table below.

Pin	Port	Processor
	1b	0
X0D23	P1H0	PORT_UART_TX
X1D24	P1I0	PORT_UART_RX

If a UART is required, it can be implemented in software by sampling and driving these ports at the required rate. The connector performs a UART-to-USB conversion on these pins, presenting a virtual COM port to the PC that can be interfaced via a terminal emulator.

9 20MHz Crystal Oscillator [I]

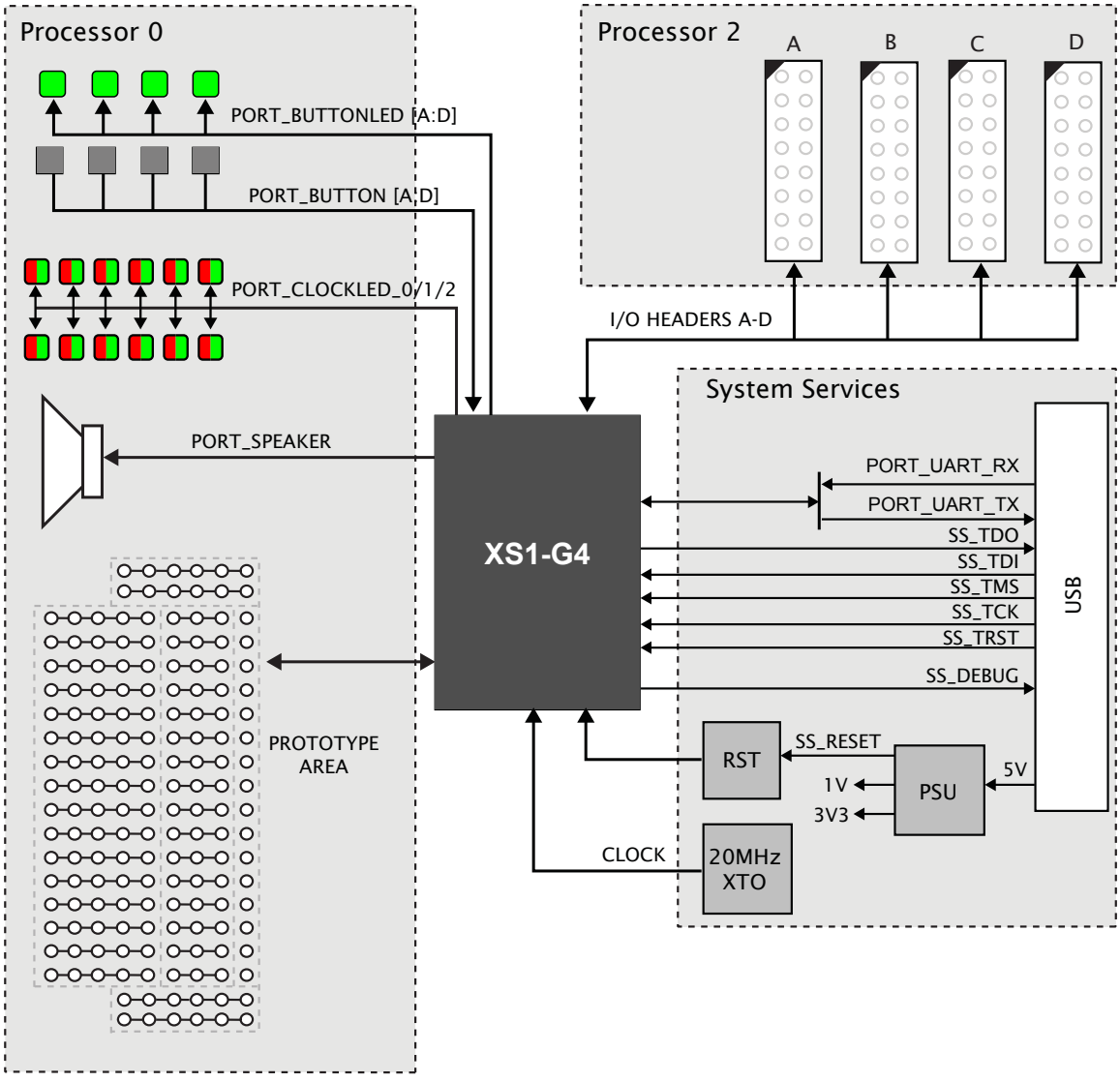
The XS1-G4 is clocked at 20MHz by a crystal oscillator on the card. Each processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

10 Dimensions

The XC-1 dimensions are 86 x 54mm. The mounting holes are 3mm in diameter.

11 XC-1 Block Diagram

The diagram below shows how the XC-1 components are connected to the XS1-G4.



11.1 I/O Port-to-Pin Mapping

The table below provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port				Processor	
	1b	4b	8b	16b	0	2
X*n*D0	P1A0				PROTOTYPE_AREA_0	X2PortA Header
X*n*D1	P1B0				PROTOTYPE_AREA_1	
X*n*D2		P4A0	P8A0	P16A0	PORT_CLOCKLED_0 [IIII]	
X*n*D3		P4A1	P8A1	P16A1	PORT_CLOCKLED_0 [V]	
X*n*D4		P4B0	P8A2	P16A2	PORT_CLOCKLED_1 [VIII]	
X*n*D5		P4B1	P8A3	P16A3	PORT_CLOCKLED_1 [IX]	
X*n*D6		P4B2	P8A4	P16A4	PORT_CLOCKLED_1 [X]	
X*n*D7		P4B3	P8A5	P16A5	PORT_CLOCKLED_1 [XI]	
X*n*D8		P4A2	P8A6	P16A6	PORT_CLOCKLED_0 [VI]	
X*n*D9		P4A3	P8A7	P16A7	PORT_CLOCKLED_0 [VII]	
X*n*D10	P1C0				PROTOTYPE_AREA_2	
X*n*D11	P1D0				PROTOTYPE_AREA_3	
X*n*D12	P1E0				PORT_CLOCKLED_SELG	X2PortB Header
X*n*D13	P1F0				PORT_CLOCKLED_SELR	
X*n*D14		P4C0	P8B0	P16A8	PORT_CLOCKLED_2 [XII]	
X*n*D15		P4C1	P8B1	P16A9	PORT_CLOCKLED_2 [I]	
X*n*D16		P4D0	P8B2	P16A10	PORT_BUTTON [A]	
X*n*D17		P4D1	P8B3	P16A11	PORT_BUTTON [B]	
X*n*D18		P4D2	P8B4	P16A12	PORT_BUTTON [C]	
X*n*D19		P4D3	P8B5	P16A13	PORT_BUTTON [D]	
X*n*D20		P4C2	P8B6	P16A14	PORT_CLOCKLED_2 [II]	
X*n*D21		P4C3	P8B7	P16A15	PORT_CLOCKLED_2 [III]	
X*n*D22	P1G0				RESERVED	
X*n*D23	P1H0				PORT_UART_TX	
X*n*D24	P1I0				PORT_UART_RX	X2PortC Header
X*n*D25	P1J0				RESERVED	
X*n*D26		P4E0	P8C0	P16B0	PROTOTYPE_AREA_4	
X*n*D27		P4E1	P8C1	P16B1	PROTOTYPE_AREA_5	
X*n*D28		P4F0	P8C2	P16B2	PROTOTYPE_AREA_6	
X*n*D29		P4F1	P8C3	P16B3	PROTOTYPE_AREA_7	
X*n*D30		P4F2	P8C4	P16B4	PROTOTYPE_AREA_8	
X*n*D31		P4F3	P8C5	P16B5	PROTOTYPE_AREA_9	
X*n*D32		P4E2	P8C6	P16B6	PROTOTYPE_AREA_10	
X*n*D33		P4E3	P8C7	P16B7	PROTOTYPE_AREA_11	
X*n*D34	P1K0				PORT_SPEAKER	
X*n*D35	P1L0				RESERVED	
X*n*D36	P1M0		P8D0	P16B8	PROTOTYPE_AREA_12	X2PortD Header
X*n*D37	P1N0		P8D1	P16B9	PROTOTYPE_AREA_13	
X*n*D38	P1O0		P8D2	P16B10	PROTOTYPE_AREA_14	
X*n*D39	P1P0		P8D3	P16B11	PROTOTYPE_AREA_15	
X*n*D40			P8D4	P16B12	PORT_BUTTONLED [A]	
X*n*D41			P8D5	P16B13	PORT_BUTTONLED [B]	
X*n*D42			P8D6	P16B14	PORT_BUTTONLED [C]	
X*n*D43			P8D7	P16B15	PORT_BUTTONLED [D]	

12 XC-1 XN File

The XCore ports linked to the hardware features on the XC-1 are mapped to generic port identifiers as part of a platform specific XN file, which simplifies the process of porting a project between platforms.

The following table lists the defined identifiers for processors 0 and 2:

Processor	Port Location	Generic Identifier
0	XS1_PORT_4A	PORT_CLOCKLED_0
	XS1_PORT_4B	PORT_CLOCKLED_1
	XS1_PORT_4C	PORT_CLOCKLED_2
	XS1_PORT_1E	PORT_CLOCKLED_SELG
	XS1_PORT_1F	PORT_CLOCKLED_SELR
	XS1_PORT_4D	PORT_BUTTON
	XS1_PORT_1H	PORT_UART_TX
	XS1_PORT_1I	PORT_UART_RX
	XS1_PORT_1K	PORT_SPEAKER
	XS1_PORT_8D	PORT_BUTTONLED
2		

13 Related Documents

The following documents provide more information on designing with the XC-1:

- *XCard-1 Tutorial* [1]: provides an introduction to programming software on the XC-1 using the XC language.
- *The XMOS XS1 Architecture* [3]: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XC-1, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xc1/`

Bibliography

[1] Douglas Watt and Ross Owen. XC-1 Development Card Tutorial. Website, 2009. http://www.xmos.com/published/xc1tut.

[2] Douglas Watt. *Programming XC on XMOS Devices*. XMOS Limited, Sep 2009. http://www.xmos.com/published/xc_en.

[3] David May. *The XMOS XS1 Architecture*. XMOS Limited, 2009. http://www.xmos.com/published/xs1_en.

Disclaimer