

TC1793

AP32163

Design Guideline for TC1793 Microcontroller Board Layout

Application Note

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Microcontrollers

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Device1

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1 Overview

The TC1793 is a 32-Bit microcontroller in a BGA-416 package, which requires a PCB carefully designed for electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for the TC1793 are discussed here.

1.1 General Information

The microcontroller has four supply domains ((VDD=1.3V for Core, VDDP=3.3V for I/O Pad, VDDEBU=2.5V-3.3V for EBU, VDDM=3.3V or 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1793

AF	N.C.	P15.15 BFCLK0	P15.14 BFCLK1	P15.13 #BKA	P15.10 #ADV	P15.9 #BWR	P15.8 #RD	P15.12 #RW	P15.6 BC2	P15.0 HOLD	VDDP	P10.1 MSTR0	P10.3 SCLK0	P4.14 GPTA	P4.10 GPTA	P4.9 GPTA	P4.6 GPTA	VSSM	VFAREF	AND1 FAN0	AND2 FAN2	VAGND0	AN43	AN39	AN37	N.C.
AE	P14.10 GPTA D05	P14.13 GPTA D06	P14.14 GPTA D07	N.C.	P15.0 N.C.	P15.11 #WAIT	P15.3 CS0	P15.7 BC3	P15.4 BC0	VDDP	P10.2 MSTR0	P10.4 SCLK0	P4.13 GPTA	P4.7 GPTA	P4.3 GPTA	P4.1 GPTA	VDDM	VFAHND	AND3 FAN3	AND4 FAN4	VAREF0	AN41	AN36	AN33	AN6	
AD	P14.8 GPTA D04	P14.11 GPTA D05	P14.15 GPTA D09	N.C.	P16.2 BREQ	P15.1 CS1	P15.2 CS2	P15.1 HDA	P15.5 BC1	VDDP	P10.2 SLS0F	P4.15 GPTA	P4.11 GPTA	P4.5 GPTA	P4.2 GPTA	P4.0 GPTA	VAREF2	AND5 FAN5	AND7 FAN7	VAREF1	AND6 FAN6	VAGND1	AN42	AN38	AN32	AN4
AC	P14.7 GPTA D03	P14.9 GPTA D05	P14.12 GPTA D08	VSSP	VDDP	N.C.	VD	VSSM	VDDP	VDDP	P10.5 SLS01	P4.12 GPTA	P4.8 GPTA	P4.4 GPTA	P4.0 GPTA	VCC	VSSP	VDDP	AND4 FAN4	AND5 FAN5	VAGND1	AN42	AN38	AN32	AN4	AN8
AB	P13.15 GPTA D15	P14.4 GPTA D02	P14.5 GPTA D01	VDD																						
AA	P13.11 GPTA D11	P14.1 GPTA D01	P14.2 GPTA D02	P14.3 GPTA D03																						
Y	P13.10 GPTA D10	P13.14 GPTA D14	P14.2 GPTA D02	VDDP																						
W	P13.7 GPTA D7	P13.12 GPTA D12	P14.0 GPTA D0	VSSM																						
V	P13.4 GPTA D4	P13.8 GPTA D8	P13.13 GPTA D13	VDD																						
U	P13.2 GPTA D2	P13.5 GPTA D5	P13.9 GPTA D9	P13.6 GPTA D6							VSS	VSS	VSSP	VSSP	VSS	VSS	VSS	VSS								
T	P13.0 GPTA D0	P13.3 GPTA D3	P13.1 GPTA D1	VDDP							VSS	VSS	VSSP	VSSP	VSS	VSS	VSS	VSS								
R	P12.4 A20	P12.5 A21	P12.3 A19	VSSC							VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
P	P12.0 A16	P12.2 A18	P12.1 A17	VDD							VSSP	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
M	P11.12 A12	P11.15 A15	P11.1 A14	P11.13 A13							VSSP	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
N	P11.8 A8	P11.9 A9	P11.10 A10	VDDP							VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
L	P11.6 A6	P11.5 A5	P11.11 A11	VSSC							VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
K	P11.2 A2	P11.1 A1	P11.4 A4	P11.7 A7							VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
J	P11.0 A0	P12.7 A23	P12.8 A22	P11.3 A3							VSSP	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
H	VDDP	VDDP	VDDP	VDDP																						
G	XTAL1 (IN)	XTAL2 (OUT)	VDDP	VDDP																						
F	VDDOSC	VSSOSC	TMS DAP1	TRST																						
E	VDDOSC1	ID1 BRN1	TDK DAP0	VDD																						
D	P9.14 EROUT	TD0 DAP2	VDD	VSSP	VDDP	P9.12 GRO	P9.7 GPTA MSC0	P9.2 GPTA MSC1	P9.4 GPTA SON0	P9.8 GPTA SON0	VDD	VSSP	VDDP	P3.11 GPTA	P3.13 GPTA	P3.12 GPTA	P3.8 GPTA	VDD	VSSP	VDDP	P0.11 ERAY	P0.13 ERAY	P0.15 SSC1	P2.2 SSC	P2.4 SSC	
C	P9.13 BRIN	VDD	VSSP	VDDP	N.C.	P9.11 GRO	P9.6 MSC0	P9.5 MSC0	P5.11 GPTA FCLD0	P5.10 GPTA FCLD0	P9.9 GPTA SON0A	P4.4 HRC0 MURGPTA	P5.5 GPTA MSC0	P3.2 GPTA	P3.4 GPTA	P3.9 GPTA	P3.10 GPTA	P3.7 GPTA	P0.9 ERAY	P0.10 ERAY	P0.12 ERAY	P0.14 ERAY	P2.11 SSC1	P2.11 GPTA	P2.8 GPTA	
B	VDD	VSSP	VDDP	TDMD	POEST	P9.10 EMOSTOP	P9.2 GPTA MSC1	P9.1 GPTA MSC1	VDDP	P5.14 GPTA FOLN0	P5.13 GPTA FOLN0	P4.8 MSC1 MURGPTA	P5.3 GPTA ASC1	P3.0 GPTA	P3.0 GPTA	P3.3 GPTA	P3.6 GPTA	P3.15 GPTA	P0.3 ERAY	P0.4 ERAY	P0.5 ERAY	P0.6 ERAY	P2.12 GPTA	P2.10 GPTA	P2.7 GPTA	
A	VSSP	VDDP	N.C.	ESR0	ESR1	P9.9 GRO	P9.3 GPTA MSC1	P9.0 GPTA MSC1	VDDP	P5.15 GPTA FOLP1A	P5.12 GPTA SON1	P5.7 GPTA MSC1	P5.2 GPTA ASC1	P3.1 GPTA	P3.5 GPTA	P3.14 GPTA	P3.0 HRC0F0	P0.1 ERAY	P0.2 ERAY	P0.4 ERAY	P0.5 ERAY	P0.8 ERAY	P2.15 GPTA	P2.13 GPTA	P2.9 GPTA	
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Figure 1 Pinout of TC1793 (BGA-416):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
 - BFCLKOUT: EBU clock output
 - LVDS Pins
 - MLI Pins
 - MSC Pins

- ERAY Pins
- Supply Pins

Route these signals with adjacent ground reference and avoid signal and reference layer changes.

Route them as short as possible.

Routing ground on each side can help to reduce coupling to other signals.

- For unused **“Output, Supply, Input and I/O “** pins following points must be considered:

1. Supply Pins (Modules)	<ul style="list-style-type: none"> • See the User’s Manual.
2. I/O-Pins	<ul style="list-style-type: none"> • Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	<ul style="list-style-type: none"> • Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4. Input Pins without internal pull device	<ul style="list-style-type: none"> • For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	<ul style="list-style-type: none"> • For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User’s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

- Separate analog and digital grounds.

- The analog ground must be separated into two groups:

1. Ground for OSC and PLL (VSSOSC for VDDOSC, VDDOSC3, VDDPF and VDDPF3) as common star point.

2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for the load capacitors and Xtal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (see Figure 2).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF (see Figure 2). Using inductance or ferrite beads (5 – 10 μH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to $\sim 10\text{dB}\mu\text{V}$ on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

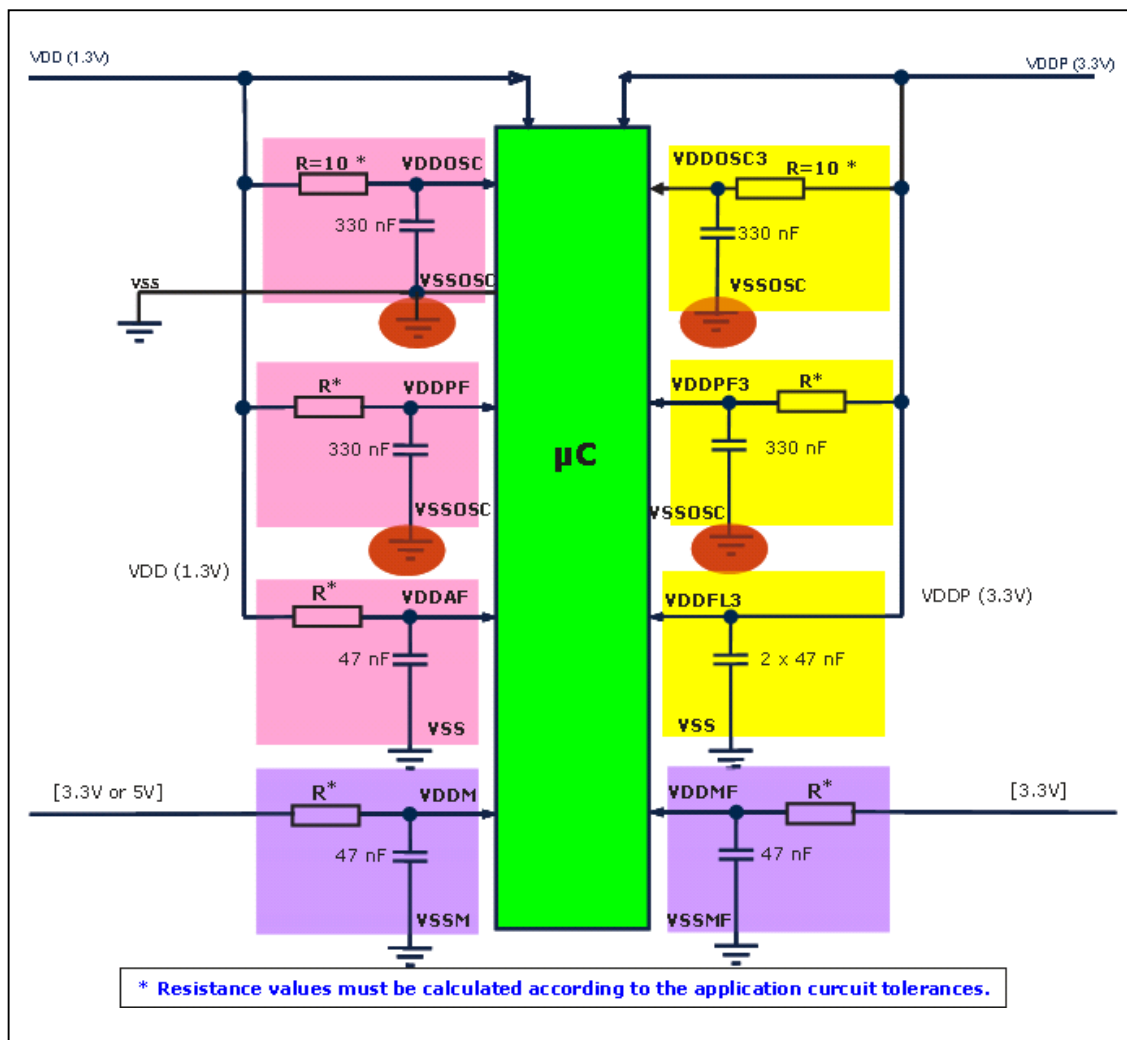


Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF supply pins

2.1 Decoupling

- The three supply domains VDD, VDDP and VDDEBU of TC1793 should be decoupled separately (see decoupling placement example in Figure 3).
- Type of capacitors:
 - Values: 47 nF, 100 nF, 330 nF
 - X7R Ceramic Multilayer (low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and POWER/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

In Figure 3 shown examples are based on device power supply concept and implementation. Alternative implementations are also acceptable and must be evaluated within application by customer.

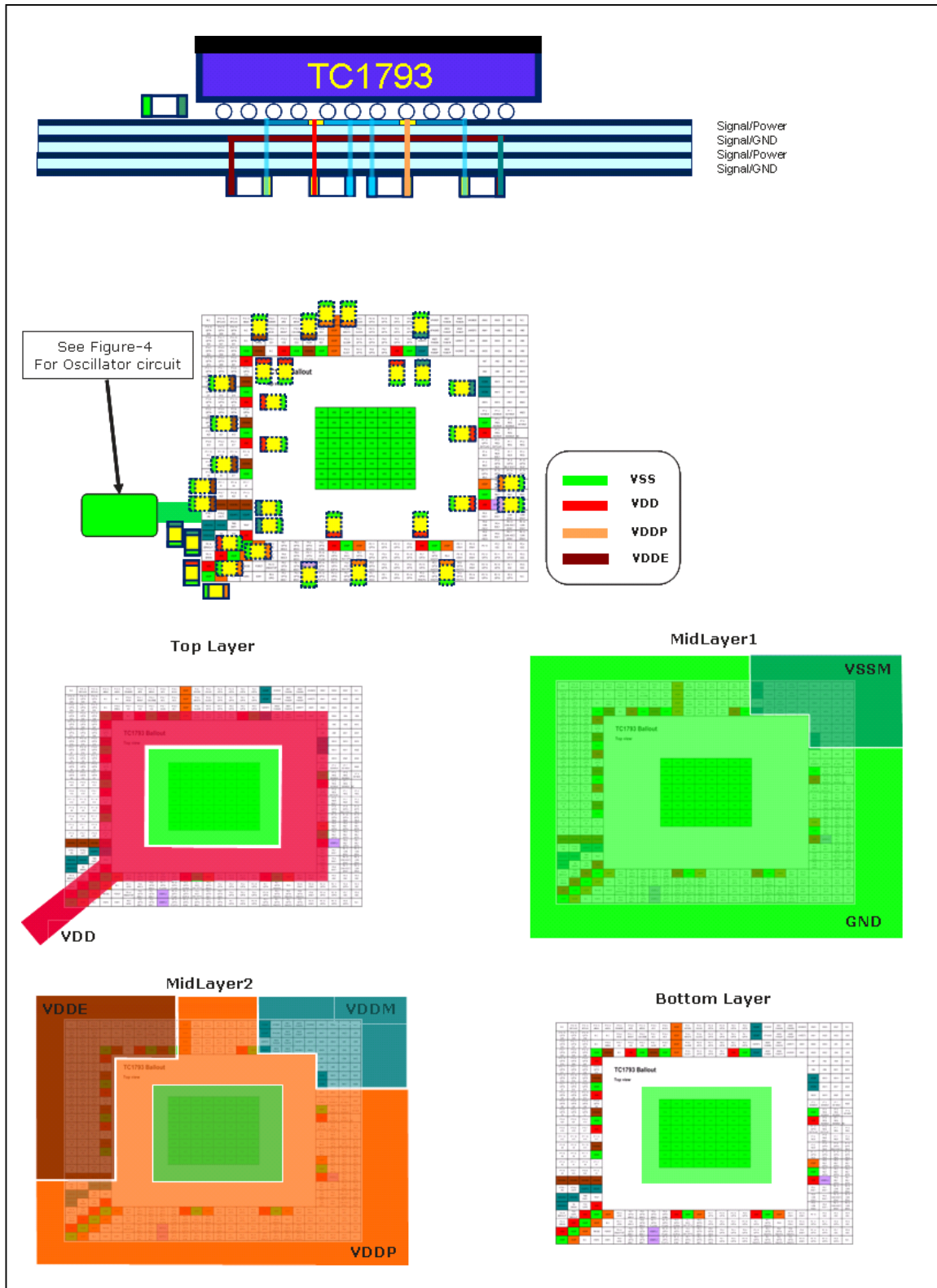


Figure 3 Capacitor Placement Example for Decoupling of TC1793 (BGA-416) on a four layer board

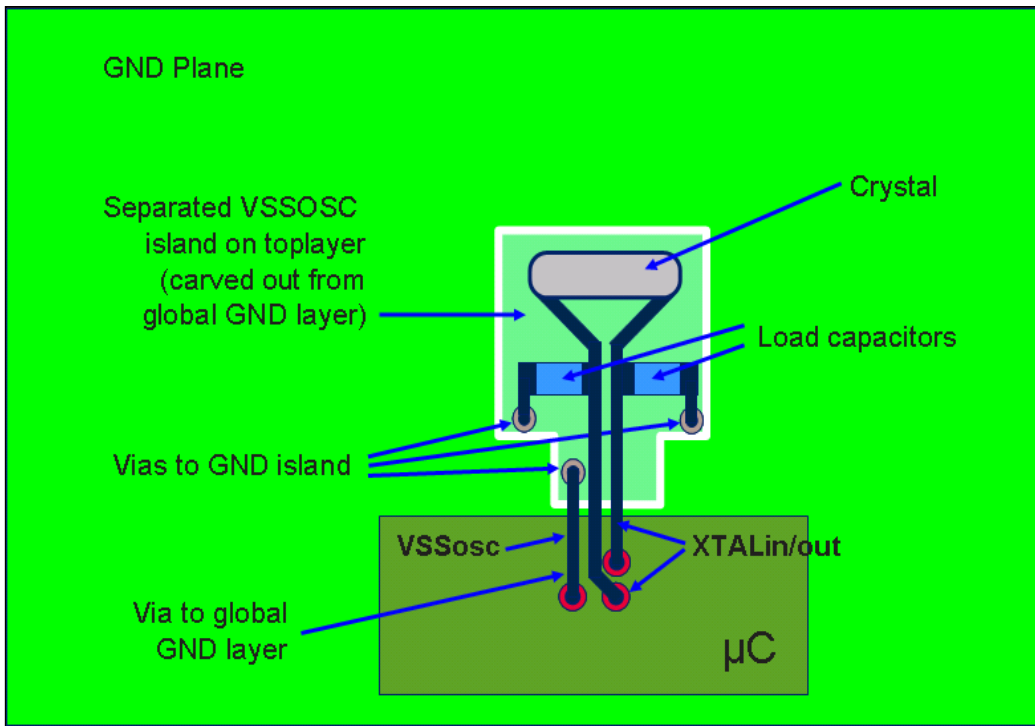


Figure 4 Layout Proposal Oscillator Circuit

2.2 Decoupling Capacitor List:

<u>Capacitor</u>	<u>Supply</u>	<u>Pins(BGA-416)</u>
47 nF	VDD	B26 / C25
47 nF	VDD	D24 / E23
47 nF	VDD	D16
47 nF	VDD	D9
47 nF	VDD	H4
47 nF	VDD	R4
47 nF	VDD	AC11
47 nF	VDD	AC20
47 nF	VDD	AB23
47 nF	VDD	Y23
47 nF	VDD	P23
47 nF	VDDP	A25 / B24
47 nF	VDDP	C23 / D22
47 nF	VDDP	D14
47 nF	VDDP	D7
47 nF	VDDP	K4
47 nF	VDDP	AC16 / AD16
47 nF	VDDP	AE16 / AF16
47 nF	VDDE	H26 / H25
47 nF	VDDE	H24 / H23
47 nF	VDDE	M23
47 nF	VDDE	T23
47 nF	VDDE	Y23
47 nF	VDDE	AC22
47 nF	VDDE	AC18
330 nF	VDDOSC	F26
330 nF	VDDOSC3	E26
47 nF	VDDFL3	H3
47 nF	VDDFL3	A18 / B18
330 nF	VDDPF	G23
330 nF	VDDPF3	G24
47 nF	VDDM	W4
47 nF	VDDMF	AE9
47 nF	VDDAF	AC9

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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