

Stratix V User Guide Lite

By Allan Davidson, Senior Product Manager, Altera Corporation

Altera's 28-nm Stratix[®] V FPGAs deliver the highest bandwidth, highest levels of system integration and ultimate flexibility to the system designer. Featuring several new innovations, this FPGA family enables designers to meet demands for the constantly-growing high bandwidth needs across a broad variety of applications while meeting required cost and power budgets.

As you read this User Guide Lite, you will learn about innovations such as a unique array of integrated hard intellectual property (IP) blocks, integrated transceivers offering up to 28 Gbps, partial reconfiguration for flexible client-side interface, variable precision digital signal processing (DSP) blocks, an enhanced core architecture, plus several other new features, all available in the Stratix V FPGA family. With these innovations, Stratix V FPGAs deliver a new class of application-targeted devices optimized for:

- Bandwidth-centric applications and protocols, including PCI Express Gen3 x8
- Data-intensive applications for 40G/100G and beyond
- Ultra-high bandwidth backplanes and switches
- High-performance, high-precision digital signal processing (DSP) applications

Stratix V Family Variants

Stratix V GT devices, with the industry's only 28 Gbps transceivers (chip-to-chip) as well as 14.1 Gbps transceivers (backplane) are optimized for applications that require ultra-high bandwidth and performance for applications such as 40G/100G/400G optical communications systems and optical test systems.

Stratix V GX devices, with up to 66 integrated 14.1 Gbps transceivers supporting backplanes and optical modules, are optimized for high-performance, high-bandwidth applications such as 40G/100G optical transport, packet processing and traffic management found in wireline, military, communications, and network test equipment markets.

Stratix V GS devices have 4,096 variable precision DSP blocks and integrated 600 Mbps to 14.1 Gbps transceivers that support backplanes and optical modules. These devices are optimized for transceiver-based, DSP-centric applications found in wireline, military, broadcast, and high-performance computing markets.

Stratix V E devices offer the greatest logic density within the Stratix V family, with over one million logic elements (LEs) contributing to the high-performance logic fabric. These devices are optimized for applications such as ASIC prototyping system emulation, diagnostic imaging and instrumentation.

In the transceiver based family variants, the 28 Gbps transceivers cover a continuous range from 20 Gbps to 28 Gbps. The 14.1 Gbps transceivers cover a continuous range from 600 Mbps to 14.1 Gbps, and are supported by a hard physical coding sublayer (PCS) for each transceiver that is used to implement over 50 industry standard and proprietary protocols.

Common to all Stratix V family variants is the enhanced logic array that now supports in-system partial reconfiguration. Also included are a rich set of high performance building blocks, including a redesigned adaptive logic module (ALM), and the new 20 Kbit (M20K) internal memory blocks, variable precision

Page 2

DSP blocks, and fractional clock synthesis PLLs (fPLLs), interconnected by Altera's multi-track routing architecture and comprehensive fabric clocking network.

Also common to Stratix V family variants is the new Embedded HardCopy Block (EHB) which is a customizable hard IP block that leverages Altera's unique HardCopy ASIC capabilities. The EHB is used for hardening standard or logic intensive functions such as interface protocols, application-specific functions and proprietary custom IP. Hardening IP into the EHB frees up valuable core logic resources and reduces overall system power and cost. The EHB blocks in Stratix V include hard IP instantiations of PCI Express Gen3/2/1 and 40GbE/100GbE. This innovation enables Altera to respond faster to customer requirements by hardening other IP into the EHB for future product variants.

Stratix V Family Plan

Tables 1-1, 1-2, 1-3, and 1-4 on pages 6-11 of the <u>Stratix V Device Handbook</u> show the Stratix V GT/GX/GS/E device features.

Moving to HardCopy V Devices

HardCopy V ASICs offer the lowest risk and lowest total cost in ASIC designs with embedded high speed transceivers. You can prototype and debug with Stratix V FPGAs, then use HardCopy V ASICs for volume production. The proven turnkey process creates a functionally-equivalent HardCopy V ASIC with or without embedded transceivers to meet all timing constraints in as little as 12 weeks.

The powerful combination of Stratix V FPGAs and HardCopy V ASICs can help meet your design requirements. Whether you are planning for ASIC production and require the lowest risk, lowest cost path from specification to production or require a cost reduction path for your FPGA-based systems, Altera provides the optimal solution for power, performance, and device bandwidth.

Market Dynamics for High-End Systems

The challenges of increased bandwidth with fixed cost and power budgets are not only being driven by applications like mobile internet and video in communication markets but across many other market segments and applications. The innovations available in the 28-nm Stratix V FPGA family dramatically improve the density and I/O performance of Altera's FPGAs and HardCopy ASICs. With these innovations we address the challenges in a way that takes the industry beyond the benefits of Moore's Law and further strengthens our competitive position vs. ASICs and ASSPs.



Figure 1. Multi-Market Demand for Higher Bandwidth in the Same Footprint with the Same or Lower Power and Cost

The bandwidth growth driven by the mobile Internet affects the wireless infrastructure and causes a fast upgrade of the entire network infrastructure. The march to 40G/100G systems - with 400G on the near horizon - is underway. The need for smaller footprints, lower cost and power is accelerating the introduction of even faster interface technologies like faster transceivers running at 28 Gbps, e.g. for optical transport and OTU-4. FPGAs are a viable alternative to ASICs and ASSPs for packet processing, traffic management, switching and routing solutions.

This trend it is not just in the communication space. The conversion from analog to digital television broadcasting is ongoing and increased bandwidth demands are driven by the proliferation of HD and 1080p worldwide for video production and delivery systems. Military systems require high bandwidth and higher performance, higher precision DSP performance, system reliability and design security to meet the requirements in secure communication, electronic warfare and embedded computing applications. In computer and storage, main drivers are the growth of traffic and data processing at lower latency. Applications like cloud computing drive up bandwidth dramatically but power consumption affects the total cost of ownership.

Stratix V FPGAs – Built for Bandwidth

FPGAs are the platform of choice when it comes to flexibility. With increased integration through extensive hardening of functions, Stratix V FPGAs provides the ultimate flexibility. This is enabled by partial reconfiguration of the FPGA core, as well as dynamic reconfiguration of the transceivers. With partial reconfiguration, you can increase your system functionality dramatically and achieve faster reconfiguration while also reducing power.

Following are brief summaries of the key new innovations that enable the highest bandwidth and integration in your system, while achieving a 50% increased system performance and lowering the total power by 30% compared to the previous generation Stratix IV FPGAs.

Embedded HardCopy Blocks

Embedded HardCopy Blocks (EHB) are customizable hard intellectual property (IP) blocks that leverage Altera's unique HardCopy ASIC capabilities. This innovation substantially increases FPGA capabilities by dramatically increasing density per area and offering up to 14M ASIC gates or up to 700K logic elements. There are significant performance and power benefits - 2X the performance at up to 65% - lower power by using the hard IP rather than soft logic.

The difference to a traditional use of hard IP is the HardCopy methodology which allows customers to take advantage of product variants or implement their custom functions quickly and efficiently without the mask and development cost-associated with a full chip design.

The EHB Blocks harden standard or logic-intensive functions such as application-specific functions, transceiver protocols and proprietary customer IP functions. This offers customers faster time to market for their designs, higher bandwidth and performance while reducing cost and power. For Altera, this innovation allows the company to quickly – usually less than 3-6 months - create variant products for target applications.

Embedded	Embedded	
HardCopy Block	HardCopy Block	

Figure 2. Altera's new Embedded HardCopy Block in Stratix V FPGAs

PCI Express Gen 3/2/1 Hard IP (EHB)

The Stratix V devices have PCI Express hard IP designed for performance, ease-of-use and increased functionality. The PCI Express hard IP consists of the PCS, Data Link and Transaction layers. The PCI Express hard IP supports Gen 3/2/1 End Point and Root Port up to a ×8 lane configuration. The Stratix V PCI Express hard IP operates independently from the core logic which enables the PCI Express link to wake up and complete link training in less than 100 ms, while the Stratix V device completes loading the programming file for the rest of the FPGA. It also provides added functionality, making it easier to support emerging features such as Single Root IO Virtualization (SR-IOV) or optional protocol extensions. In addition, the Stratix V device PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC) and now supports Configuration via PCI Express. See detailed description in the <u>Stratix V Device Handbook</u>.

40G and 100G Ethernet Hard IP (EHB)

The 40G and 100G Ethernet hard IP in Stratix V GT and Stratix V GX devices is standards- compliant and proven. The Hard IP includes 40GBASE-R PCS and XLAUI PMA for 40GE, and 100GBASE-R PCS and CAUI PMA for 100GE. The 40G and 100G Ethernet hard IP are scalable because applications requiring multiple 40/100 GbE ports may use a single PLL for the 40/100GBASE-R PCS instantiations to reduce FPGA core and clock resources.

Furthermore, the integrated 10G transceiver simplifies multi-port 40/100GbE systems implementation by reducing chip count, board space, and power. Stratix V transceivers interface directly with 40Gbps QSFP and SFP, and 100 Gbps CFP pluggable modules.



Figure 3. Stratix V Hard IP Variants Support Configuration via PCI Express

Interlaken PCS Hard IP

Stratix V devices have integrated Interlaken PCS hard IP supporting up to 24 channels at up to 14.1 Gbps. It is based on the soft IP proven in Stratix IV GX devices to interoperate with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in the Stratix V GX, GT, and GS devices.

10G Ethernet Hard IP

Stratix V GS, GT, and GX devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The Ethernet PHY with the embedded 10.3125 Gbps serial transceivers completes the 10GbE solution. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations which saves core logic resources and clock networks.

The 10G integrated transceivers simplify multi-port 10GbE systems as compared with XAUI interfaces that require an external XAUI to 10G PHY. Further, the integrated 10G transceivers incorporate Electronic Dispersion Compensation (EDC) which enables direct connection to standard 10 Gb XFP and SFP+ pluggable modules. Additionally, the 10G transceivers support backplane applications. The integrated 10G transceivers save external PHY cost, board space and system power.

The 10G Ethernet PCS hard IP is present in every transceiver channel in Stratix V devices.

Variable Precision DSP Block

Signal processing applications increasingly demand not only higher performance but also higher precision – and indeed different precision levels make sense at different stages of the signal processing data paths. For example, video broadcast applications can use multipliers ranging from 9x9 to all the way up to 18x18. Other applications such as wireless and medical systems push the precision needs even further as they develop complex, multi-channel filters with the need to maintain data precision after each stage of the filter. Then there are applications within the military, test and high-performance computing industries that push the envelope in terms of both performance and precision – sometimes even requiring the need for single/double precision floating point when implementing complex matrix operations and FFTs.



Figure 4. Industry's First Variable-Precision DSP Block - Set the Precision Dial to Match your Application

Stratix V FPGAs feature the industry's first variable precision DSP block that can be configured to natively support signal processing with precision ranging from 9×9 all the way up to 54×54. The DSP blocks are designed to be cascaded with the widest, dedicated cascade bus in the industry – 64 bits. This allows the building of DSP data paths of even higher precision in the most efficient manner with maximum performance.

The variable precision DSP block is designed to enable the most silicon efficient implementation of your signal processing chain. It is the industry's only DSP block architecture to feature a configurable 18/26 pre-adder, a 64-bit accumulator + cascade bus and an internal co-efficient storage – all designed to allow the most area efficient implementation of common functions such as FIR filters, FFTs and floating point. While this block is backward compatible with all the existing modes supported by our 65-nm and 40-nm devices, it adds native, efficient support for a range of higher precision modes.

Each DSP block can be independently configured at compile time as either dual 18×18 or a single 27×27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently. Table 5 shows how different precision is accommodated within a DSP block or by utilizing multiple blocks.

Multiplier Size	DSP Block Resources	Expected Usage	
9×9 bit	1/3 of Variable Precision DSP Block	Low precision fixed point	
18×18 bit	1/2 of Variable Precision DSP Block	Medium precision fixed point	
27×27 bit	1 Variable Precision DSP Block	High precision fixed or single precision floating point	
36×36 bit	2 Variable Precision DSP Blocks	Very high precision fixed point	
54×54 bit	4 Variable Precision DSP Blocks	Double precision floating point	

Table 1. Variable Precision DSP Block Configurations

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The variable precision DSP block is designed to support this with proportional increase in DSP resources with precision growth.

Multiplier Size	DSP Block Resources	Expected Usage
18×18 bits	2 Variable Precision DSP Blocks	Resource optimized FFTs
18×25 bits	3 Variable Precision DSP Blocks	Accommodate bit growth through FFT stages
18×36 bits	4 Variable Precision DSP Blocks	Highest precision FFT stages
27×27 bits	4 Variable Precision DSP Blocks	Single precision floating point

Table 2. Complex Multiplication with Variable Precision DSP Blocks

Additionally, for FFT applications with high dynamic range requirements, only the Altera FFT Megacore offers an option of single precision floating point implementation, with resource usage and performance similar to high precision fixed point implementations.

Other new features include:

- 64-bit accumulator, the largest in the industry
- Hard Pre-adder, available in both 18 and 27 bit modes
- Cascaded output adders, for efficient systolic FIR filters
- Internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single and double precision floating point arithmetic
- Inferability of all modes by the Quartus II design suite

The variable precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. The Stratix V FPGA series, with the variable precision DSP block architecture, is the only FPGA family that can efficiently support many different precision levels, up to and including floating point implementations. This flexibility results in increased system performance, reduced power consumption and reduced architecture constraints on system algorithm designers.

Easy-to-Use Partial Reconfiguration

Partial reconfiguration allows designers to reconfigure designated sections of the FPGA while other sections remain running. This is required in systems where uptime is critical. It allows customers to make updates or adjust functionality without disrupting device operation, while lowering power and cost. Partial reconfiguration also increases the effective logic density by removing the necessity to place FPGA functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as required. This reduces the size of the FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power.

Partial reconfiguration solutions typically have been time-intensive tasks that required designers to know the majority of the intricate FPGA architecture details. Altera has simplified the partial reconfiguration process by building the capability on top of a proven methodology using LogicLock[™] and incremental compile design flow in its Quartus II design software.



Figure 5. Partial Reconfiguration for the FPGA Core

Partial reconfiguration is supported through the following configuration options:

- Partial reconfiguration through the FPP ×16 I/O interface
- Configuration via PCI Express
- Soft internal core such as the Nios[®] II embedded processor

Dynamic reconfiguration on the other hand enables data rates or encoding schemes to be changed dynamically while maintaining data transfer on adjacent transceiver channels in Stratix V GT/GX/GS devices. Dynamic reconfiguration is ideal for applications requiring on-the-fly multi-protocol or multi-rate support. The PMA and PCS blocks can be reconfigured with dynamic reconfiguration, thus providing the ultimate flexibility which in turn enables differentiation.

Partial reconfiguration can be seamlessly used in tandem with dynamic reconfiguration to enable partial reconfiguration of both core and I/O simultaneously. Application operation is not affected during reconfiguration, there is no system downtime with dynamic updates, thus allowing faster reconfiguration and reducing cost and power through integration.

Embedded Low Power Serial Transceivers

Stratix V FPGAs deliver the industry's most flexible transceivers with the highest bandwidth from 600 Mbps to 28 Gbps, low Bit Error Ratio (BER), and low power. Many enhancements have been made to the Stratix V transceivers, which improve flexibility and robustness. These enhancements include:

- Low jitter LC (inductor-capacitor) Transmit PLLs
- Robust analog receive Clock and Data Recovery (CDR)
- Advanced pre-emphasis and equalization for 14.1 Gbps backplanes
- 28 Gbps chip-to-chip transceivers (Stratix V GT)
- On-chip instrumentation

In addition, all transceivers are identical with full-featured embedded PCS hard IP to simplify the design, lower the power and save valuable core resources. Stratix V transceivers are designed to be standard-compliant for a wide range of <u>protocols</u> and data rates, and are equipped with a variety of signal conditioning features to support backplane, optical module and chip-to-chip applications.

The transceivers are positioned on the outer edges of the chip as shown in Figure 6. They are isolated from the rest of the chip to prevent core and I/O noise from coupling into the transceivers; thereby ensuring optimal signal integrity. The transceiver channels consist of the Physical Medium Attachment

Altera Corporation

Page 8

(PMA), Physical Coding Sub-layer (PCS), ultralow jitter LC transmit PLLs and clock networks. Unused transceiver PMA channels can also be used as additional transmit PLLs. Reference clocks for the transceivers are either derived from off-chip oscillators, or generated on-chip with the precise frequency synthesis capabilities of the fPLLs (see Page 11 for detailed description). fPLLs synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators in multi-protocol or multi-rate applications.

The Stratix V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64 or 66-bit interface, depending on the transceiver data rate and protocol. Stratix V devices contain PCS hard IP to support PCI Express Gen 3/2/1, 40G/100G Ethernet, Interlaken, 10GE, XAUI, GbE, SRIO, CPRI and GPON (see Table 3 for PMA features). All other standard and proprietary protocols from 600 Mbps to 14.1 Gbps are supported through the 10G Basic (up to 14.1 Gbps), 6G Basic (up to 8.5 Gbps) and 3G Basic (up to 3.75 Gbps) transceiver PCS hard IP. Table 4 lists the transceiver PCS features.



Notes to Figure 6:

(1) This figure represents a given variant of a Stratix V device with transceivers. Other variants may have a different floorplan than the one shown here.

(2) You can use the unused transceiver channels as additional transceiver transmit PLLs.

Figure 6. Stratix V GT/GX/GST Device Chip View

Features	Capability
Backplane support	10GBase-KR, 14.1 Gbps (Stratix V GT/GX/GS devices)
Optical module support with Electronic Dispersion Compensation (EDC)	10G Form-factor Pluggable (XFP), Small Form-factor Pluggable (SFP+), Quad Small Form-factor Pluggable (QSFP), CXP, 100G Pluggable (CFP), 100G Form-factor Pluggable
Cable driving support	PCI Express cable and eSATA applications
Chip-to-chip support	28 Gbps (Stratix V GT devices),14.1 Gbps (Stratix V GT/GX/GS devices)
Continuous Time Linear Equalization (CTLE)	Receiver 4-stage linear equalization to support high-attenuation channels
Decision Feedback Equalization (DFE)	Receiver 5-tap digital equalizer to minimize losses and crosstalk
Adaptive equalization (ADCE)	Adaptive engine to automatically adjust equalization to compensate for changes over time
PLL-based clock recovery	Superior jitter tolerance versus phase interpolation techniques
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment patterns
Transmit equalization (pre-emphasis)	Transmit driver 4 tap pre-emphasis and de-emphasis for protocol compliance under lossy conditions
Ring and LC oscillator transmit PLLs	Choice of transmit PLLs per channel, optimized for specific protocols and applications
On-chip instrumentation (EyeQ data-eye monitor)	Allows non-intrusive on-chip monitoring of both width and height of data eye
Dynamic reconfiguration	Allows reconfiguration of single channels without affecting operation of other channels
Protocol support	Compliance with over 50 industry standard protocols in the range 600 Mbps to 28 Gbps

Table 3. Transceiver PMA Features

Protocol	Data Rates (Gbps)	Transmit Data Path	Receiver Data Path		
Custom PHY	0.6 to 8.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Word aligner, de-skew FIFO, rate match FIFO, 8B/10B decoder, byte deserializer, and byte ordering		
Custom 10G PHY	9.98 to 14.1	TX FIFO, gear box and bit-slipper	RX FIFO and gear box		
×1, ×4, ×8 PCle Gen 1/2	2.5 and 5.0	Same as custom PHY plus PIPE 2.0 interface to core logic	Same as custom PHY plus PIPE 2.0 interface to core logic		
x1, x4, x8 PCle Gen 3	8.5	Phase compensation FIFO, encoder, scrambler, gear box, and bit slip	Block synchronization, rate match FIFO, decoder, de-scrambler, and phase compensation FIFO		
10G Ethernet	10.3125	TX FIFO, 64/66 encoder, scrambler, and gear box	RX FIFO, 64/66 decoder, de-scrambler, block synchronization, and gear box		
Interlaken	4.9 to 14.1	TX FIFO, frame generator, CRC-32 generator. scrambler, disparity generator, and gear box	RX FIFO, frame generator, CRC-32 checker, frame decoder, descrambler, disparity checker, block synchronization, and gear box		
40GBASE-R Ethernet	4 × 10.3125	TX FIFO, 64/66 encoder, scrambler,	RX FIFO, 64/66 decoder, de-scrambler, lane reorder, deskew, alignment marker lock, block synchronization, gear box, and destripper		
100GBASE-R Ethernet	10 × 10.3125	and block striper			
	(4 +1) × 11.3	TX FIFO, channel bonding, and byte	RX FIFO, lane deskew, and byte de-		
OTN 40 and 100	(10 +1) × 11.3	serializer	serializer		
GbE	1.25	Same as custom PHY plus GbE state machine	Same as custom PHY plus GbE state machine		
XAUI	3.125 to 4.25	Same as custom PHY plus XAUI state machine for bonding 4 channels	Same as custom PHY plus XAUI state machine for re-aligning 4 channels		
SRIO	1.25 to 6.25	Same as custom PHY plus SRIO V2.1 compliant ×2 and ×4 channel bonding	Same as custom PHY plus SRIO V2.1 compliant x2 and x4 deskew state machine		
CPRI	0.6144 to 9.83	Same as custom PHY plus TX deterministic latency	Same as custom PHY plus RX deterministic latency		
GPON	1.25 and 2.5	Same as custom PHY	Same as custom PHY		

Table 4. Transceiver PCS Features

External Memory and General Purpose I/O

Stratix V devices offer high I/O bandwidth with up to seven 72-bit DDR3 memory interfaces running at 1066 MHz / 2133 Mbps and ubiquitous LVDS running at 1.4 Gbps. This translates to an aggregate memory bandwidth of 1075 Gbps and LVDS bandwidth of 315 Gbps.

Significant architectural enhancements in the I/O blocks increase the overall external memory performance (see Figure 6). First, all timing critical circuits in the DDR read-and-write paths are hardened in the I/O block to enable timing closure at 1066 MHz. Second, each I/O block has a hard FIFO that improves the resynchronization margin as the data is transferred from memory to the FPGA. The hard FIFO also lowers PHY latency, resulting in higher random access performance. Third, the I/Os include on-chip dynamic termination to reduce the number of external components and minimize reflections. Altera Corporation

Page 12

Fourth, the on-package decoupling (OPD) capacitors suppress noise on the power lines, which reduce noise coupling into the I/Os. Last, the memory banks are isolated to prevent core noise from coupling to the output; thus reducing jitter and providing optimal signal integrity.

The external memory interface block also uses advanced calibration algorithms to compensate for PVT (process, voltage and temperature) variations in the FPGA and external memory components. These advanced algorithms ensure maximum bandwidth and robust timing margin across all conditions. Stratix V devices also deliver a complete memory solution with High Performance Memory Controller II (HPMC II) and UniPHY Megacores that simplify design for today's advanced memory modules. Table 5 shows external memory interface block performance.



Hard IP

Figure 7. Stratix V FPGA PHY Architecture (UniPHY) for Implementing Memory Subsystems Quickly and Easily

Interface	Performance		
DDR3	1066 MHz		
DDR2	533 MHz		
QDR II	400 MHz		
QDR II+	667 MHz		
RLDRAM III	800 MHz		
RLDRAM II	667 MHz		

Table 5. External Memory Interface Performance

Adaptive Logic Module (ALM)

Stratix V devices use an improved adaptive logic module (ALM) to implement logic functions more efficiently. The ALM shown in Figure 8 has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders and four dedicated registers.



Figure 8. Stratix V Device ALM

The new ALM has the following enhancements:

- Packs 6% more logic compared to the traditional ALM found in Stratix IV devices
- Implements select 7-input LUT-based functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core utilization
- Adds more registers (4 registers per 8-input fracturable LUT). This enables Stratix V devices to maximize core performance at a higher core logic utilization and provides easier timing closure for register rich and heavily pipelined designs

The Quartus II design software leverages the Stratix V ALM logic structure to deliver the highest performance, optimal logic utilization and lowest compile times. The Quartus II design software simplifies design reuse as it automatically maps legacy Stratix designs into the new Stratix V ALM architecture.

Clocking

The Stratix V device core clock network is designed to support 717 MHz fabric operation and 1066 MHz/2133 Mbps external memory interfaces. The clock network architecture is based on Altera's proven global, quadrant and peripheral clock structure which is supported by dedicated clock input pins and fractional clock synthesis PLLs. All unused sections of the clock network are identified by the Quartus II design software and powered down to reduce power consumption.

Fractional PLL (fPLL)

Stratix V devices have up to 28 fractional PLLs (fPLLs) that can be used to reduce the number of oscillators required on a board, as well as reduce clock pins used in the FPGA by synthesizing multiple clock frequencies from a single reference clock source. Additionally, the fPLLs can be used for clock network delay compensation, zero-delay buffering and transmit clocking for transceivers. fPLLs may be individually configured for conventional integer mode, which is equivalent to a general purpose PLL (GPLL), or enhanced fractional mode with third-order delta-sigma modulation. The fPLLs also support cascading to and from the transceiver CMU and LC PLLs, thus enabling optical transport muxponder applications that require precise transmit frequency generation and recovered clock cleanup. Figure 9 shows a typical application.





Figure 9. fPLLs in Stratix V FPGAs Reduce Cost, Power, and Board Space

Embedded Memory

Stratix V devices contain two types of embedded memory blocks: MLAB (640-bit) and M20K (20-Kbit). MLAB blocks are ideal for wide and shallow memories. M20K blocks are useful for supporting larger memory configurations and include ECC. Both types operate up to 600 MHz and are configurable to be a single- or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are flexible and support a number of memory configurations as shown in Table 6, while improving area efficiency and higher system performance.

MLAB (640 Bits)	M20K (20,480 Bits)	
32×20	512×40	
64×10	1K×20	
	2K×10	
	4K×5	
	8K×2	
	16K×1	

Table 6. Internal Memory Block Configuration

Quartus II design software simplifies design reuse by automatically mapping memory blocks from previous generations into Stratix V MLAB or M20K blocks.

Power Management

Stratix V devices leverage FPGA architectural features and process technology advancements to reduce total power consumption by as much as 30% compared to Stratix IV devices at the same performance level.

Stratix V devices continue to provide Programmable Power Technology, introduced in earlier generations of Stratix FPGA families. With Programmable Power Technology, the Quartus II design software PowerPlay feature identifies critical timing paths in a design and biases core logic in that path for high performance (see Figure 10). The PowerPlay feature also identifies non-critical timing paths and biases core logic in that path for low power instead of high performance. PowerPlay monitors the slack of each

circuit domain and automatically biases core logic to meet performance and optimize power consumption.

Additionally, Stratix V devices have a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. The list includes PCI Express Gen 3/2/1, 10G/40G/100G Ethernet, Interlaken PCS, hard I/O FIFOs and transceivers. Hard IP blocks consume up to 50% less power than equivalent soft implementations.

Stratix V transceivers are also designed for power efficiency. As a result, the transceiver channels consume 50% less power than the previous generation Stratix IV FPGAs. The transceiver PMA consumes 90mW at 6.5 Gbps and 170 mW at 12.5 Gbps.

Lastly, Stratix V devices are built on TSMC high-performance, high-k metal gate (HKMG), 28-nm process node. 28-nm silicon operates at a supply voltage of 0.85 V whereas 40-nm silicon operates at 0.90 V. The 50 mV lower supply voltage also reduces FPGA power consumption, translating to a 12% dynamic power savings.



Figure 10. Stratix V FPGAs Deliver 30% Less Total Power, while Providing the Industry's Highest Performance

Incremental Compilation

The Quartus II design software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure. Incremental compilation supports top-down, bottomup, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently, and then you can import these blocks into the top-level project. The incremental compilation feature enables the partial reconfiguration flow of Stratix V devices.

Enhanced Configuration and Configuration via PCI Express

Stratix V device configuration is enhanced for ease-of-use, speed and cost. These devices support a new 4bit bus Active Serial mode (AS×4) and Configuration by Protocol (CvP), where ASx4 supports up to 400 Mbps data rate using small low cost quad interface Flash devices. This new mode is easy to use and offers an ideal balance between cost and speed. Finally the Fast Passive Parallel (FPP) interface is enhanced to support 8-, 16-, and 32-bit data widths to meet a wide range of performance and cost goals.

Stratix V FPGAs can now be configured through PCI Express CvP instead of an external flash or ROM. CvP offers the fastest configuration rate and flexibility with the easy-to-use PCI Express hard IP block interface. CvP meets the PCI Express 100 ms power-up to active time requirement. Stratix V devices and the Quartus II software support partial reconfiguration through CvP, which reduces system downtime by keeping the PCI Express link alive while the FPGA is reconfigured.

Mode	Fast or Slow POR	Compression	Encryption	Remote Update	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)
Active Serial	~	~	~	~	1, 4	100	400
Passive Serial	~	~	~	_	1	125	125
Passive Parallel	~	~	~	Remote update support with Parallel Flash Loader.	8, 16, 32	125	3,000
Configuration via PCIe	_	_	~	~	1, 2, 4, 8	_	3,000
Partial Reconfiguration	_	_	~	~	16	125	2,000
JTAG	_	_	_	_	1	33	33

Note to Table 7:

(1) Remote update support with Parallel Flash Loader.

Table 7. Stratix V Device Configuration Modes

Automatic Single Event Upset (SEU) Error Detection and Correction

Stratix V devices offer new SEU error detection and correction circuitry that is easy to use and robust. The correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through a core programming file reload that provides a complete design refresh while the FPGA continues to operate.

Furthermore, the physical layout of the FPGA is optimized to make the majority of multi-bit upsets appear as independent single- or double-bit errors, which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection in Stratix V devices, the user memories also include integrated ECC circuitry and are layout optimized to enable error detection of 12-bit errors and correction for 8-bit errors.

Design Security

Stratix V FPGAs secure designs through industry-leading anti-tamper features including an enhanced AES algorithm in accordance with FIPS-197, 256-bit volatile and non-volatile keys with key bits scrambled, key bits placed under layers of metal and key bits distributed among other logic, as well as tamper-protection bit which accepts only encrypted configuration files and easy to use on-board and offboard key programming.

Summary

With innovations such as Embedded HardCopy Blocks, Variable Precision DSP Blocks, Partial Reconfiguration and Embedded 28-Gbps transceivers, Altera's new 28-nm Stratix V FPGAs are moving the industry beyond the benefits of Moore's Law, while solving the challenge of increasing bandwidth and staying within designer's cost and power requirements. Altera continues to dramatically improve the density and I/O performance of their FPGAs, and further strengthens its competitive position versus ASICs and ASSPs. From the core to the I/O, Altera is delivering innovations that provide higher system performance at lower cost and power. Stratix V FPGAs break through the bandwidth barrier.

For complete and detailed information on Stratix V FPGAs, see Stratix V Device Handbook

Features Summary

- Technology
 - 28-nm TSMC process technology
 - 0.85-V core voltage
- Low-power serial transceivers
 - 28-Gbps transceivers on Stratix V GT devices
 - Electronic Dispersion Compensation (EDC) for XFP, SFP+, QSFP, CFP optical module support
 - Adaptive linear and decision feedback equalization
 - 600 Mbps to 14.1 Gbps backplane capability
 - Transmit pre-emphasis and de-emphasis
 - Dynamic reconfiguration of individual channels
 - On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
- General purpose I/Os
 - 1.4-Gbps LVDS
 - 1066-MHz/2133-Mbps external memory interface
 - On-chip termination (OCT)
 - 1.2-V to 3.3-V interfacing for Stratix V GX/GS/E devices
 - 1.2-V to 2.5-V interfacing for Stratix V GT devices
- Embedded Hardcopy Block
 - PCle Gen 3/2/1 complete protocol stack, ×1/×2/×4/×8 end point and root port
 - 40G/100G Ethernet PCS
- Embedded transceiver hard IP
 - Interlaken PCS
 - Gigabit Ethernet (GbE) and XAUI PCS
 - 10G Ethernet PCS
 - Serial RapidIO (SRIO) PCS
 - Common Public Radio Interface (CPRI) PCS
 - Gigabit Passive Optical Networking (GPON) PCS
- Power Management
 - Programmable Power Technology
 - Quartus II integrated PowerPlay Power Analysis
- High-performance core fabric
 - Enhanced ALM with four registers
 - Improved routing architecture reduces congestion and improves compile times

- Embedded memory blocks
 - M20K: 20-Kbit with hard error correction coding (ECC)
 - MLAB: 640-bit
- Variable precision DSP blocks
 - Up to 500 MHz performance
 - Natively support signal processing with precision ranging from 9×9 up to 54×54
 - New native 27×27 multiply mode
 - 64-bit accumulator and cascade for systolic FIRs
 - Embedded internal coefficient memory
 - Pre-adder/subtractor improves efficiency
 - Increased number of outputs allows more independent multipliers
- Fractional PLLs
 - Fractional mode with third-order delta-sigma modulation
 - Integer mode
 - Precision clock synthesis, clock delay compensation, and zero delay buffering
- Clock networks
 - 717-MHz fabric clocking
 - Global, quadrant, and peripheral clock networks
 - Unused clock networks can be powered down to reduce dynamic power
- Device Configuration
 - Serial and parallel flash interface
 - Enhanced advanced encryption standard (AES) design security features
 - Tamper protection
 - Partial and dynamic reconfiguration
 - Configuration via PCIe
- High-performance packaging
 - Multiple device densities with identical package footprints enables seamless migration between different FPGA densities
 - FBGA packaging with on-package decoupling capacitors
 - Lead and RoHS-compliant lead-free options
- HardCopy V migration