LPC11U1x

32-bit ARM Cortex-M0 microcontroller; up to 32 kB flash; 6 kB SRAM; USB device; USART

Rev. 1 — 11 April 2011 Objective data sheet

1. General description

The LPC11U1x are a ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11U1x operate at CPU frequencies of up to 50 MHz.

Equipped with a highly flexible and configurable Full Speed USB 2.0 device controller, the LPC11U1x brings unparalleled design flexibility and seamless integration to today's demanding connectivity solutions.

The peripheral complement of the LPC11U1x includes up to 32 kB of flash memory, 6 kB of SRAM data memory, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, a 10-bit ADC, and up to 40 general purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 32 kB on-chip flash program memory.
  - Total of 6 kB SRAM data memory (4 kB main SRAM and 2 kB USB SRAM).
  - 16 kB boot ROM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Debug options:
  - Standard JTAG test/debug interface.
  - Serial Wire Debug.
  - Boundary scan for simplified board testing.
- Digital peripherals:
  - Up to 40 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can beselected as edge and level sensitive interrupt sources.

- Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- High-current source output driver (20 mA) on one pin (P0_7).
- High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
- Four general purpose counter/timers with a total of up to 5 capture inputs and 13 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range –40 °C to +85 °C.
- Available as 48-pin LQFP, 48-pin TFBGA, and 33-pin HVQFN package.
- Pin compatible to the LPC134x series.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

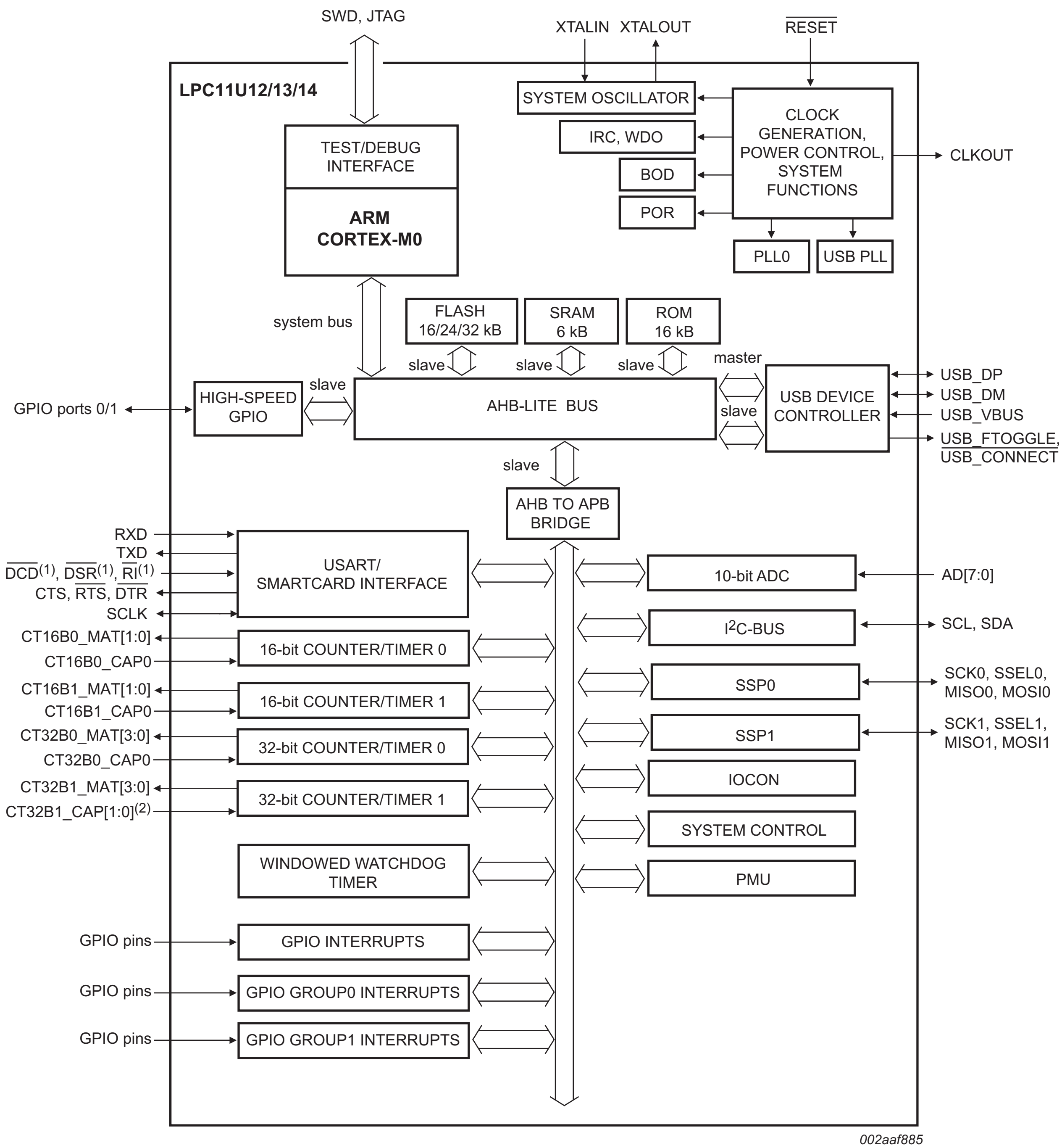
Type number	Package		
	Name	Description	Version
LPC11U12FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U12FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U13FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U14FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FET48/201	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM			USART	I²C-bus FM+	SSP	USB device	ADC channels	GPIO pins
		CPU	USB	Total						
LPC11U12FHN33/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U12FBD48/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U13FBD48/201	24 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FHN33/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U14FBD48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FET48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40

5. Block diagram



(1) Not available on HVQFN33 packages.

(2) CT32B1_CAP1 available in TFBGA48 only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

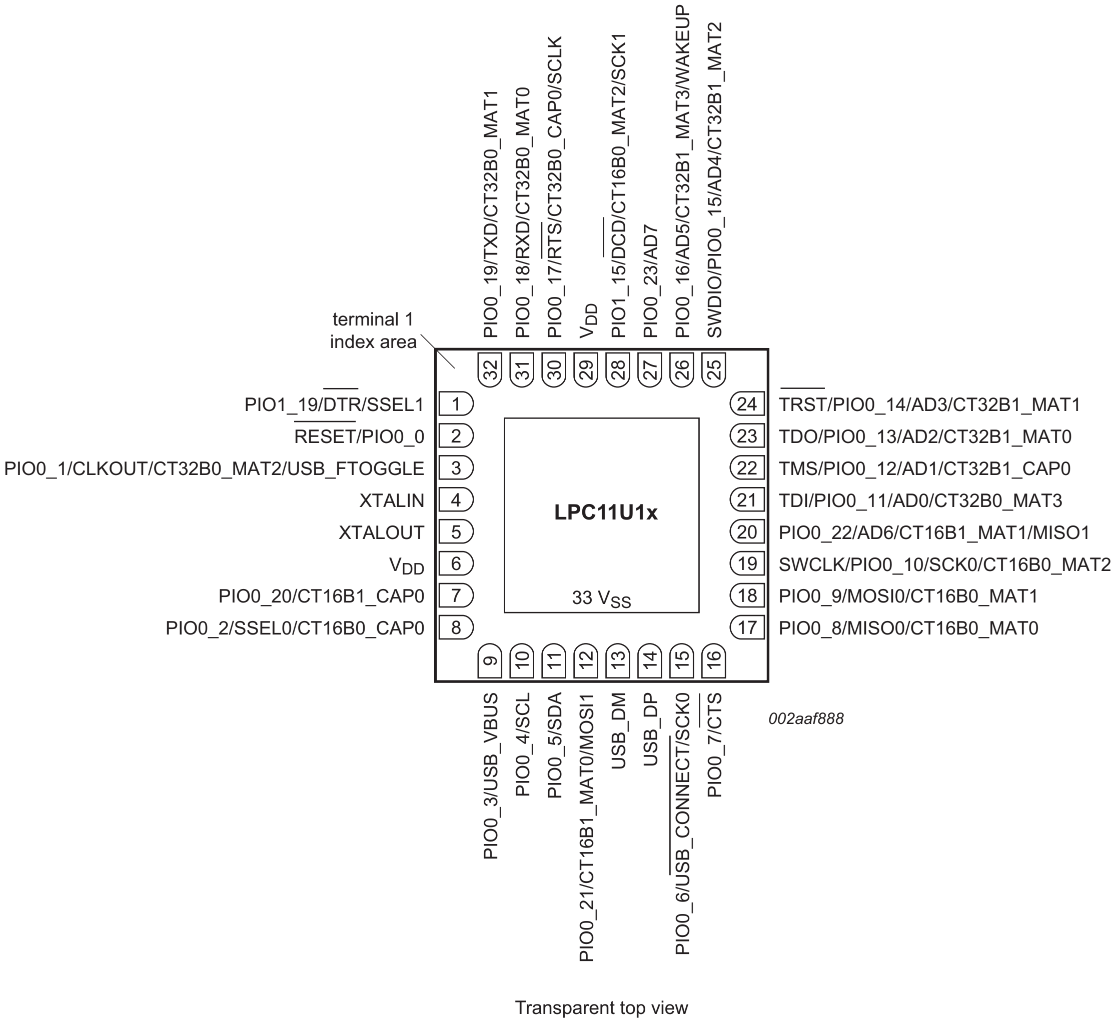


Fig 2. Pin configuration (HVQFN33)

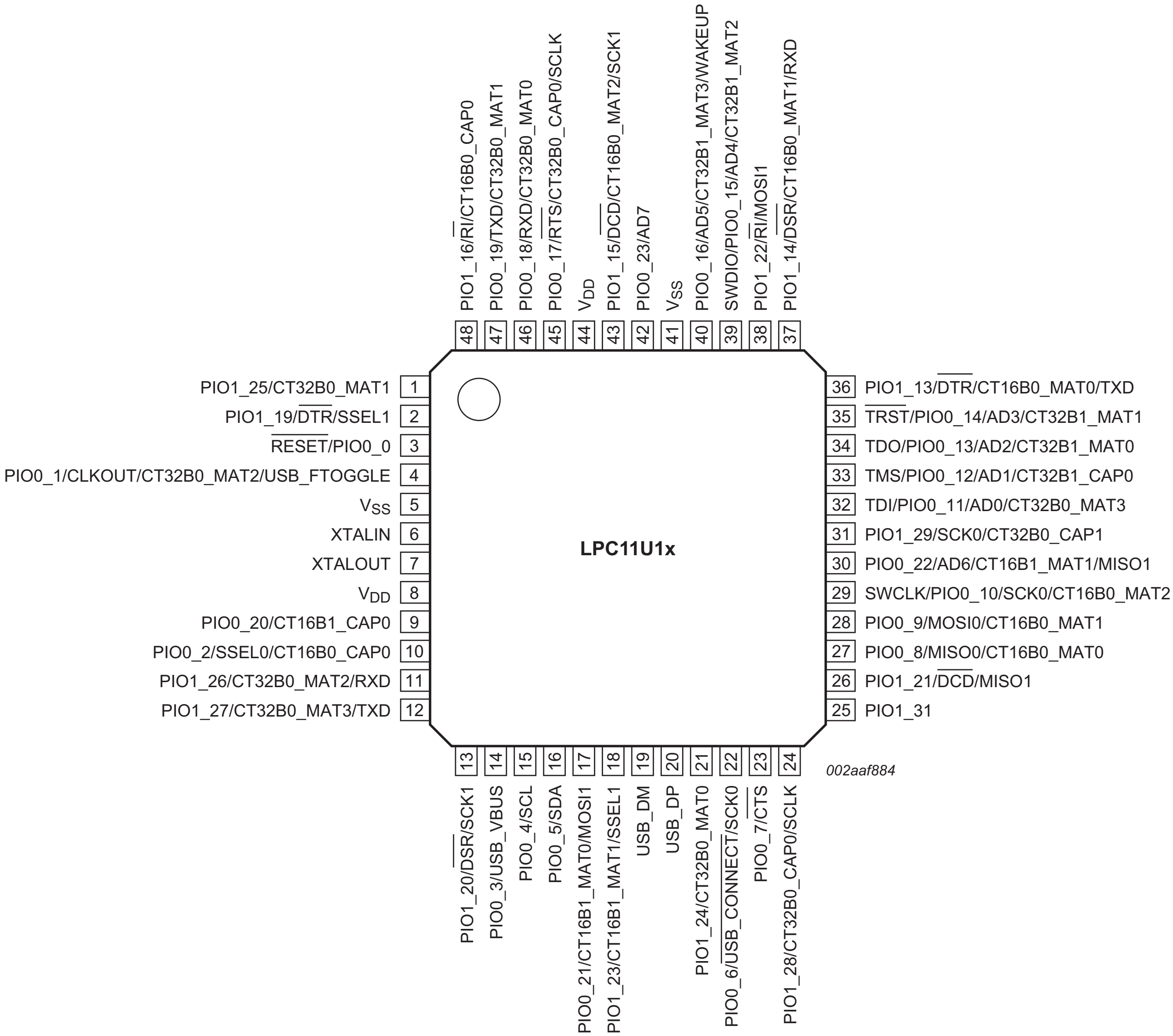


Fig 3. Pin configuration (LQFP48)

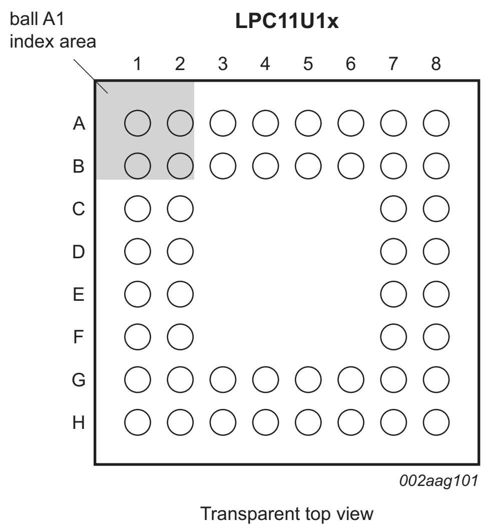


Fig 4. Pin configuration (TFBGA48)

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions ordered by GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register through which the digital or analog function, pull-up/pull-down configuration, repeater, and open-drain modes can be programmed.

The USART, counter/timer, and SSP functions are available on more than one port pin. Table 4 shows how peripheral functions are assigned to port pins.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
RESET/PIO0_0	2	3	C1	[2]	I; PU	I	**RESET —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	4	C2	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	8	10	F1	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
					-	I/O	**SSEL0 —** Slave select for SSP0.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	9	14	H2	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler, a HIGH level starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
PIO0_4/SCL	10	15	G3	[4]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^{2}C-bus clock input/output (open-drain). High-current sink only if I^{2}C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11	16	H3	[4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^{2}C-bus data input/output (open-drain). High-current sink only if I^{2}C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/USB_CONNECT/ SCK0	15	22	H6	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/CTS	16	23	G7	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**CTS —** Clear To Send input for USART.
PIO0_8/MISO0/ CT16B0_MAT0	17	27	F8	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18	28	F7	[3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19	29	E7	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21	32	D8	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	33	C7	[6]	I; PU	I	**TMS** — Test Mode Select for JTAG interface.
					-	I/O	**PIO_12** — General purpose digital input/output pin.
					-	I	**AD1** — A/D converter, input 1.
					-	I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	34	C8	[6]	I; PU	O	**TDO** — Test Data Out for JTAG interface.
					-	I/O	**PIO0_13** — General purpose digital input/output pin.
					-	I	**AD2** — A/D converter, input 2.
					-	O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	35	B7	[6]	I; PU	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
					-	I/O	**PIO0_14** — General purpose digital input/output pin.
					-	I	**AD3** — A/D converter, input 3.
					-	O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	39	B6	[6]	I; PU	I/O	**SWDIO** — Serial wire debug input/output.
					-	I/O	**PIO0_15** — General purpose digital input/output pin.
					-	I	**AD4** — A/D converter, input 4.
					-	O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	26	40	A6	[6]	I; PU	I/O	**PIO0_16** — General purpose digital input/output pin.
					-	I	**AD5** — A/D converter, input 5.
					-	O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
					-	I	**WAKEUP** — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	45	A3	[3]	I; PU	I/O	**PIO0_17** — General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$** — Request To Send output for USART.
					-	I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK** — Serial clock input/output for USART in synchronous mode.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
PIO0_18/RXD/ CT32B0_MAT0	31	46	B3	[3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
					-	I	**RXD —** Receiver input for USART.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	47	B2	[3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
					-	O	**TXD —** Transmitter output for USART.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	9	F2	[3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	17	G4	[3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	30	E8	[6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
					-	I	**AD6 —** A/D converter, input 6.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7	27	42	A5	[6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
					-	I	**AD7 —** A/D converter, input 7.
PIO1_0/CT32B1_MAT0	-	-	-	[3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	-	-	-	[3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	-	-	-	[3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
PIO1_3/CT32B1_MAT3	-	-	-	[3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	-	-	-	[3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	-	-	H8	[3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO1_6	-	-	-	[3]	I; PU	I/O	**PIO1_6 —** General purpose digital input/output pin.
PIO1_7	-	-	-	[3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
PIO1_8	-	-	-	[3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
PIO1_9	-	-	-	[3]	I; PU	I/O	**PIO1_9 —** General purpose digital input/output pin.
PIO1_10	-	-	-	[3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	-	-	-	[3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_12	-	-	-	[3]	I; PU	I/O	**PIO1_12 —** General purpose digital input/output pin.
PIO1_13/$\overline{DTR}$/ CT16B0_MAT0/TXD	-	36	B8	[3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
					-	O	**$\overline{DTR}$ —** Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{DSR}$/ CT16B0_MAT1/RXD	-	37	A8	[3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
					-	I	**$\overline{DSR}$ —** Data Set Ready input for USART.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
PIO1_15/DCD/ CT16B0_MAT2/SCK1	28	43	A4	[3]	I; PU	I/O	**PIO1_15** — General purpose digital input/output pin.
						I	**DCD** — Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_16/RI/ CT16B0_CAP0	-	48	A2	[3]	I; PU	I/O	**PIO1_16** — General purpose digital input/output pin.
					-	I	**RI** — Ring Indicator input for USART.
					-	I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	[3]	I; PU	I/O	**PIO1_17** — General purpose digital input/output pin.
					-	I	**CT16B0_CAP1** — Capture input 1 for 16-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	[3]	I; PU	I/O	**PIO1_18** — General purpose digital input/output pin.
					-	I	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
					-	O	**TXD** — Transmitter output for USART.
PIO1_19/DTR/SSEL1	1	2	B1	[3]	I; PU	I/O	**PIO1_19** — General purpose digital input/output pin.
					-	O	**DTR** — Data Terminal Ready output for USART.
					-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_20/DSR/SCK1	-	13	H1	[3]	I; PU	I/O	**PIO1_20** — General purpose digital input/output pin.
					-	I	**DSR** — Data Set Ready input for USART.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_21/DCD/MISO1	-	26	G8	[3]	I; PU	I/O	**PIO1_21** — General purpose digital input/output pin.
					-	I	**DCD** — Data Carrier Detect input for USART.
					-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO1_22/RI/MOSI1	-	38	A7	[3]	I; PU	I/O	**PIO1_22** — General purpose digital input/output pin.
					-	I	**RI** — Ring Indicator input for USART.
					-	I/O	**MOSI1** — Master Out Slave In for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
PIO1_23/CT16B1_MAT1/ SSEL1	-	18	H4	[3]	I; PU	I/O	**PIO1_23** — General purpose digital input/output pin.
					-	O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	21	G6	[3]	I; PU	I/O	**PIO1_24** — General purpose digital input/output pin.
					-	O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	1	A1	[3]	I; PU	I/O	**PIO1_25** — General purpose digital input/output pin.
					-	O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	-	11	G2	[3]	I; PU	I/O	**PIO1_26** — General purpose digital input/output pin.
					-	O	**CT32B0_MAT2** — Match output 2 for 32-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	-	12	G1	[3]	I; PU	I/O	**PIO1_27** — General purpose digital input/output pin.
					-	O	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.
					-	O	**TXD** — Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	-	24	H7	[3]	I; PU	I/O	**PIO1_28** — General purpose digital input/output pin.
					-	I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK** — Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	31	D7	[3]	I; PU	I/O	**PIO1_29** — General purpose digital input/output pin.
					-	I/O	**SCK0** — Serial clock for SSP0.
					-	I	**CT32B0_CAP1** — Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O	**PIO1_31** — General purpose digital input/output pin.
USB_DM	13	19	G5	[7]	F	-	**USB_DM** — USB bidirectional D– line.
USB_DP	14	20	H5	[7]	F	-	**USB_DP** — USB bidirectional D+ line.
XTALIN	4	6	D1	[8][9]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin TFBGA48		Reset state [1]	Type	Description
XTALOUT	5	7	E1	[8][9]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	8; 44	B4, E2		-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	5; 41	B5, D2		-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 31 for the reset pad configuration. RESET functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 30).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 30); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 30); includes digital input glitch filter.

[7] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

[9] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

To select a port pin for a peripheral function from Table 4, program the FUNC bits in the port pin's IOCON register with this function. The user must ensure that the assignment of a function to a port pin is unambiguous. Only the debug functions for JTAG and SWD are selected by default in their corresponding IOCON registers. All other functions must be programmed in the IOCON block before they can be used. For details see the *LPC11U1x user manual*.

Table 4. Multiplexing of peripheral functions

Peripheral	Function	Type	Default	Available on ports			
USART	RXD	I	no	PIO0_18	PIO1_14	PIO1_17	PIO1_26
	TXD	O	no	PIO0_19	PIO1_13	PIO1_18	PIO1_27
	$\overline{CTS}$	I	no	PIO0_7	-	-	-
	$\overline{RTS}$	O	no	PIO0_17	-	-	-
	$\overline{DTR}$	O	no	PIO1_13	PIO1_19	-	-
	$\overline{DSR}$	I	no	PIO1_14	PIO1_20	-	-
	$\overline{DCD}$	I	no	PIO1_15	PIO1_21	-	-
	$\overline{RI}$	I	no	PIO1_16	PIO1_22	-	-
	SCLK	I/O	no	PIO0_17	PIO1_28	-	-

Table 4. Multiplexing of peripheral functions

Peripheral	Function	Type	Default	Available on ports			
SSP0	SCK0	I/O	no	PIO0_6	PIO0_10	PIO1_29	
	SSEL0	I/O	no	PIO0_2	-	-	-
	MISO0	I/O	no	PIO0_8	-	-	-
	MOSI0	I/O	no	PIO0_9	-	-	-
SSP1	SCK1	I/O	no	PIO1_15	PIO1_20	-	-
	SSEL1	I/O	no	PIO1_19	PIO1_23	-	-
	MISO1	I/O	no	PIO0_22	PIO1_21	-	-
	MOSI1	I/O	no	PIO0_21	PIO1_22	-	-
CT16B0	CT16B0_CAP0	I	no	PIO0_2	PIO1_16	-	-
	CT16B0_CAP1	I	no	PIO1_17	-	-	-
	CT16B0_MAT0	O	no	PIO0_8	PIO1_13	-	-
	CT16B0_MAT1	O	no	PIO0_9	PIO1_14	-	-
	CT16B0_MAT2	O	no	PIO0_10	PIO1_15	-	-
CT16B1	CT16B1_CAP0	I	no	PIO0_20	-	-	-
	CT16B1_CAP1	I	no	PIO1_18	-	-	-
	CT16B1_MAT0	O	no	PIO0_21	-	-	-
	CT16B1_MAT1	O	no	PIO0_22	PIO1_23	-	-
CT32B0	CT32B0_CAP0	I	no	PIO0_17	PIO1_28	-	-
	CT32B0_CAP1	I	no	PIO1_29	-	-	-
	CT32B0_MAT0	O	no	PIO0_18	PIO1_24	-	-
	CT32B0_MAT1	O	no	PIO0_19	PIO1_25	-	-
	CT32B0_MAT2	O	no	PIO0_1	PIO1_26	-	-
	CT32B0_MAT3	O	no	PIO0_11	PIO1_27	-	-
CT32B1	CT32B1_CAP0	I	no	PIO0_12	PIO1_4	-	-
	CT32B1_CAP1	I	no	PIO1_5	-	-	-
	CT32B1_MAT0	O	no	PIO0_13	PIO1_0	-	-
	CT32B1_MAT1	O	no	PIO0_14	PIO1_1	-	-
	CT32B1_MAT2	O	no	PIO0_15	PIO1_2	-	-
	CT32B1_MAT3	O	no	PIO0_16	PIO1_3	-	-
ADC	AD0	I	no	PIO0_11	-	-	-
	AD1	I	no	PIO0_12	-	-	-
	AD2	I	no	PIO0_13	-	-	-
	AD3	I	no	PIO0_14	-	-	-
	AD4	I	no	PIO0_15	-	-	-
	AD5	I	no	PIO0_16	-	-	-
	AD6	I	no	PIO0_22	-	-	-
	AD7	I	no	PIO0_23	-	-	-
USB	USB_VBUS	I	no	PIO0_3	-	-	-
	USB_FTOGGLE	O	no	PIO0_1	-	-	-
	$\overline{\text{USB\_CONNECT}}$	O	no	PIO0_6	-	-	-
CLKOUT	CLKOUT	O	no	PIO0_1	-	-	-

Table 4. Multiplexing of peripheral functions

Peripheral	Function	Type	Default	Available on ports			
JTAG	TDI	I	yes	PIO0_11	-	-	-
	TMS	I	yes	PIO0_12	-	-	-
	TDO	O	yes	PIO0_13	-	-	-
	$\overline{\text{TRST}}$	I	yes	PIO0_14	-	-	-
	TCK	I	yes	PIO0_10	-	-	-
SWD	SWCLK	I	yes	PIO0_10	-	-	-
	SWDIO	I/O	yes	PIO0_15	-	-	-

7. Functional description

7.1 Memory map

The LPC11U1x incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

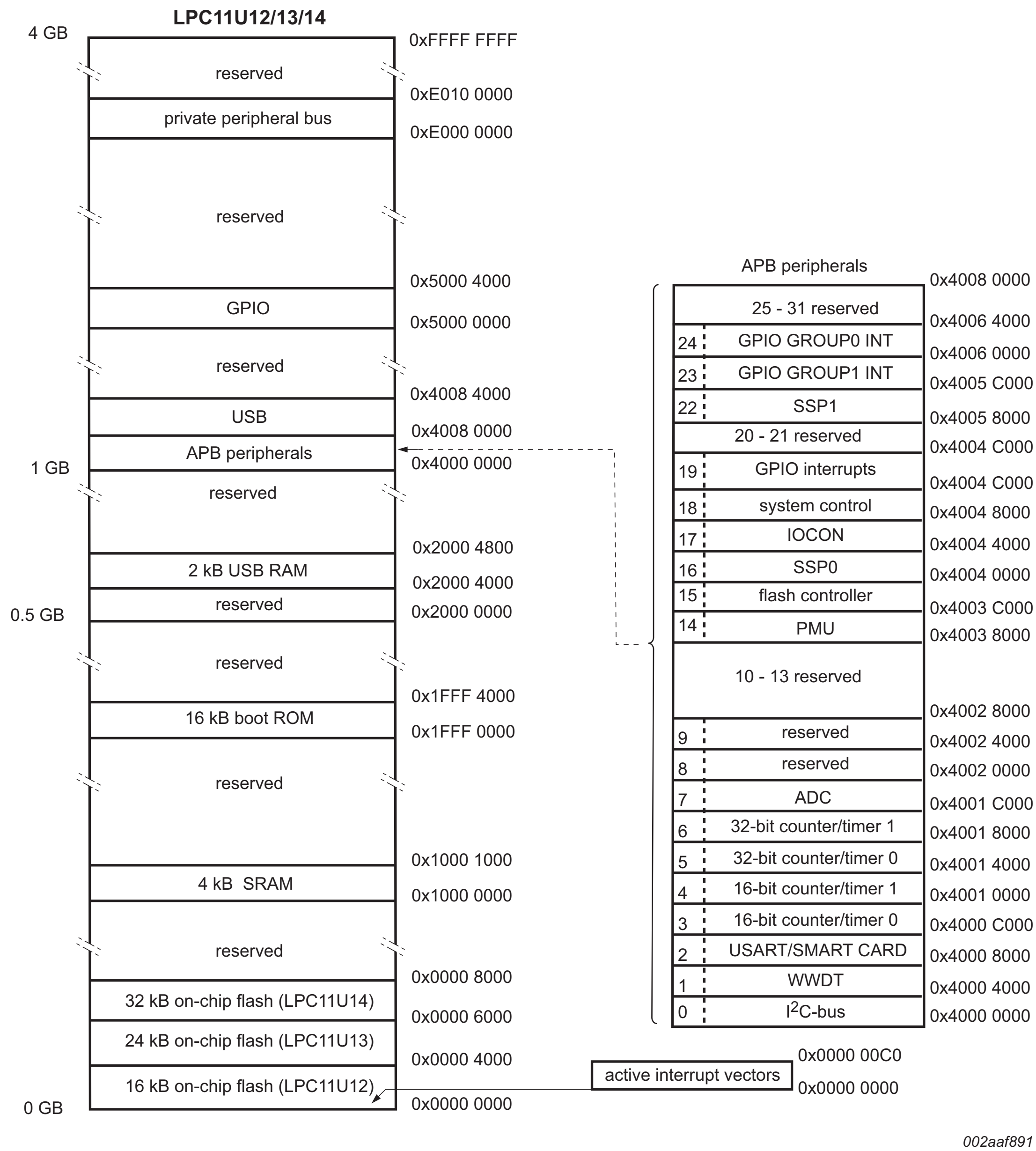


Fig 5. LPC11U1x memory map

7.2 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.2.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U1x, the NVIC supports 24 vectored interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.

- Software interrupt generation.

7.2.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.3 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.4 General Purpose Input/Output GPIO

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U1x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.4.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Port interrupts can be triggered by any pin or pins in each port.

7.5 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC11U1x USB interface is a device controller with on-chip PHY for device functions.

7.5.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

7.5.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 5 physical (10 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.

7.6 USART

The LPC11U1x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.6.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

7.7 SSP serial I/O controller

The SSP controllers are capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.7.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.8 I^2C-bus serial I/O controller

The LPC11U1x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.8.1 Features

- The I^2C-interface is an I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.9 10-bit ADC

The LPC11U1x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.9.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time ≥ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.10 General purpose external event counter/timers

The LPC11U1x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.10.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.11 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.12 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.12.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.13 Clocking and power control

7.13.1 Integrated oscillators

The LPC11U1x include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11U1x will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC11U1x clock generation.

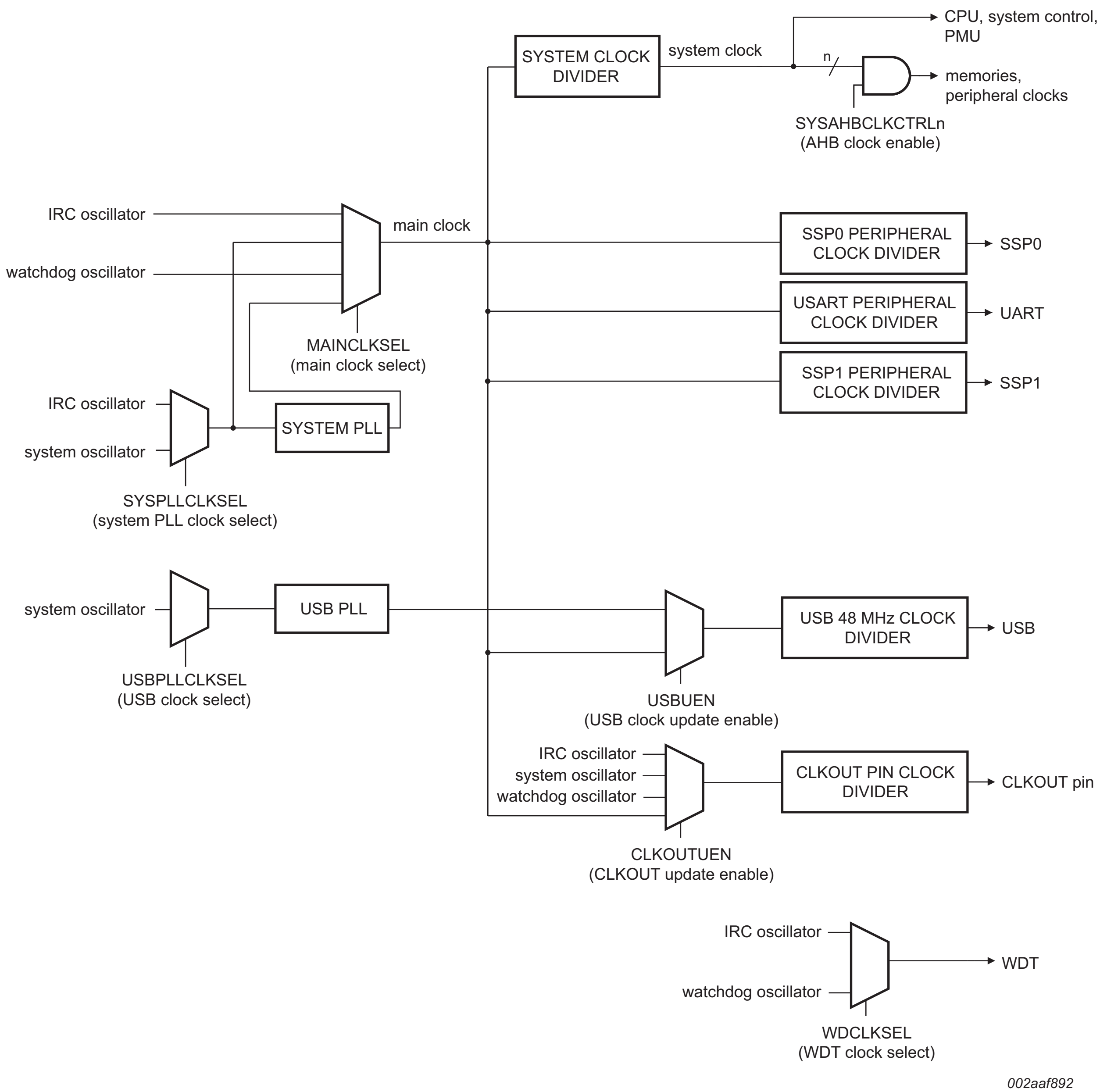


Fig 6. LPC11U1x clocking generation block diagram

7.13.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11U1x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.13.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U1x, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.13.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.13.2 System PLL and USB PLL

The LPC11U1x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.13.3 Clock output

The LPC11U1x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.13.4 Wake-up process

The LPC11U1x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.13.5 Power control

The LPC11U1x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.13.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U1x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.13.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.13.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11U1x is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11U1x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

7.13.5.4 Power-down mode

In Power-down mode, the LPC11U1x is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the user has the option to keep the BOD circuit running for BOD protection.

The LPC11U1x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.13.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC11U1x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11U1x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the user to always keep the watchdog timer or the BOD running.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.13.6 System control

7.13.6.1 Reset

Reset has four sources on the LPC11U1x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.13.6.2 Brownout detection

The LPC11U1x includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.13.6.3 Code security (Code Read Protection - CRP)

This feature of the LPC11U1x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC11U1x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC11U1x user manual*.

7.13.6.4 APB interface

The APB peripherals are located on one APB bus.

7.13.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

7.13.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.14 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11U1x is in reset.

Remark: Boundary scan operations should not be started until 250 μs after POR, and the test TAP should be reset after the boundary scan. Boundary scan is not affected by Code Read Protection.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	–0.5	+5.5	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	–6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash;					
		system clock = 12 MHz	[2][3][4] [5][6][7]	-	2	-	mA
		system clock = 50 MHz	[3][4][5] [6][7][8]	-	8	-	mA
		Sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; system clock = 12 MHz	[2][3][4] [5][6][7]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[3][6]	-	360	-	μA
		Power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	2	-	μA
		Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[9]	-	220	-	nA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[10][11] [12]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = –4 mA		V_{DD} – 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OH} = –3 mA		V_{DD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} – 0.4 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		–4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		–3	-	-	mA

Table 6. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		–15	–50	–85	µA
		1.8 V ≤ V_{DD} < 2.0 V		–10	–50	–85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[10][11][12]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = –20 mA		V_{DD} – 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = –12 mA		V_{DD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} – 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V		–15	–50	–85	µA
		1.8 V ≤ V_{DD} < 2.0 V		–10	–50	–85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I²C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins					mA
		2.0 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins					mA
		2.0 V ≤ V_{DD} ≤ 3.6 V		20	-	-	
		1.8 V ≤ V_{DD} < 2.0 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[14]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V		-	-	±10	µA
V_{BUS}	bus supply voltage			-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage	driven; for low-/full-speed; R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[15]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] IRC enabled; system oscillator disabled; system PLL disabled.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] BOD disabled.

[5] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the syscon block.

[6] USB_DP and USB_DM pulled LOW externally.

[7] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

[10] Including voltage on outputs in 3-state mode.

[11] V_{DD} supply voltage must be present.

[12] 3-state outputs go into 3-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] To V_{SS}.

[15] Includes external resistors of 33 $\Omega \pm 1$ % on USB_DP and USB_DM.

Table 7. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	±1.5	LSB
E_O	offset error	[4]	-	-	±3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

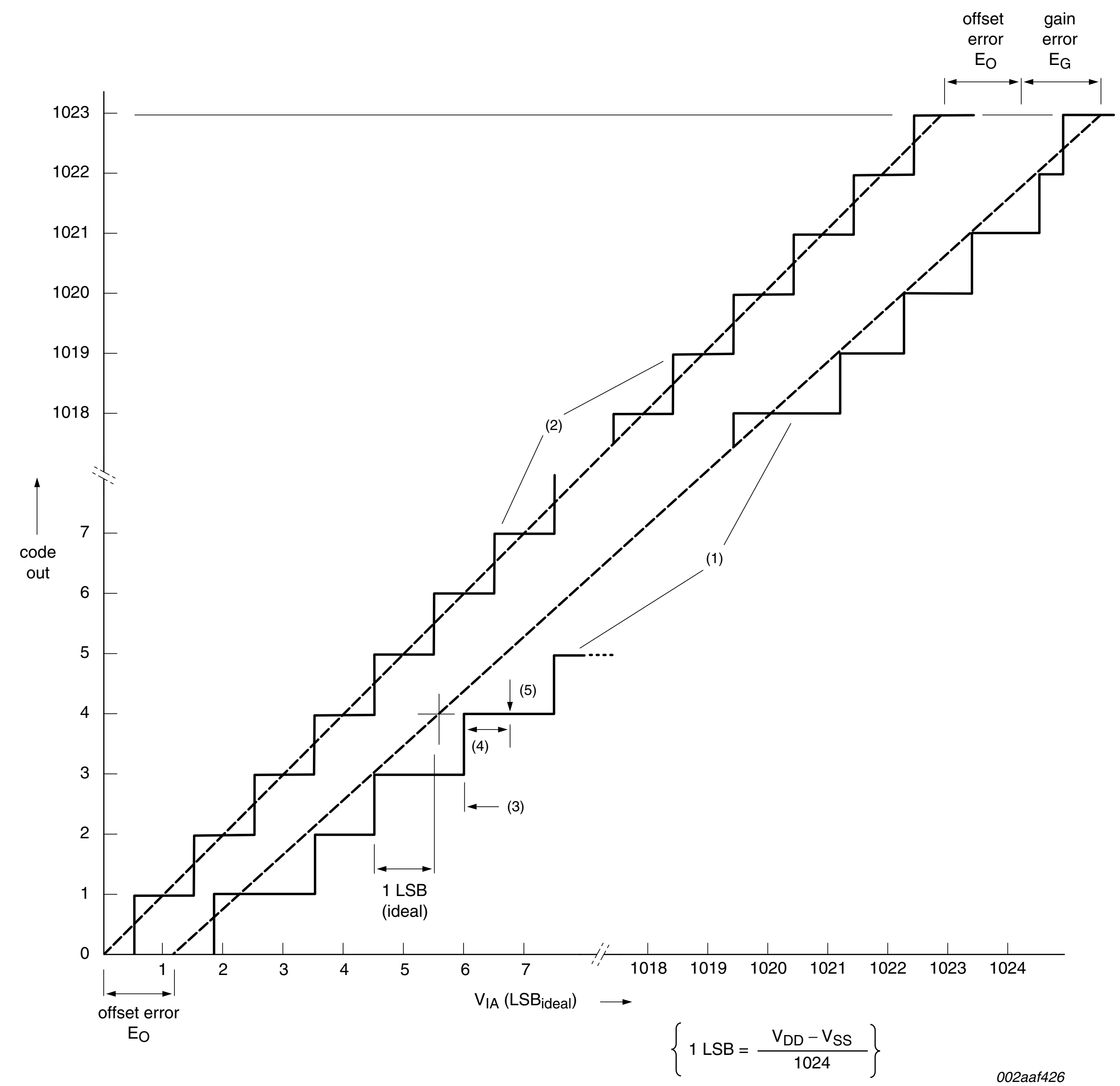
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 7.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 4.5 MHz and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

9.1 BOD static characteristics

Table 8. BOD static characteristics[1]

T_{amb} = 25 °C.

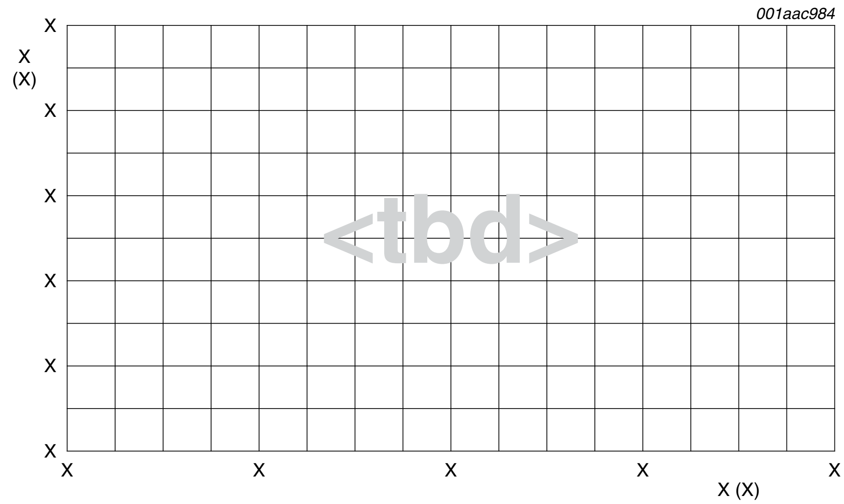
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC11U1x user manual*.

9.2 Power consumption

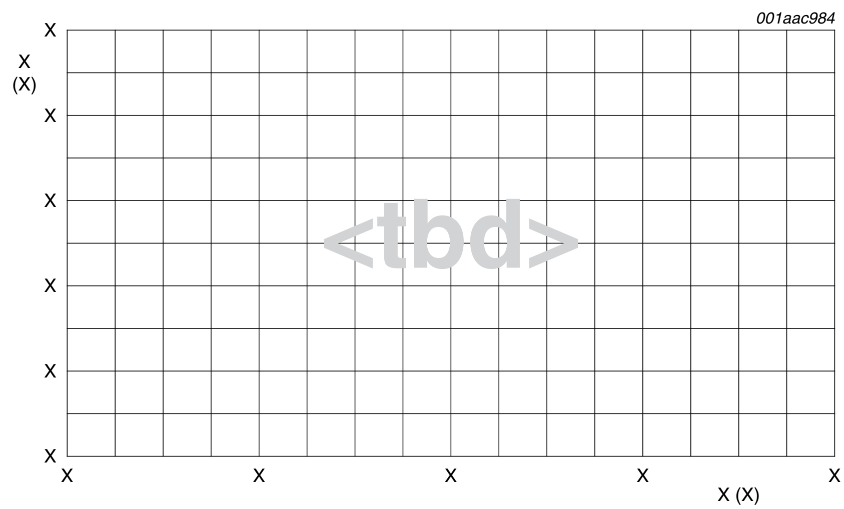
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC11U1x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



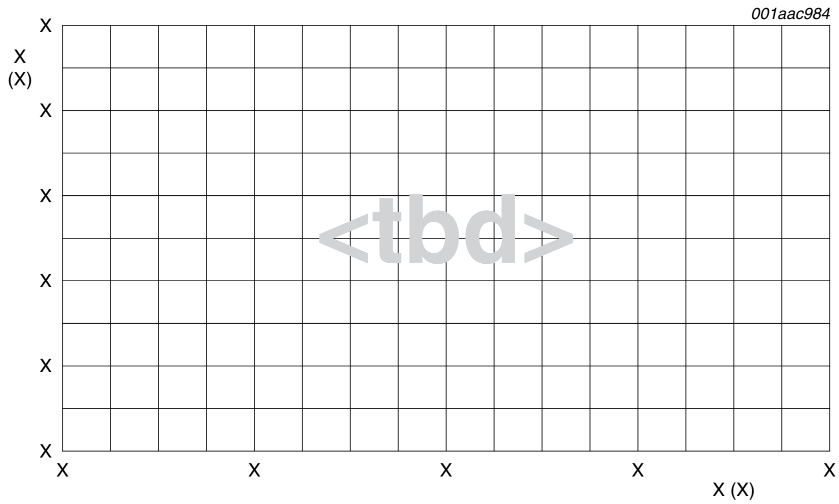
Conditions: T_{amb} = 25 °C; active mode entered executing code from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

Fig 8. Typical supply current versus regulator supply voltage V_{DD} in active mode



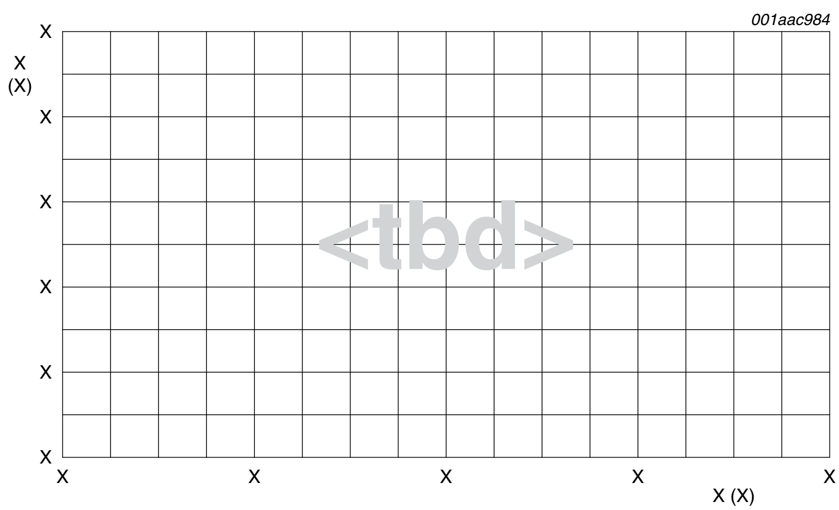
Conditions: V_{DD} = 3.3 V; Active mode entered executing code from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

Fig 9. Typical supply current versus temperature in Active mode



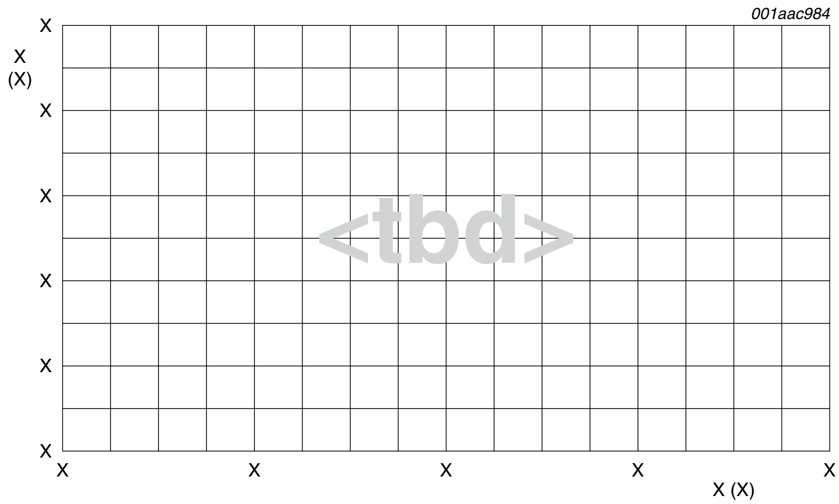
Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally.

Fig 10. Typical supply current versus temperature in Sleep mode



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = <tbd>; USB_DP and USB_DM pulled LOW externally.

Fig 11. Typical supply current versus temperature in Deep-sleep mode



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = <tbd>; USB_DP and USB_DM pulled LOW externally.

Fig 12. Typical supply current versus temperature in Power-down mode

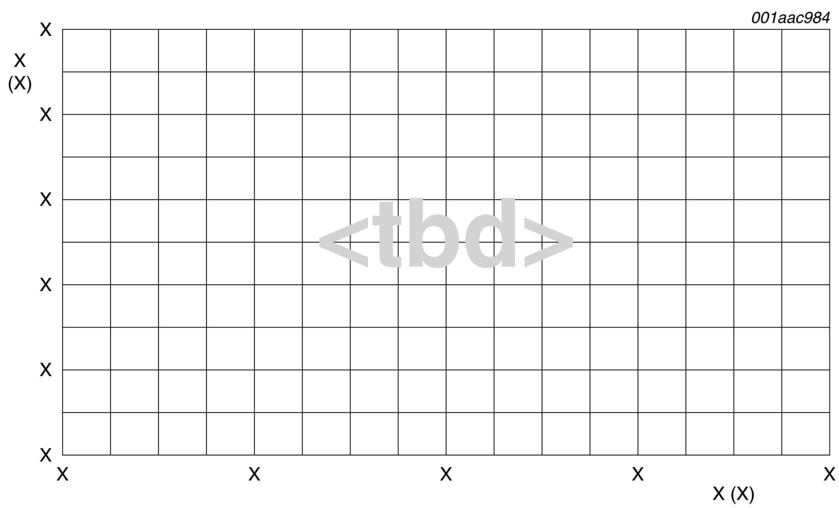


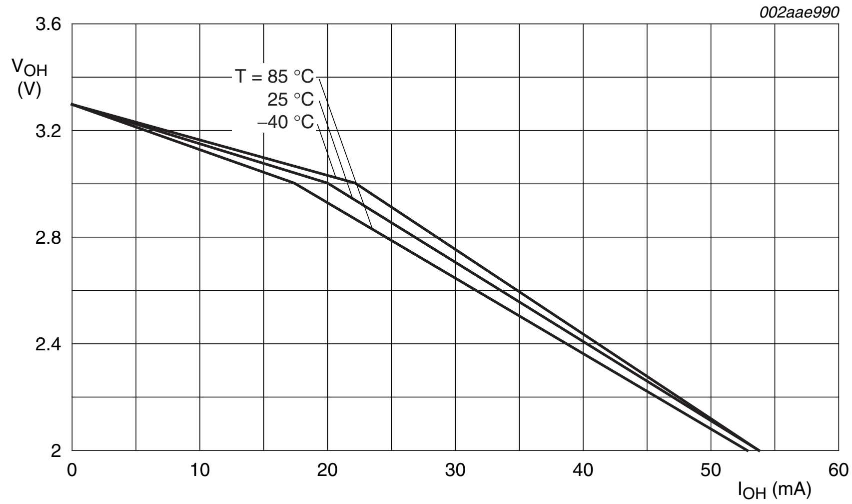
Fig 13. Typical supply current versus temperature in Deep power-down mode

Table 9. Power consumption for individual analog and digital blocks

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCTRL or PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

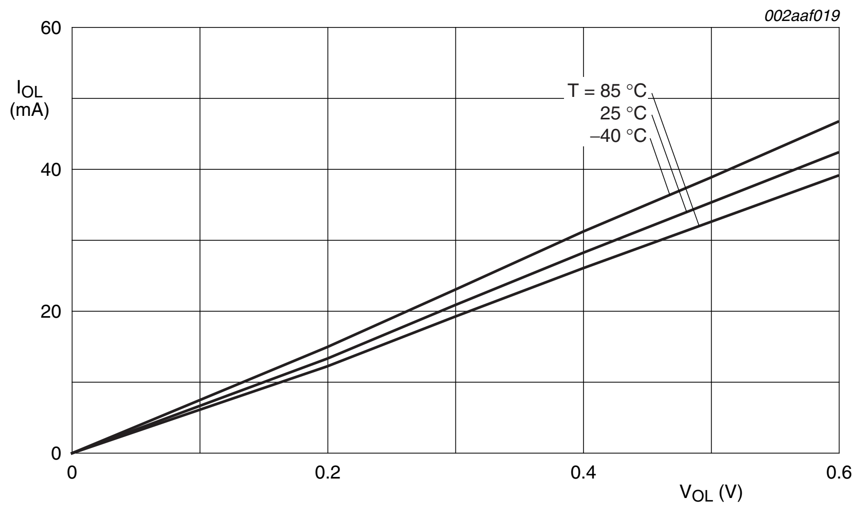
	Typical supply current per peripheral in mA for different system clock frequencies				Notes
	n/a	12 MHz	<tbd> MHz	<tbd> MHz	
IRC	<tbd>	-	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	<tbd>	-	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	<tbd>	-	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	<tbd>	-	-	-	Independent of main clock frequency.
Main PLL	-	<tbd>	-	-	
USB PLL	-	<tbd>	<tbd>	<tbd>	
ADC	-	<tbd>	<tbd>	<tbd>	
CLKOUT	-	<tbd>	<tbd>	<tbd>	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	<tbd>	<tbd>	<tbd>	
CT16B1	-	<tbd>	<tbd>	<tbd>	
CT32B0	-	<tbd>	<tbd>	<tbd>	
CT32B1	-	<tbd>	<tbd>	<tbd>	
GPIO	-	<tbd>	<tbd>	<tbd>	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	<tbd>	<tbd>	<tbd>	
I2C	-	<tbd>	<tbd>	<tbd>	
ROM	-	<tbd>	<tbd>	<tbd>	
SSP0	-	<tbd>	<tbd>	<tbd>	
SSP1	-	<tbd>	<tbd>	<tbd>	
USART	-	<tbd>	<tbd>	<tbd>	
WDT	-	<tbd>	<tbd>	<tbd>	Main clock selected as clock source for the WDT.
USB	-	-	<tbd>	-	Main clock selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.
USB	-	<tbd>	<tbd>	<tbd>	Dedicated USB PLL selected as cock source for the USB. USB_DP and USB_DM pulled LOW externally.

9.3 Electrical pin characteristics



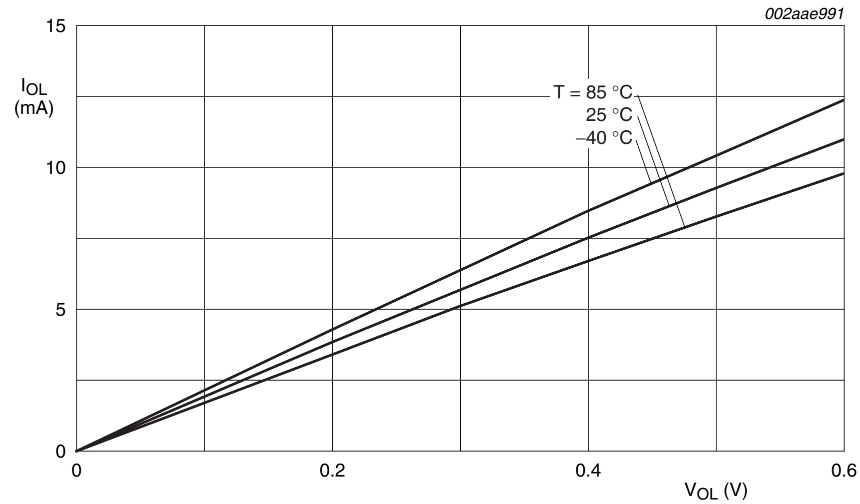
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 14. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



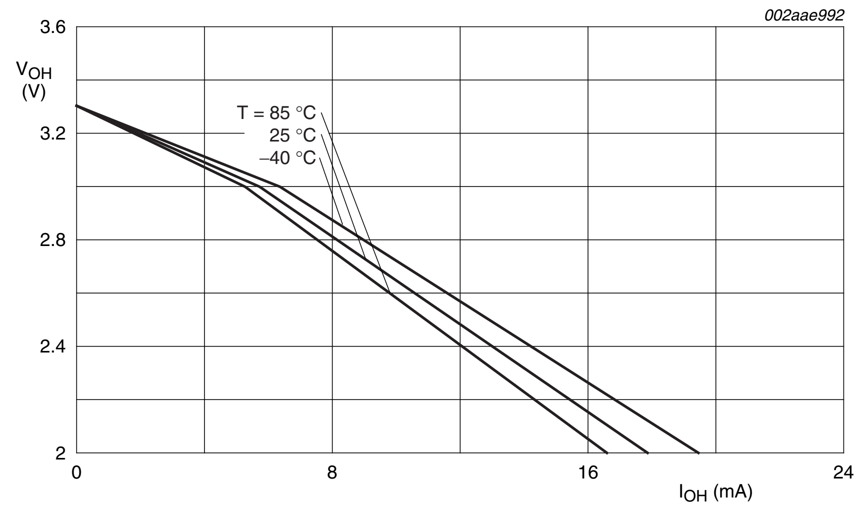
Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 15. I²C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



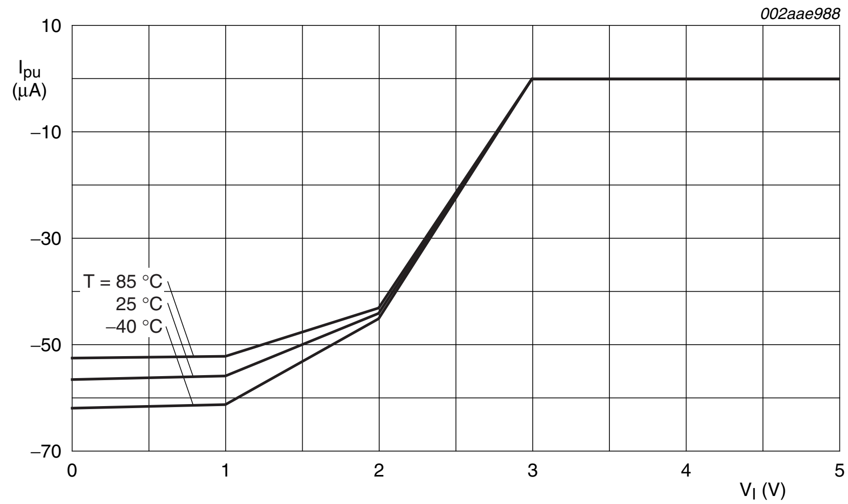
Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 16. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



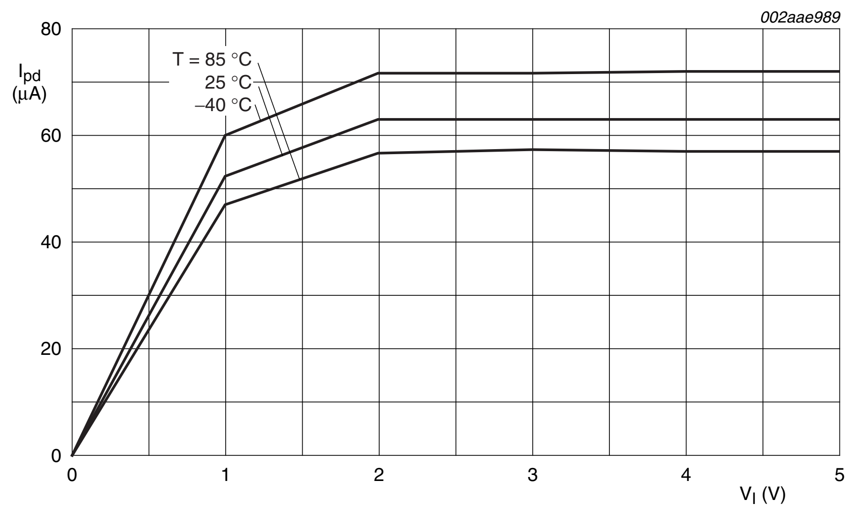
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 17. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 18. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Flash memory

Table 10. Flash characteristics
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 11. Dynamic characteristic: external clock
T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

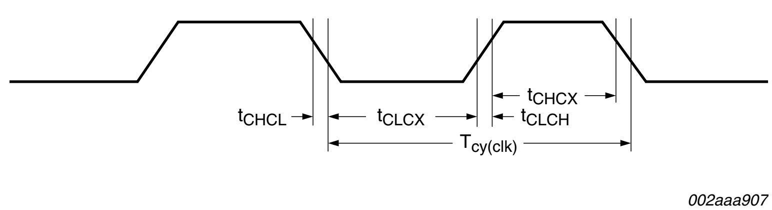


Fig 20. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.3 Internal oscillators

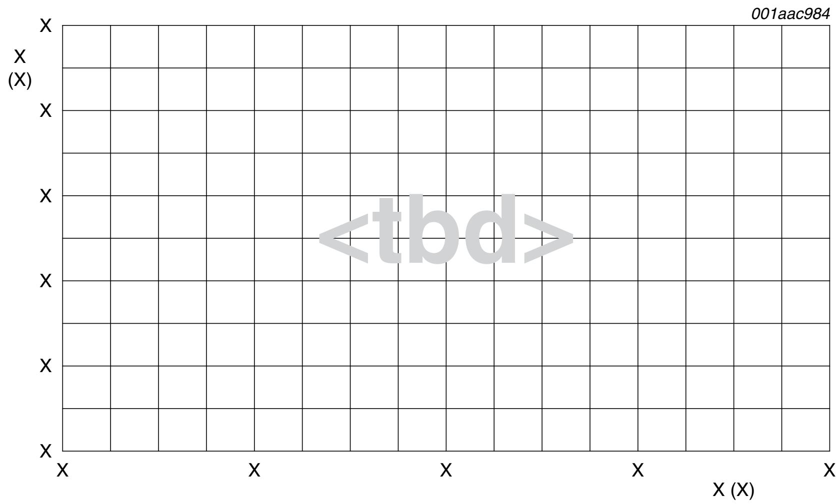
Table 12. Dynamic characteristics: IRC

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]*.*

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	<tbd>	12	<tbd>	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± <tbd> % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± <tbd> % accuracy specification for voltages below 2.7 V.

Fig 21. Internal RC oscillator frequency versus temperature

Table 13. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11U1x user manual.*

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{RESET}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

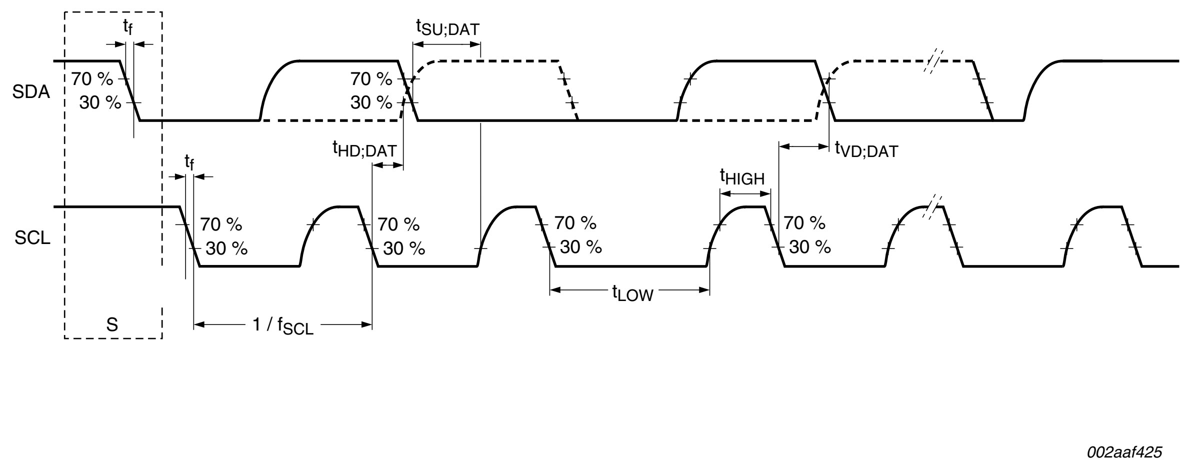


Fig 22. I²C-bus pins clock timing

10.6 SSP interface

Table 16. Dynamic characteristics: SSP pins in SPI mode

Symbol	Parameter	Conditions		Min	Max	Unit
SSP master						
$T_{cy(clk)}$	clock cycle time	when only receiving	[1]	<tbd>	-	ns
		when only transmitting	[1]	<tbd>	-	ns
t_{DS}	data set-up time	in SPI mode; $2.4\ V \leq V_{DD} \leq 3.6\ V$	[2]	<tbd>	-	ns
		$2.0\ V \leq V_{DD} < 2.4\ V$	[2]	<tbd>	-	ns
t_{DH}	data hold time	in SPI mode	[2]	<tbd>	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	<tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	<tbd>	-	ns
SSP slave						
$T_{cy(PCLK)}$	PCLK cycle time			<tbd>	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	<tbd>	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	<tbd> × $T_{cy(PCLK)}$ + <tbd>	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{amb} = -40$ °C to 85 °C.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25$ °C; $V_{DD} = 3.3$ V.

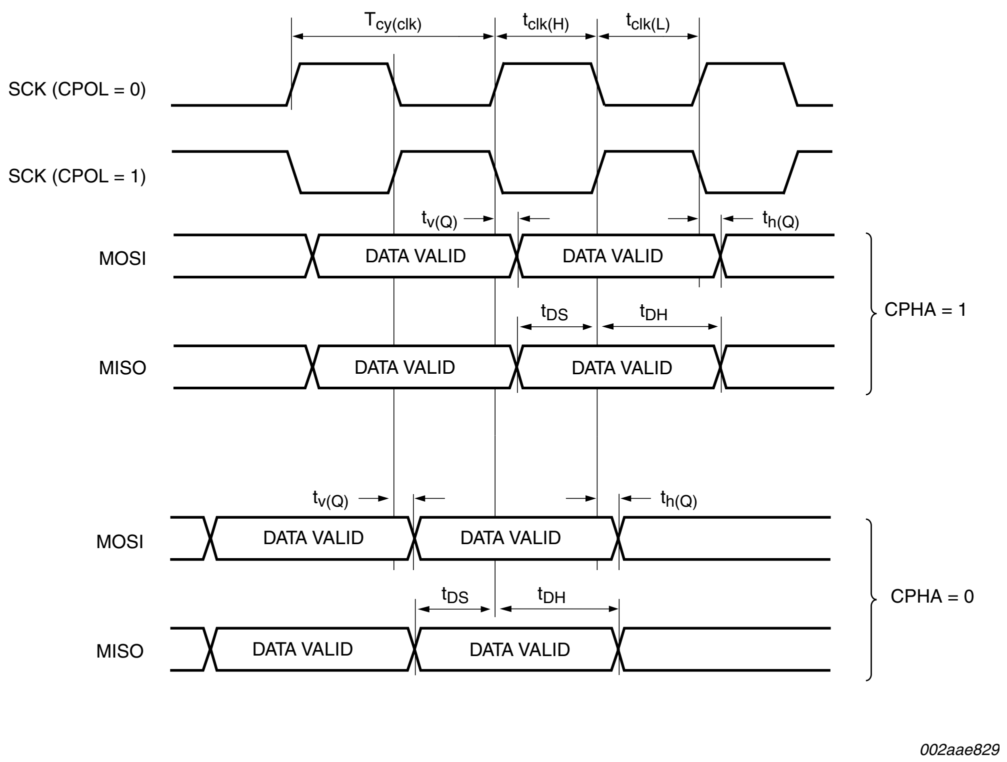


Fig 23. SSP master timing in SPI mode

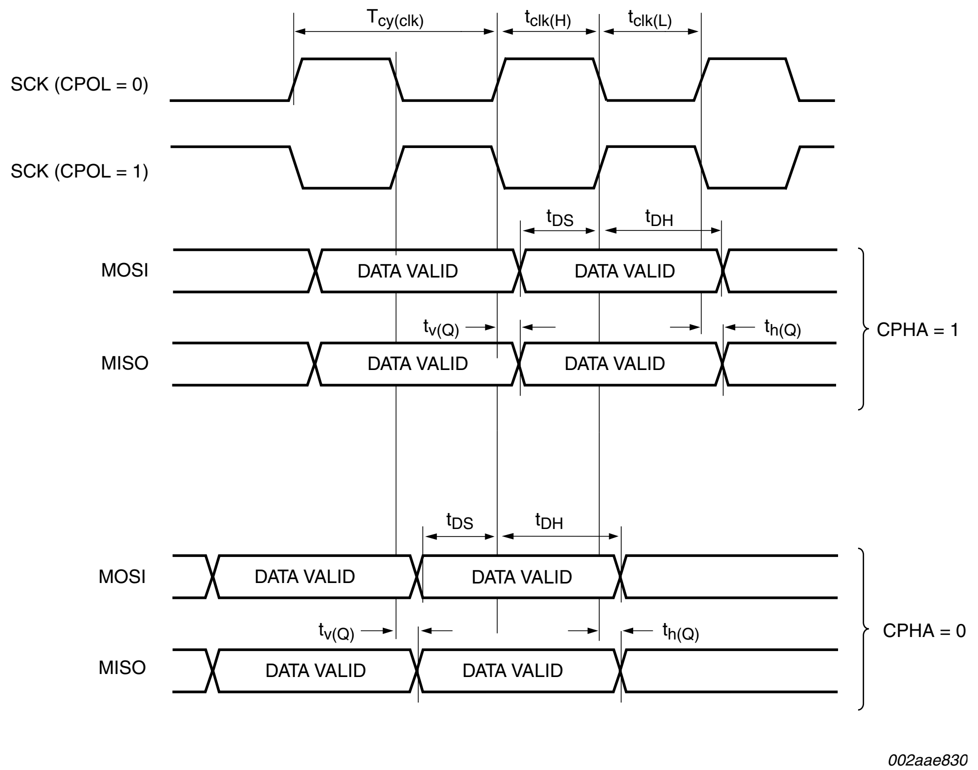


Fig 24. SSP slave timing in SPI mode

10.7 USB interface

Table 17. Dynamic characteristics: USB pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	<tbd>	-	<tbd>	ns
t_f	fall time	10 % to 90 %	<tbd>	-	<tbd>	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	<tbd>	%
V_{CRS}	output signal crossover voltage		<tbd>	-	<tbd>	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 25	<tbd>	-	<tbd>	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 25	<tbd>	-	<tbd>	ns
t_{JR1}	receiver jitter to next transition		<tbd>	-	<tbd>	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	<tbd>	-	<tbd>	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 25 [1]	<tbd>	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 25 [1]	<tbd>	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

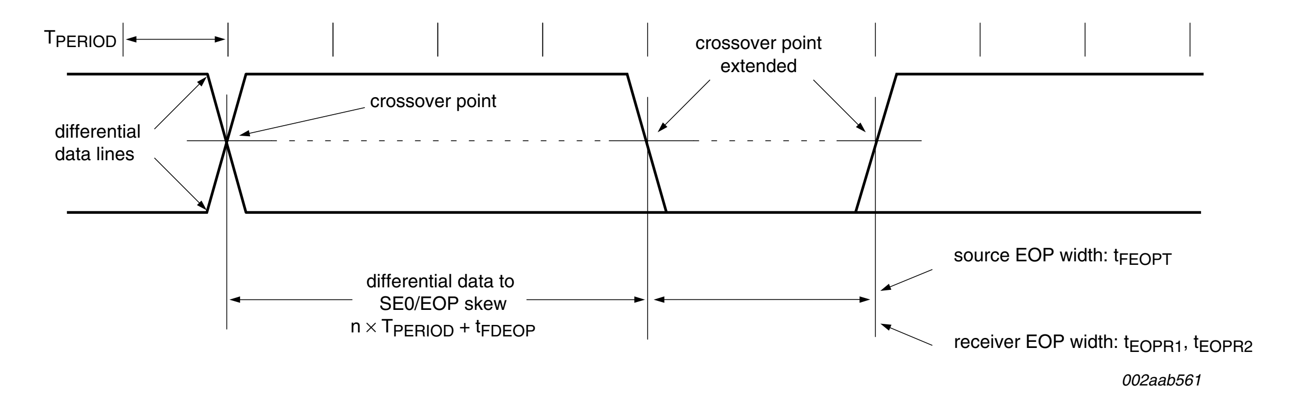


Fig 25. Differential data-to-EOP transition skew and EOP width

11. Application information

11.1 Suggested USB interface solutions

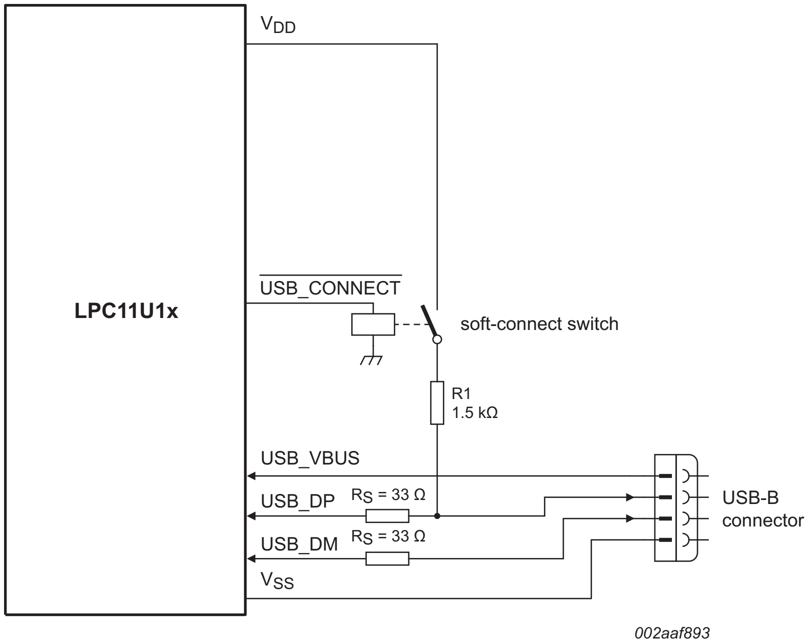


Fig 26. USB interface on a self-powered device

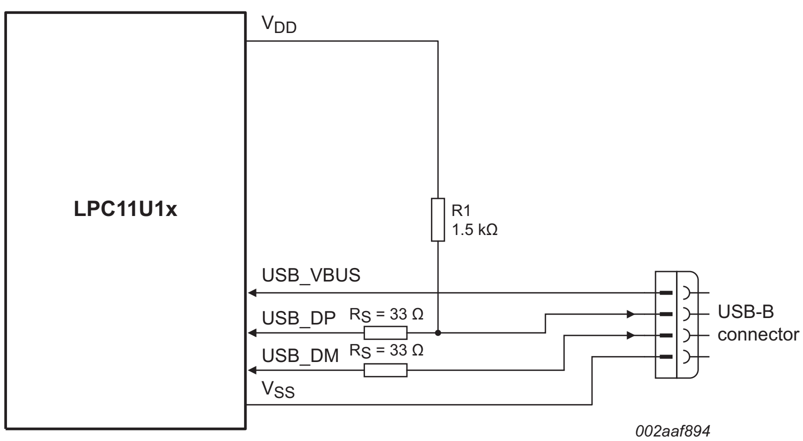


Fig 27. USB interface on a bus-powered device

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

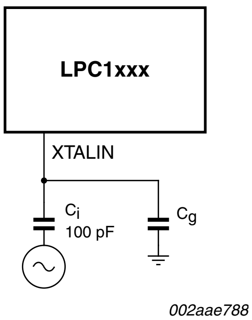


Fig 28. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 28), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 29 and in Table 18 and Table 19. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 29 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

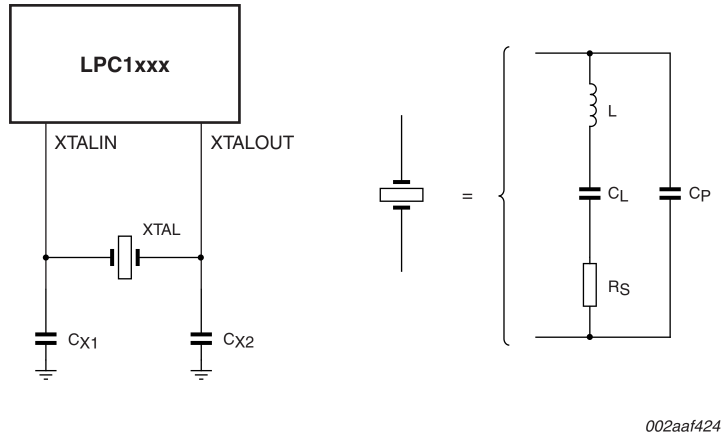


Fig 29. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

11.4 Standard I/O pad configuration

Figure 30 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

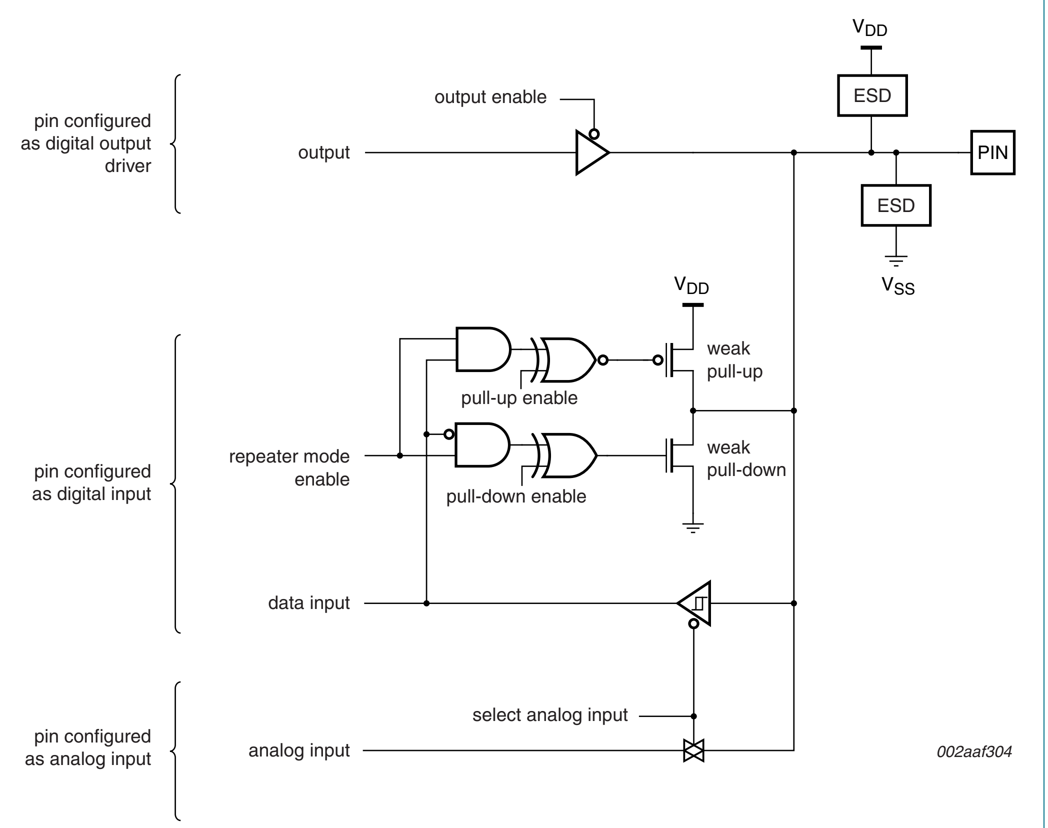


Fig 30. Standard I/O pad configuration

11.5 Reset pad configuration

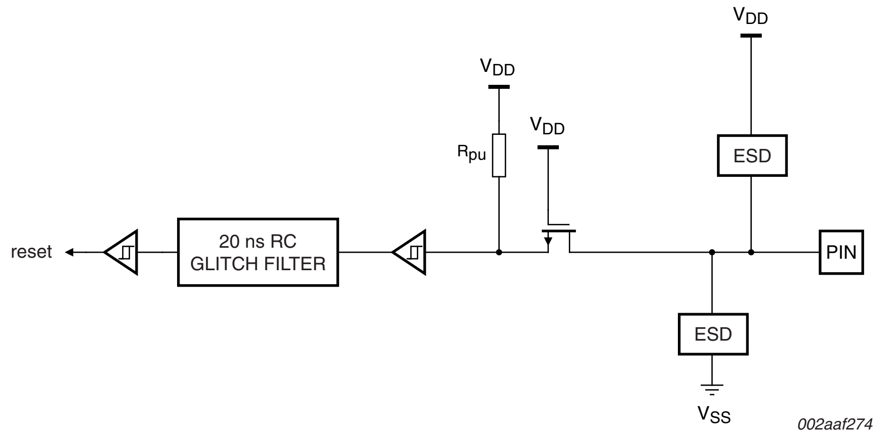


Fig 31. Reset pad configuration

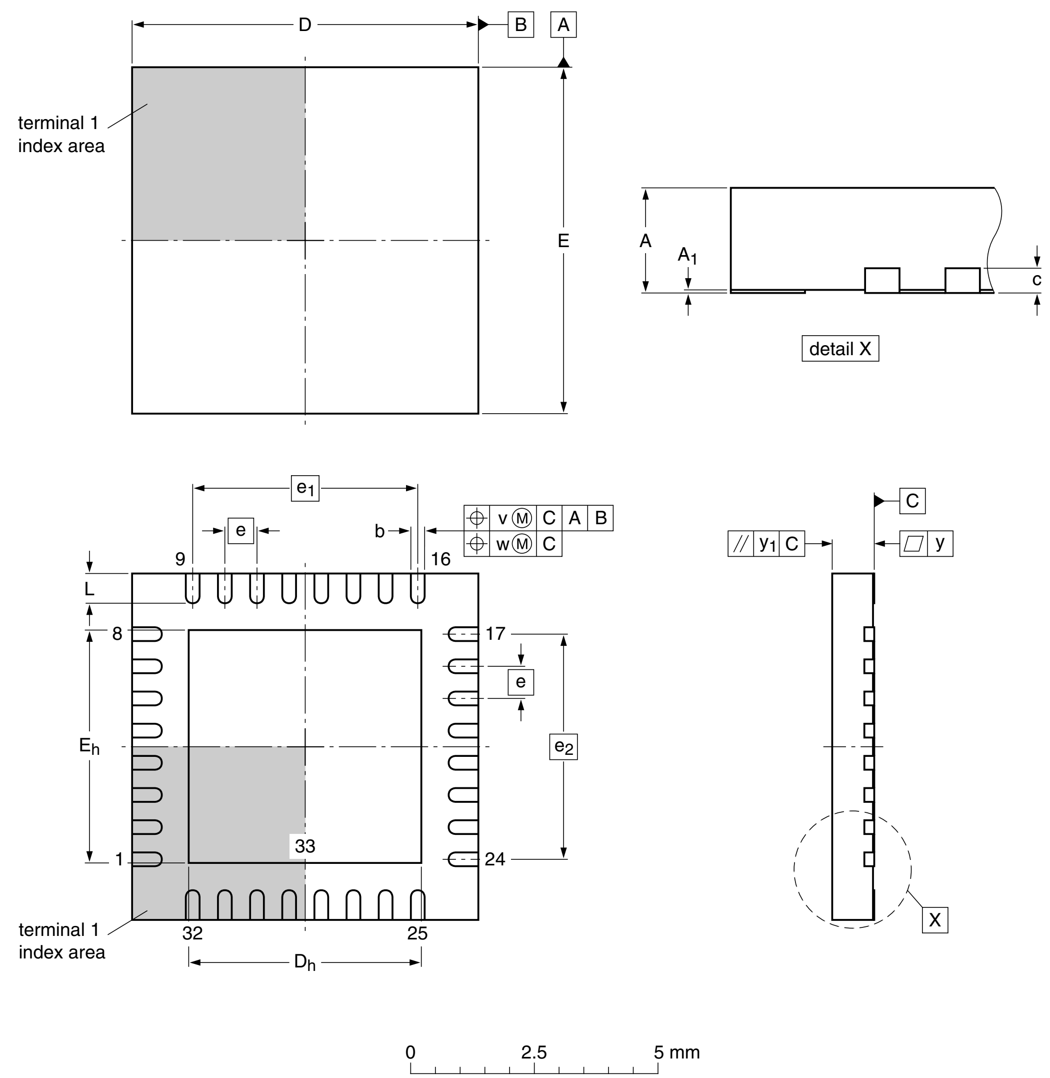
11.6 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 7:

- The ADC input trace must be short and as close as possible to the LPC11U1x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

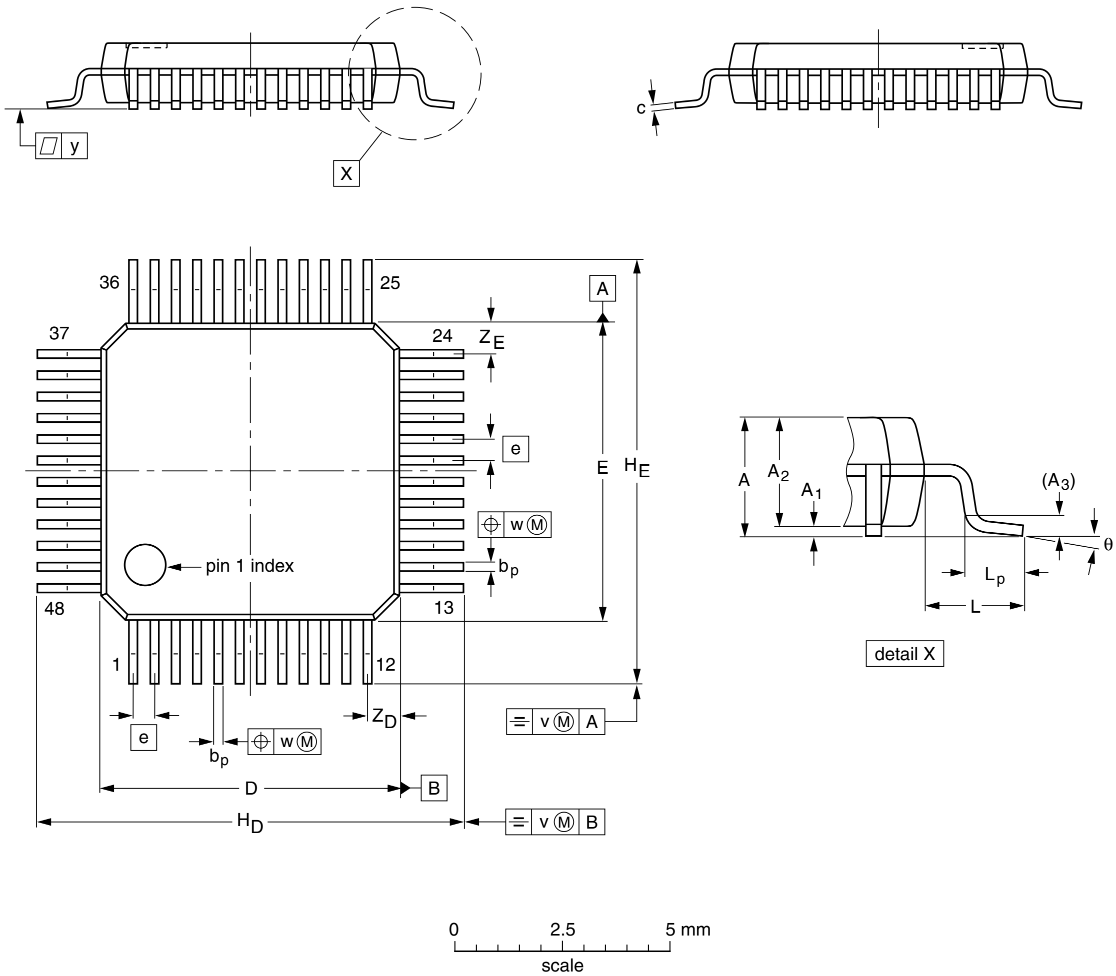
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
			- - -			~~09-03-17~~ 09-03-23

Fig 32. Package outline HVQFN33

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

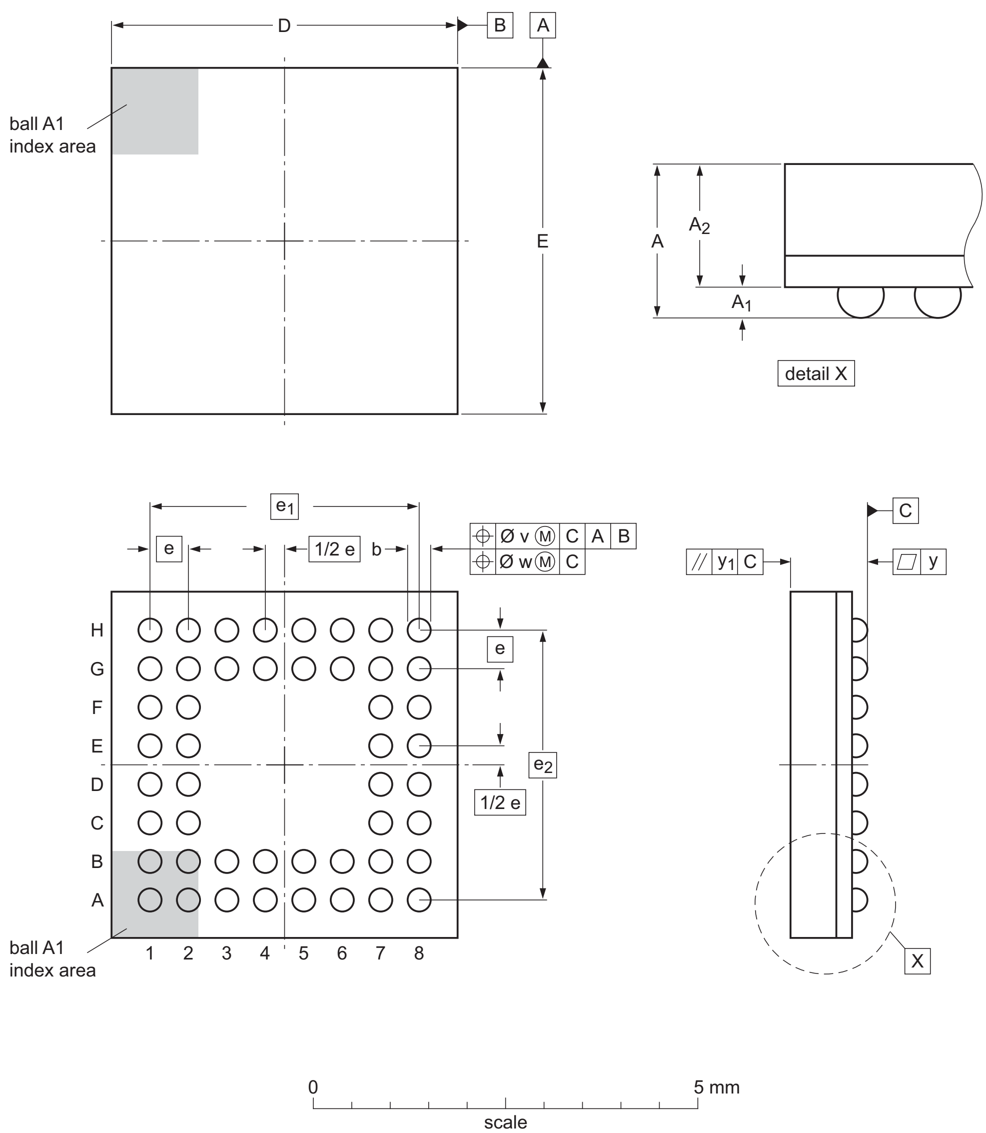
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 33. Package outline LQFP48 (SOT313-2)

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.7 mm **SOT1155-2**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.10	0.30	0.80	0.35	4.6	4.6							
	nom	0.95	0.25	0.70	0.30	4.5	4.5	0.5	3.5	3.5	0.15	0.05	0.08	0.1
	min	0.85	0.20	0.65	0.25	4.4	4.4							

sot1155-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1155-2		- - -				~~11-01-18~~ 11-03-01

Fig 34. Package outline TFBGA48 (SOT1155-2)

All information provided in this document is subject to legal disclaimers.

13. Abbreviations

Table 20. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
JTAG	Joint Action Test Group
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TAP	Test Access Port
USART	Universal Synchronous Asynchronous Receiver/Transmitter

14. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U1X v.1	20110411	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

Date of release: 11 April 2011
Document identifier: LPC11U1X