

DDR SDRAM RDIMM

MT36VDDF12872 – 1GB

MT36VDDF25672 – 2GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 184-pin, registered dual in-line memory module (RDIMM)
- Tall- and standard-height PCB options
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 1GB (128 Meg x 72) and 2GB (256 Meg x 72)
- Supports ECC error detection and correction
- VDD = VDDQ = +2.5V
(-40B VDD = VDDQ = +2.6V)
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) 2n-prefetch architecture
- Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Dual rank
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts

184-Pin RDIMM Figures

Figure 1: Tall-Height Layout – 1GB, 2GB (MO-206-EA)

PCB height: 43.18mm (1.7in)

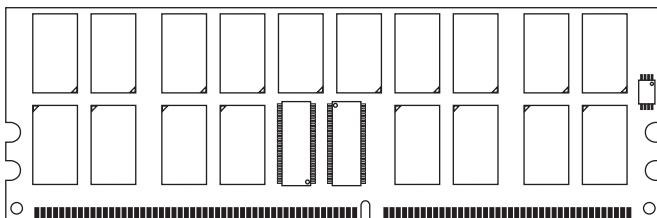


Figure 2: Standard-Height Layout – 1GB (MO-206-CA R/C D)

PCB height: 30.48mm (1.2in)

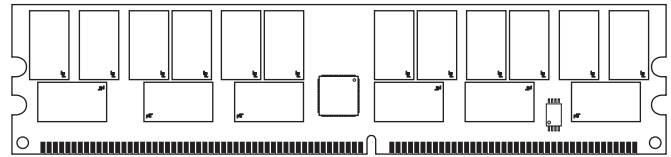
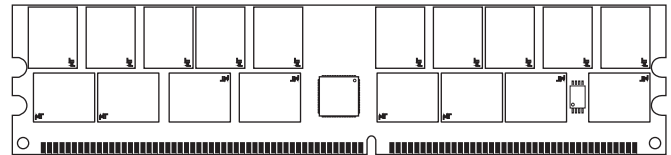


Figure 3: Standard-Height Layout – 2GB (MO-206-CA R/C D)

PCB height: 30.48mm (1.2in)



Options

- Operating temperature¹
 - Commercial (0°C ≤ T_A ≤ +70°C) None
 - Industrial (-40°C ≤ T_A ≤ +85°C) I
- Package
 - 184-pin DIMM (standard) G
 - 184-pin DIMM (Pb-free) Y
- Memory clock, speed, CAS latency²
 - 5.0ns (200 MHz), 400 MT/s, CL = 3 -40B
 - 6.0ns (166 MHz), 333 MT/s, CL = 2.5 -335
 - 7.5ns (133 MHz), 266 MT/s, CL = 2 -262
 - 7.5ns (133 MHz), 266 MT/s, CL = 2 -26A
 - 7.5ns (133 MHz), 266 MT/s, CL = 2.5 -265

Marking

Notes: 1. Contact Micron for industrial temperature module offerings.

2. CL = CAS (READ) latency; registered mode adds one clock cycle to CL.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | ^t RCD (ns) | ^t RP (ns) | ^t RC (ns) | Notes |
|-------------|-----------------------|------------------|----------|--------|-----------------------|----------------------|----------------------|-------|
| | | CL = 3 | CL = 2.5 | CL = 2 | | | | |
| -40B | PC3200 | 400 | 333 | 266 | 15 | 15 | 55 | |
| -335 | PC2700 | - | 333 | 266 | 18 | 18 | 60 | 1 |
| -262 | PC2100 | - | 266 | 266 | 15 | 15 | 60 | |
| -26A | PC2100 | - | 266 | 266 | 20 | 20 | 65 | |
| -265 | PC2100 | - | 266 | 200 | 20 | 20 | 65 | |

Notes: 1. The values of ^tRCD and ^tRP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

| Parameter | 1GB | 2GB |
|----------------------|--------------------|----------------------|
| Refresh count | 8K | 8K |
| Row address | 8K (A0–A12) | 8K (A0–A12) |
| Device bank address | 4 (BA0, BA1) | 4 (BA0, BA1) |
| Device configuration | 256Mb (64 Meg x 4) | 512Mb (128 Meg x 4) |
| Column address | 2K (A0–A9, A11) | 4K (A0–A9, A11, A12) |
| Module rank address | 2 (S0#, S1#) | 2 (S0#, S1#) |

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT46V64M4,¹ 256Mb DDR SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|-------------------------|--|
| MT36VDDF12872G-40B__ | 1GB | 128 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT36VDDF12872Y-40B__ | 1GB | 128 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT36VDDF12872G-335__ | 1GB | 128 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |
| MT36VDDF12872Y-335__ | 1GB | 128 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |
| MT36VDDF12872G-262__ | 1GB | 128 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT36VDDF12872G-26A__ | 1GB | 128 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT36VDDF12872Y-26A__ | 1GB | 128 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT36VDDF12872G-265__ | 1GB | 128 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |
| MT36VDDF12872Y-265__ | 1GB | 128 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

Notes: 1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
 Example: MT36VDDF12872Y-335G3.

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT46V128M4,¹ 512Mb DDR SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT36VDDF25672G-40B__ | 2GB | 256 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT36VDDF25672Y-40B__ | 2GB | 256 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT36VDDF25672G-335__ | 2GB | 256 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |
| MT36VDDF25672Y-335__ | 2GB | 256 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |
| MT36VDDF25672G-262__ | 2GB | 256 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT36VDDF25672G-26A__ | 2GB | 256 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT36VDDF25672G-265__ | 2GB | 256 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |
| MT36VDDF25672Y-265__ | 2GB | 256 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT36VDDF12872Y-335G3.

Pin Assignments and Descriptions

Table 5: Pin Assignments

| 184-Pin DDR RDIMM Front | | | | | | | | 184-Pin DDR RDIMM Back | | | | | | | |
|-------------------------|--------|-----|--------|-----|--------|-----|--------|------------------------|--------|-----|--------|-----|--------|-----|--------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | | |
| 1 | VREF | 24 | DQ17 | 47 | DQS8 | 70 | VDD | 93 | Vss | 116 | Vss | 139 | Vss | 162 | DQ47 |
| 2 | DQ0 | 25 | DQS2 | 48 | A0 | 71 | NC | 94 | DQ4 | 117 | DQ21 | 140 | DQS17 | 163 | NC |
| 3 | Vss | 26 | Vss | 49 | CB2 | 72 | DQ48 | 95 | DQ5 | 118 | A11 | 141 | A10 | 164 | VDDQ |
| 4 | DQ1 | 27 | A9 | 50 | Vss | 73 | DQ49 | 96 | VDDQ | 119 | DQS11 | 142 | CB6 | 165 | DQ52 |
| 5 | DQS0 | 28 | DQ18 | 51 | CB3 | 74 | Vss | 97 | DQS9 | 120 | VDD | 143 | VDDQ | 166 | DQ53 |
| 6 | DQ2 | 29 | A7 | 52 | BA1 | 75 | NC | 98 | DQ6 | 121 | DQ22 | 144 | CB7 | 167 | NC |
| 7 | VDD | 30 | VDDQ | 53 | DQ32 | 76 | NC | 99 | DQ7 | 122 | A8 | 145 | Vss | 168 | VDD |
| 8 | DQ3 | 31 | DQ19 | 54 | VDDQ | 77 | VDDQ | 100 | Vss | 123 | DQ23 | 146 | DQ36 | 169 | DQS15 |
| 9 | NC | 32 | A5 | 55 | DQ33 | 78 | DQS6 | 101 | NC | 124 | Vss | 147 | DQ37 | 170 | DQ54 |
| 10 | RESET# | 33 | DQ24 | 56 | DQS4 | 79 | DQ50 | 102 | NC | 125 | A6 | 148 | VDD | 171 | DQ55 |
| 11 | Vss | 34 | Vss | 57 | DQ34 | 80 | DQ51 | 103 | NC | 126 | DQ28 | 149 | DQS13 | 172 | VDDQ |
| 12 | DQ8 | 35 | DQ25 | 58 | Vss | 81 | Vss | 104 | VDDQ | 127 | DQ29 | 150 | DQ38 | 173 | NC |
| 13 | DQ9 | 36 | DQS3 | 59 | BA0 | 82 | NC | 105 | DQ12 | 128 | VDDQ | 151 | DQ39 | 174 | DQ60 |
| 14 | DQS1 | 37 | A4 | 60 | DQ35 | 83 | DQ56 | 106 | DQ13 | 129 | DQS12 | 152 | Vss | 175 | DQ61 |
| 15 | VDDQ | 38 | VDD | 61 | DQ40 | 84 | DQ57 | 107 | DQS10 | 130 | A3 | 153 | DQ44 | 176 | Vss |
| 16 | NC | 39 | DQ26 | 62 | VDDQ | 85 | VDD | 108 | VDD | 131 | DQ30 | 154 | RAS# | 177 | DQS16 |
| 17 | NC | 40 | DQ27 | 63 | WE# | 86 | DQS7 | 109 | DQ14 | 132 | Vss | 155 | DQ45 | 178 | DQ62 |
| 18 | Vss | 41 | A2 | 64 | DQ41 | 87 | DQ58 | 110 | DQ15 | 133 | DQ31 | 156 | VDDQ | 179 | DQ63 |
| 19 | DQ10 | 42 | Vss | 65 | CAS# | 88 | DQ59 | 111 | CKE1 | 134 | CB4 | 157 | S0# | 180 | VDDQ |
| 20 | DQ11 | 43 | A1 | 66 | Vss | 89 | Vss | 112 | VDDQ | 135 | CB5 | 158 | S1# | 181 | SA0 |
| 21 | CKE0 | 44 | CB0 | 67 | DQS5 | 90 | NC | 113 | NC | 136 | VDDQ | 159 | DQS14 | 182 | SA1 |
| 22 | VDDQ | 45 | CB1 | 68 | DQ42 | 91 | SDA | 114 | DQ20 | 137 | CK0 | 160 | Vss | 183 | SA2 |
| 23 | DQ16 | 46 | VDD | 69 | DQ43 | 92 | SCL | 115 | A12 | 138 | CK0# | 161 | DQ46 | 184 | VDDSPD |

Table 6: Pin Descriptions

| Symbol | Type | Description |
|-----------------|--------|---|
| A0–A12 | Input | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| BA0, BA1 | Input | Bank address: BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| CK0, CK0# | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#. |
| CKE0, CEK1 | Input | Clock enable: CEK enables (registered HIGH) and CEK disables (registered LOW) the internal clock, input buffers, and output drivers. |
| RAS#, CAS#, WE# | Input | Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input | Reset: Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CEK is LOW and DQ are High-Z. |
| S0#, S1# | Input | Chip selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SA0–SA2 | Input | Presence-detect address inputs: These pins are used to configure the SPD EEPROM address range on the I ² C bus. |
| SCL | Input | Serial clock for SPD EEPROM: SCL is used to synchronize the presence-detect data transfer to and from the module. |
| CB0–CB7 | I/O | Check bits. |
| DQ0–DQ63 | I/O | Data input/output: Data bus. |
| DQS0–DQS17 | I/O | Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data. |
| SDA | I/O | Serial data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| VDD/VDDQ | Supply | Power supply: +2.5V ±0.2V (-40B: +2.6V ±0.1V). |
| VDDSPD | Supply | SPD EEPROM power supply: +2.3V to +3.6V. |
| VREF | Supply | SSTL_2 reference voltage (VDD/2). |
| VSS | Supply | Ground. |
| NC | – | No connect: These pins are not connected on the module. |

Functional Block Diagrams

Figure 4: Functional Block Diagram – Tall-Height Layout (1GB, 2GB)

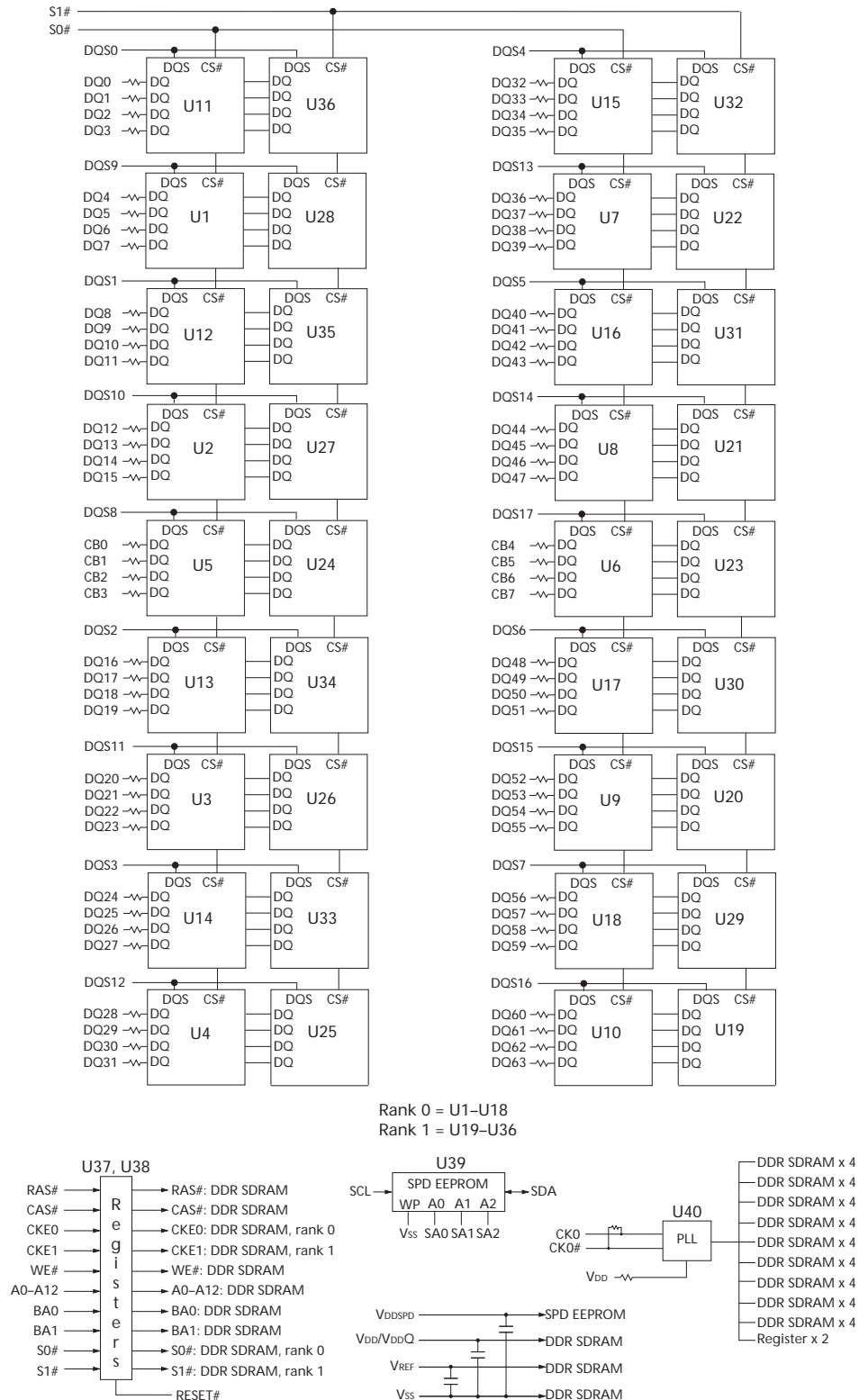


Figure 5: Functional Block Diagram – Standard-Height Layout (1GB)

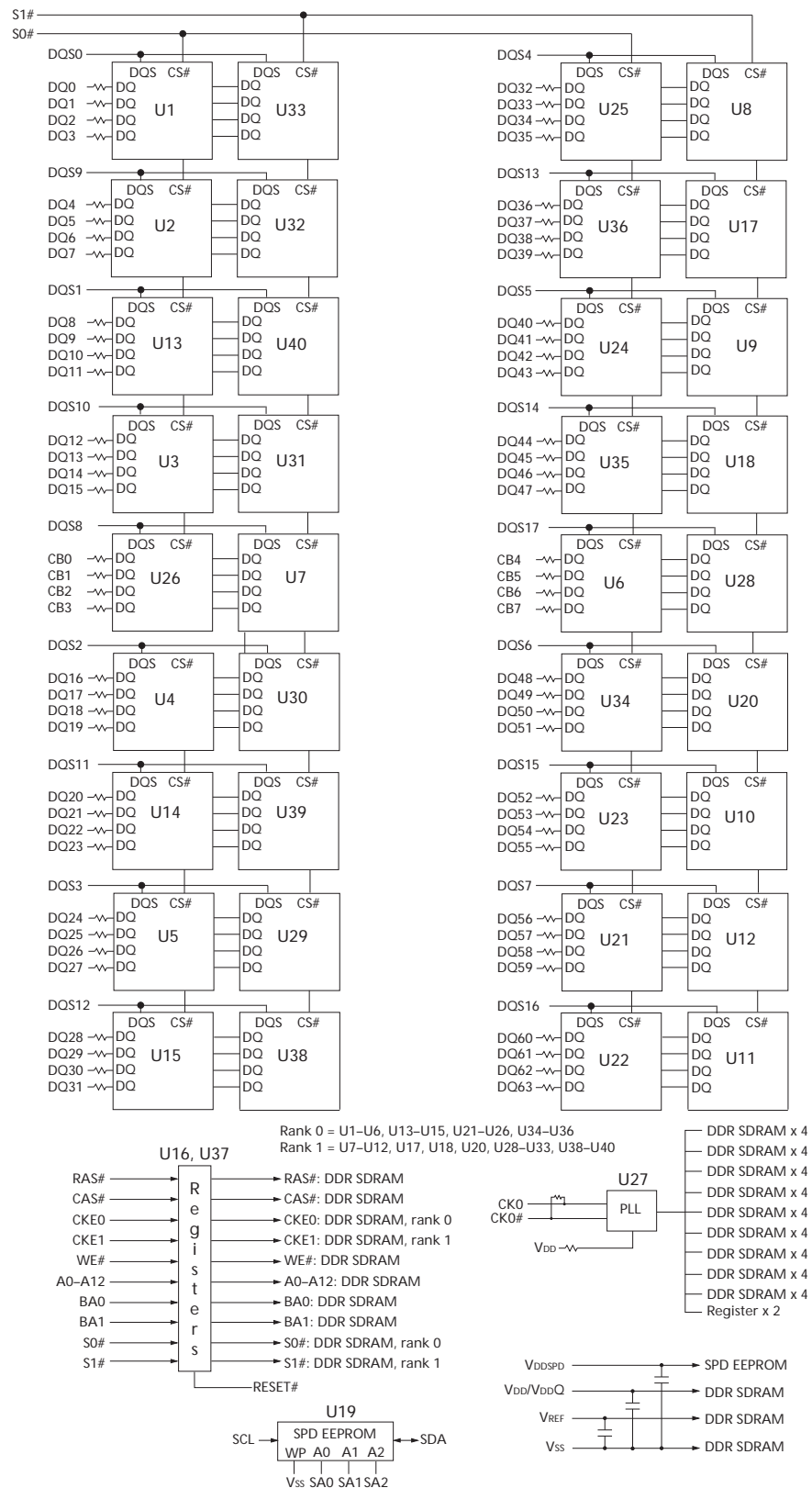
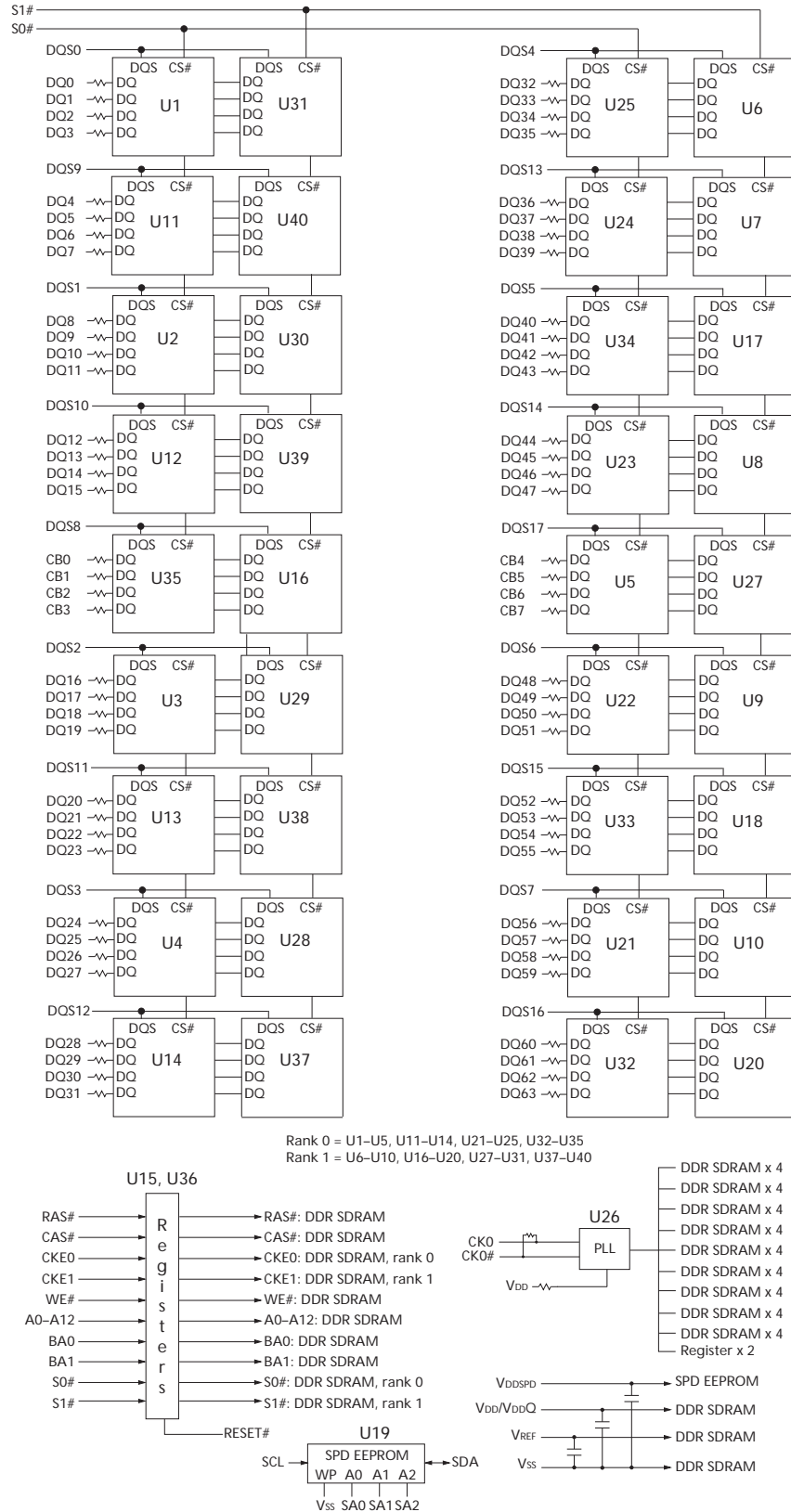


Figure 6: Functional Block Diagram – Standard-Height Layout (2GB)



General Description

The MT36VDDF12872 and MT36VDDF25672 are high-speed, CMOS dynamic random access 1GB and 2GB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR SDRAM modules operate in registered mode, where the control, command, and address input signals are latched in the registers on the rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR SDRAM devices. The register(s) and PLL reduce control, command, address, and clock signals loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various DDR SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to VSS, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

| Symbol | Parameter | | Min | Max | Units |
|-----------|---|--|------|------|-------------|
| VDD/VDDQ | VDD/VDDQ supply voltage relative to Vss | | -1.0 | +3.6 | V |
| VIN, VOUT | Voltage on any pin relative to Vss | | -0.5 | +3.2 | V |
| II | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 1.35V$ (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, BA, S#, CKE | -5 | +5 | μA |
| | | CK, CK# | -10 | +10 | |
| IOZ | Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ are disabled | DQ, DQS | -10 | +10 | μA |
| TA | DRAM ambient operating temperature ¹ | Commercial | 0 | +70 | $^{\circ}C$ |
| | | Industrial | -40 | +85 | $^{\circ}C$ |

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in table 8.

Table 8: Module and Component Speed Grades
DDR components may exceed the listed module speed grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -40B | -5B |
| -335 | -6 |
| -262 | -75E |
| -26A | -75Z |
| -265 | -75 |

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

IDD Specifications

Table 9: IDD Specifications and Conditions – 1GB (Die Revision K)

Values are for the MT46V64M4 DDR SDRAM only and are computed from values specified in the 256Mb (64 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -40B | -335 | Units | |
|--|---------------------------------|--------------------|-------|-------|----|
| Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN}); t_{CK} = t_{CK}(\text{MIN});$ DQ and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | IDD0 ¹ | 1,872 | 1,692 | mA | |
| Operating one bank active-read-precharge current: BL = 2; $t_{RC} = t_{RC}(\text{MIN});$ $t_{CK} = t_{CK}(\text{MIN}); I_{OUT} = 0\text{mA};$ Address and control inputs changing once per clock cycle | IDD1 ¹ | 2,232 | 2,142 | mA | |
| Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN}); \text{CKE} = \text{LOW}$ | IDD2P ² | 144 | 144 | mA | |
| Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN}); \text{CKE} = \text{HIGH};$ Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ and DQS | IDD2F ² | 1,800 | 1,800 | mA | |
| Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN}); \text{CKE} = \text{LOW}$ | IDD3P ² | 1,260 | 1,080 | mA | |
| Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX}); t_{CK} = t_{CK}(\text{MIN});$ DQ and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | IDD3N ² | 2,160 | 1,980 | mA | |
| Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN});$ $I_{OUT} = 0\text{mA}$ | IDD4R ¹ | 3,312 | 2,952 | mA | |
| Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN});$ DQ and DQS inputs changing twice per clock cycle | IDD4W ¹ | 3,312 | 2,952 | mA | |
| Auto refresh current | $t_{RFC} = t_{RFC}(\text{MIN})$ | IDD5 ² | 5,760 | 5,760 | mA |
| | $t_{RFC} = 7.8125\mu\text{s}$ | IDD5A ² | 216 | 216 | mA |
| Self refresh current: CKE $\leq 0.2\text{V}$ | IDD6 ² | 144 | 144 | mA | |
| Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN}); t_{CK} = t_{CK}(\text{MIN});$ Address and control inputs change only during active READ or WRITE commands | IDD7 ¹ | 5,292 | 4,932 | mA | |

- Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
 2. Value calculated reflects all module ranks in this operating condition.

Table 10: IDD Specifications and Conditions – 1GB (All Other Die Revisions)

Values are for the MT46V64M4 DDR SDRAM only and are computed from values specified in the 256Mb (64 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -40B | -335 | -262 | -26A/ -265 | Units |
|--|---------------------------------|-------|-------|-------|-----------------|-------|
| Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | IDD0 ¹ | 2,502 | 2,322 | 2,322 | 2,232 | mA |
| Operating one bank active-read-precharge current: BL = 2; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; I _{OUT} = 0mA; Address and control inputs changing once per clock cycle | IDD1 ¹ | 3,132 | 3,132 | 2,952 | 2,682 | mA |
| Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD2P ² | 144 | 144 | 144 | 144 | mA |
| Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ and DQS | IDD2F ² | 2,160 | 1,800 | 1,620 | 1,620 | mA |
| Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD3P ² | 1,440 | 1,080 | 900 | 900/ 1,080 | mA |
| Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | IDD3N ² | 2,520 | 2,160 | 1,800 | 1,800 | mA |
| Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; I _{OUT} = 0mA | IDD4R ¹ | 3,672 | 3,222 | 2,772 | 2,772 | mA |
| Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing twice per clock cycle | IDD4W ¹ | 3,582 | 3,222 | 2,772 | 2,772 | mA |
| Auto refresh current | $t_{RFC} = t_{RFC}(\text{MIN})$ | 9,360 | 9,180 | 8,460 | 8,460/ 8,820 | mA |
| | $t_{RFC} = 7.8125\mu\text{s}$ | 216 | 216 | 216 | 216 | mA |
| Self refresh current: CKE ≤ 0.2V | IDD6 ² | 144 | 144 | 144 | 144 | mA |
| Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands | IDD7 ¹ | 8,532 | 7,452 | 6,372 | 6,372/ 6,642 | mA |

- Notes: 1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 11: IDD Specifications and Conditions – 2GB

Values are for the MT46V128M4 DDR SDRAM only and are computed from values specified in the 512Mb (128 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -40B | -335 | -262 | -26A/ -265 | Units | |
|--|---------------------------------|--------------------|--------|--------|---------------|--------|----|
| Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | IDD0 ¹ | 2,880 | 2,430 | 2,430 | 2,160 | mA | |
| Operating one bank active-read-precharge current: BL = 2; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; IOUT = 0mA; Address and control inputs changing once per clock cycle | IDD1 ¹ | 3,420 | 2,970 | 2,970 | 2,700 | mA | |
| Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD2P ² | 180 | 180 | 180 | 180 | mA | |
| Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ and DQS | IDD2F ² | 1,980 | 1,620 | 1,620 | 1,440 | mA | |
| Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD3P ² | 1,620 | 1,260 | 1,260 | 1,080 | mA | |
| Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | IDD3N ² | 2,160 | 1,800 | 1,800 | 1,620 | mA | |
| Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; IOUT = 0mA | IDD4R ¹ | 3,510 | 3,060 | 3,060 | 2,700 | mA | |
| Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ and DQS inputs changing twice per clock cycle | IDD4W ¹ | 3,600 | 3,240 | 2,880 | 2,520 | mA | |
| Auto refresh current | $t_{RFC} = t_{RFC}(\text{MIN})$ | IDD5 ² | 12,420 | 10,440 | 10,440 | 10,080 | mA |
| | $t_{RFC} = 7.8125\mu\text{s}$ | IDD5A ² | 396 | 360 | 360 | 360 | mA |
| Self refresh current: CKE ≤ 0.2V | IDD6 ² | 180 | 180 | 180 | 180 | mA | |
| Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands | IDD7 ¹ | 8,190 | 7,380 | 7,290 | 6,390 | mA | |

- Notes: 1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Register and PLL Specifications

Table 12: Register Specifications
SSTV16859 devices or equivalent JESD82-4B

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|---------------------|---------------------------|---|----------------------------|----------------------------|-------|
| DC high-level input voltage | V _{IH(DC)} | Control, command, address | SSTL_25 | V _{REF(DC)} + 150 | – | mV |
| DC low-level input voltage | V _{IL(DC)} | Control, command, address | SSTL_25 | – | V _{REF(DC)} - 150 | mV |
| AC high-level input voltage | V _{IH(AC)} | Control, command, address | SSTL_25 | V _{REF(DC)} + 310 | V _{DD} | mV |
| AC low-level input voltage | V _{IL(AC)} | Control, command, address | SSTL_25 | – | V _{REF(DC)} - 310 | mV |
| Output high voltage | V _{OH} | Parity output | LVC MOS | V _{DD} - 0.2 | – | V |
| Output low voltage | V _{OL} | Parity output | LVC MOS | – | 0.2 | V |
| Input current | I _I | All pins | V _I = V _{DDQ} or V _{SSQ} | -5.0 | +5.0 | μA |
| Static standby | I _{DD} | All pins | RESET# = V _{SSQ} (I _O = 0) | – | 100 | μA |
| Static operating | I _{DD} | All pins | RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _O = 0 | – | Varies by manufacturer | mA |
| Dynamic operating (clock tree) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle | – | Varies by manufacturer | μA |
| Dynamic operating (per each input) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle; One data input switching at ^t CK/2, 50% duty cycle | – | Varies by manufacturer | μA |
| Input capacitance (per device, per pin) | C _I | All inputs except RESET# | V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V | 2.5 | 3.5 | pF |
| Input capacitance (per device, per pin) | C _I | RESET# | V _I = V _{DDQ} or V _{SSQ} | – | Varies by manufacturer | pF |

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.

Table 13: PLL Specifications
 CVF857 device or equivalent JESD82-1A

| Parameter | Symbol | Min | Max | Units |
|---------------------------------------|---------------------|-----------------------------|-----------------------------|-------|
| DC high-level input voltage | V _{IH} | 1.7 | V _{DDQ} + 0.3 | V |
| DC low-level input voltage | V _{IL} | -0.3 | 0.7 | V |
| Input voltage (limits) | V _{IN} | -0.3 | V _{DDQ} + 0.3 | V |
| Input differential-pair cross voltage | V _{IX} | (V _{DDQ} /2) - 0.2 | (V _{DDQ} /2) + 0.2 | V |
| Input differential voltage | V _{ID(DC)} | 0.36 | V _{DDQ} + 0.6 | V |
| Input differential voltage | V _{ID(AC)} | 0.70 | V _{DDQ} + 0.6 | V |
| Input current | I _I | -10 | +10 | μA |
| Dynamic supply current | I _{DDPD} | - | 200 | μA |
| Dynamic supply current | I _{DDQ} | - | 300 | μA |
| Dynamic supply current | I _{ADD} | - | 12 | mA |
| Input capacitance | C _{IN} | 2.0 | 3.5 | pF |

Table 14: PLL Clock Driver Timing Requirements and Switching Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|---------------------|-----|------|-------|
| Stabilization time | t _L | - | 100 | μs |
| Input clock slew rate | t _{slr(i)} | 1.0 | 4.0 | V/ns |
| SSC modulation frequency | - | 30 | 50 | kHz |
| SSC clock input frequency deviation | - | 0 | -0.5 | % |
| PLL loop bandwidth (-3dB from unity gain) | - | 2.0 | - | MHz |

- Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82-1A.

Serial Presence-Detect

Table 15: Serial Presence-Detect EEPROM DC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|--|-----------------|--------------|--------------|-------|
| Supply voltage | VDDSPD | 2.3 | 3.6 | V |
| Input high voltage: Logic 1; All inputs | V _{IH} | VDDSPD × 0.7 | VDDSPD + 0.5 | V |
| Input low voltage: Logic 0; All inputs | V _{IL} | -1.0 | VDDSPD × 0.3 | V |
| Output low voltage: I _{OUT} = 3mA | V _{OL} | - | 0.4 | V |
| Input leakage current: V _{IN} = GND to V _{DD} | I _{LI} | - | 10 | μA |
| Output leakage current: V _{OUT} = GND to V _{DD} | I _{LO} | - | 10 | μA |
| Standby current: SCL = SDA = V _{DD} - 0.3V; All other inputs = V _{SS} or V _{DD} | I _{SB} | - | 30 | μA |
| Power supply current: SCL clock frequency = 100 kHz | I _{CC} | - | 2.0 | mA |

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid | t _{AA} | 0.2 | 0.9 | μs | 1 |
| Time the bus must be free before a new transition can start | t _{BUF} | 1.3 | - | μs | |
| Data-out hold time | t _{HD:DAT} | 200 | - | ns | |
| SDA fall time | t _F | - | 300 | ns | 2 |
| SDA rise time | t _R | - | 300 | ns | 2 |
| Data-in hold time | t _{HD:DI} | 0 | - | μs | |
| Start condition hold time | t _{HD:STA} | 0.6 | - | μs | |
| Clock HIGH period | t _{HIGH} | 0.6 | - | μs | |
| Clock LOW period | t _{LOW} | 1.3 | - | μs | |
| SCL clock frequency | f _{SCL} | - | 400 | kHz | |
| Data-in setup time | t _{SU:DAT} | 100 | - | ns | |
| Start condition setup time | t _{SU:STA} | 0.6 | - | μs | 3 |
| Stop condition setup time | t _{SU:STO} | 0.6 | - | μs | |
| WRITE cycle time | t _{WRC} | - | 5 | ms | 4 |

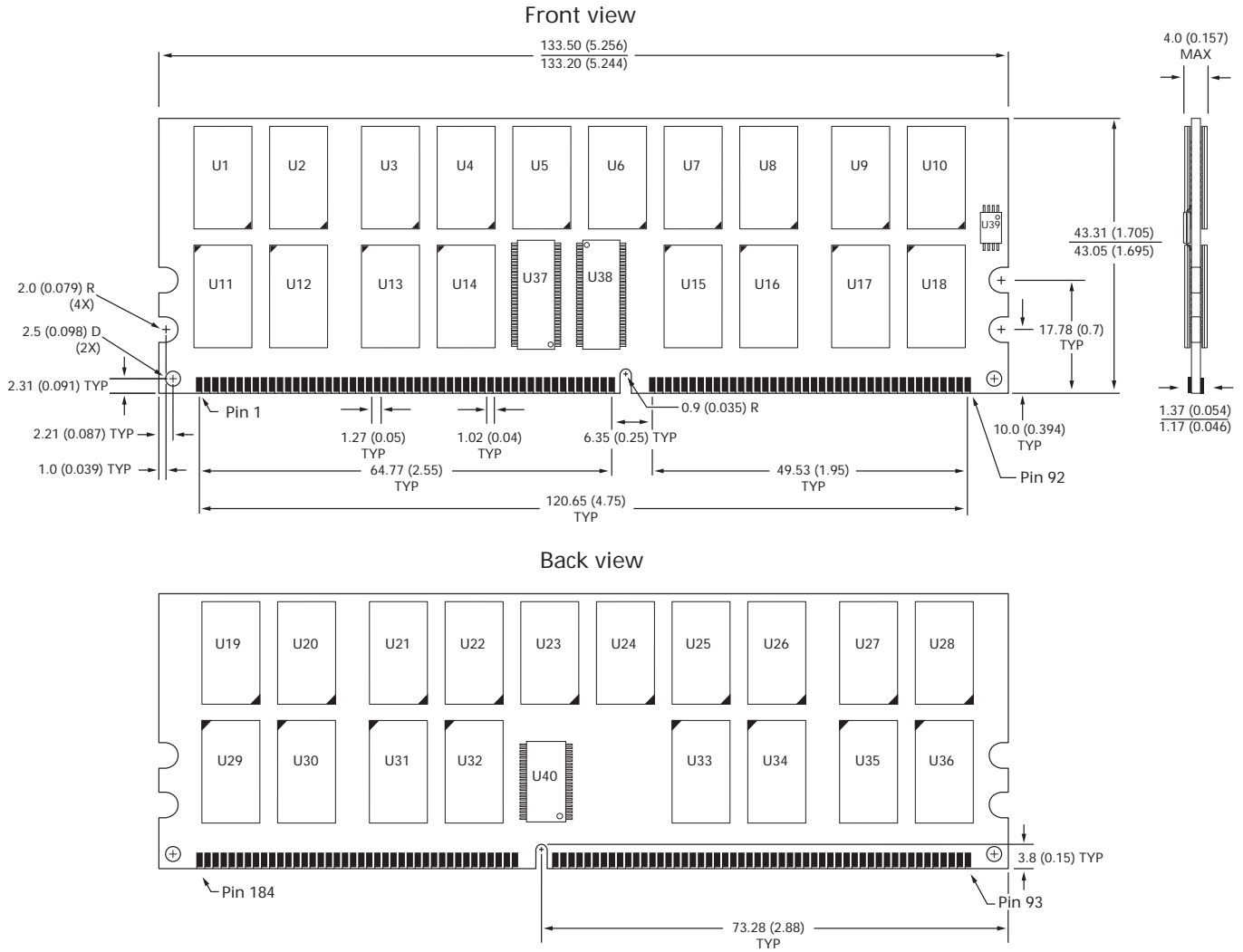
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD.

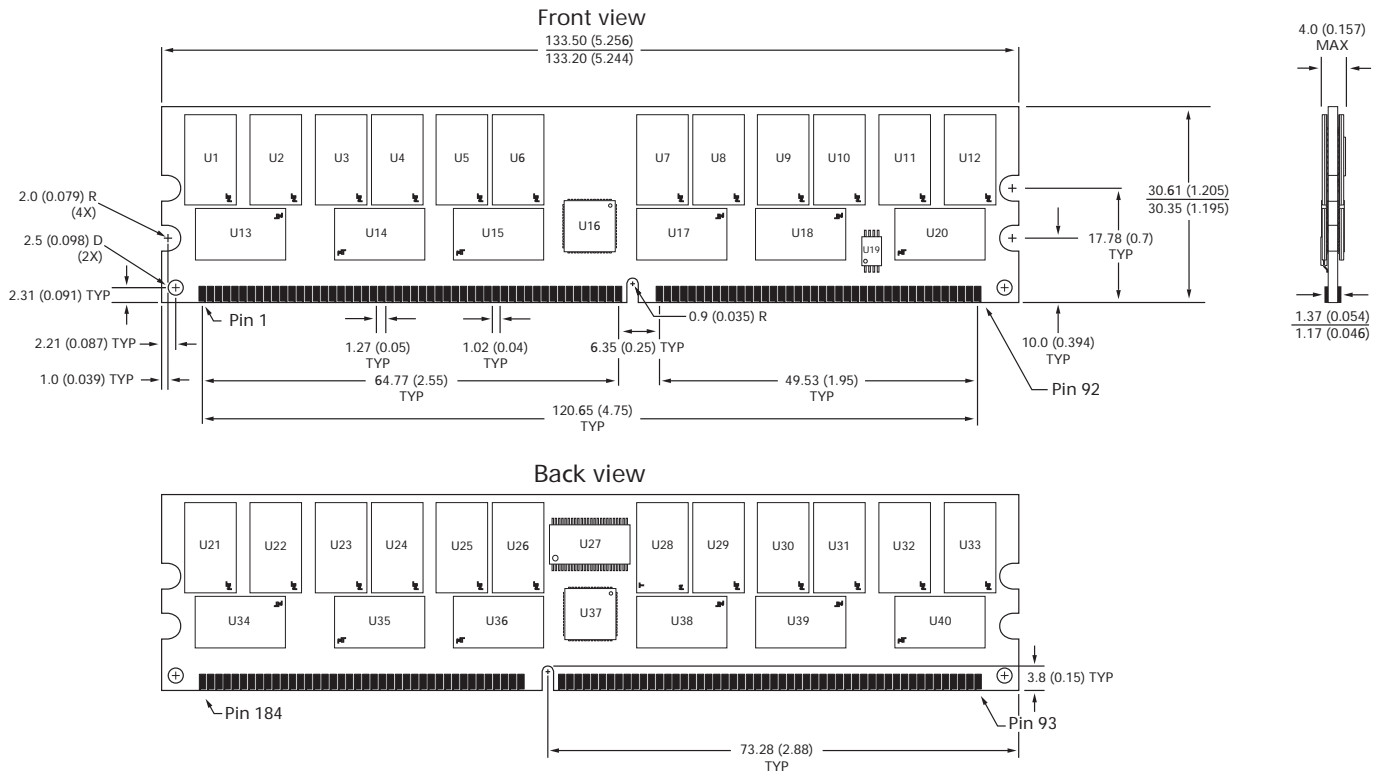
Module Dimensions

Figure 7: 184-Pin RDIMM – Tall-Height Layout (1GB, 2GB)



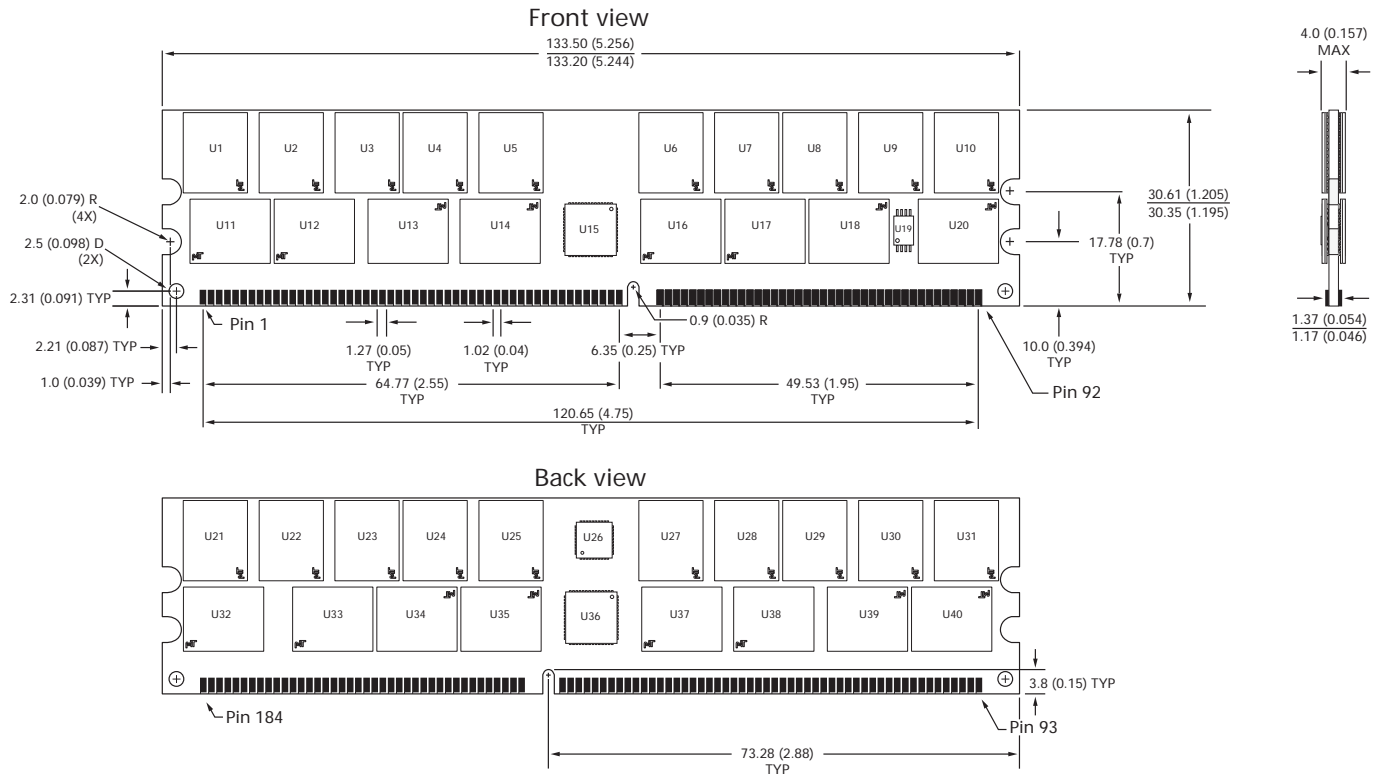
- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

Figure 8: 184-Pin RDIMM – Standard-Height Layout (1GB)



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

Figure 9: 184-Pin RDIMM – Standard-Height Layout (2GB)



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.



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