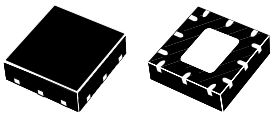
ST2S08B

Dual synchronous rectification, 1.5 A, 1.5 MHz adjustable step-down switching regulator

Features

- Step-down current mode PWM (1.5 MHz) DC-DC converter
- Adjustable output voltage from 0.8 V
- 2 % DC output voltage tolerance
- Synchronous rectification
- Integrated current limit
- Inhibit function
- Soft-start for start delay of 800 µs typ.
- Typical efficiency: > 80 % at V_{OUT} = 1.2 V
- 1.5 A output current capability
- Non-switching quiescent current: max 1 mA over temperature range
- $R_{DS(ON)}$ 150 mΩ (typ.)
- Uses tiny capacitors and inductors
- Available in QFN12L (4 x 4 mm)



QFN12L (4 x 4 mm)

ST2S08B is available in the QFN12L (4 x 4 mm) package.

Description

The ST2S08B is a dual step-down DC-DC converter optimized for powering low-voltage digital cores in ODD applications and, generally, to replace the high current linear solution when the power dissipation may cause a high heating of the application environment. It provides up to 1.5 A over an input voltage range of 3 V to 5.5 V. A high switching frequency of 1.5 MHz allows the use of tiny surface-mounted components as well as a resistor divider to set the output voltage value. Only an inductor and two capacitors are required. A low output ripple is guaranteed by the current mode PWM topology and the utilization of low ESR SMD ceramic capacitors. The device is thermally protected and current limited. The

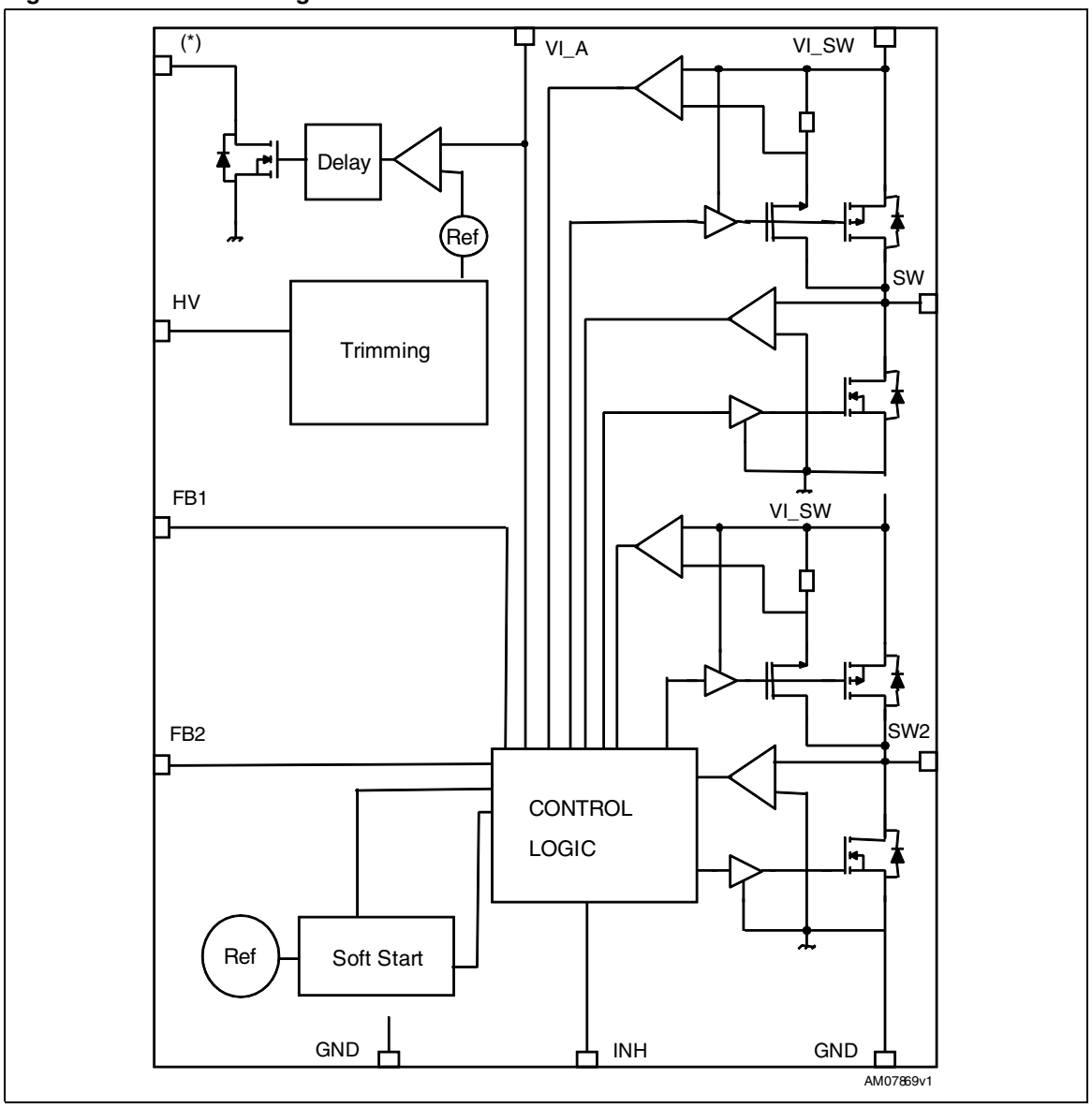
Table 1. Device summary

Order code	Package	Packaging
ST2S08BPQR	QFN12L (4 x 4 mm)	Tape and reel

Contents

1 Diagram

Figure 1. Schematic diagram



* Not available on the ST2S08B version.

2 Pin configuration

Figure 2. Pin connections (top view)

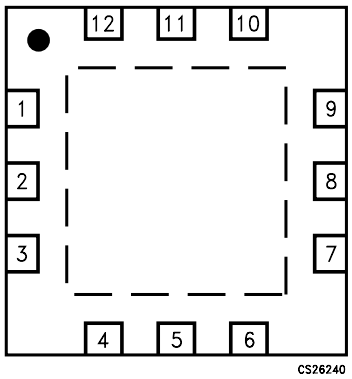


Table 2. Pin description

Pin n°	Name	Function
1	HV	Programing pin. It must be floating or connected to GND.
2	FB2	Feedback voltage
3	GND2	Power ground
4	SW2	Switching pin
5	VIN_SW	Power input voltage pin
6	SW1	Switching pin
7	GND1	Power ground
8	FB1	Feedback voltage/output voltage
9	NC	Not connect
10	INH	Inhibit pin: - High device on - Low device off
11	VIN_A	Supply for analog circuit
12	GND_A	System ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Inhibit voltage	-0.3 to 7	V
SWITCH voltage	Max. voltage of output pin	-0.3 to 7	V
$V_{FB1,2}$	Feedback voltage/output voltage	-0.3 to 2.5	V
Current into V_{FB} pin	Common mode input voltage	+1 to -1	mA
T_J	Max junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec.	300	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	60	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM-DH11C	4	kV

4 Electrical characteristics

$V_{IN\_SW} = V_{IN\_A} = 5$ V, $V_{O1,2}$ =1.2 V, C_1= 4.7 µF, $C_2 = C_3$ = 22 µF, L1 = L2 = 3.3 µH, T_J = -30 to 125 °C, unless otherwise specified. Typical values refer to 25 °C.

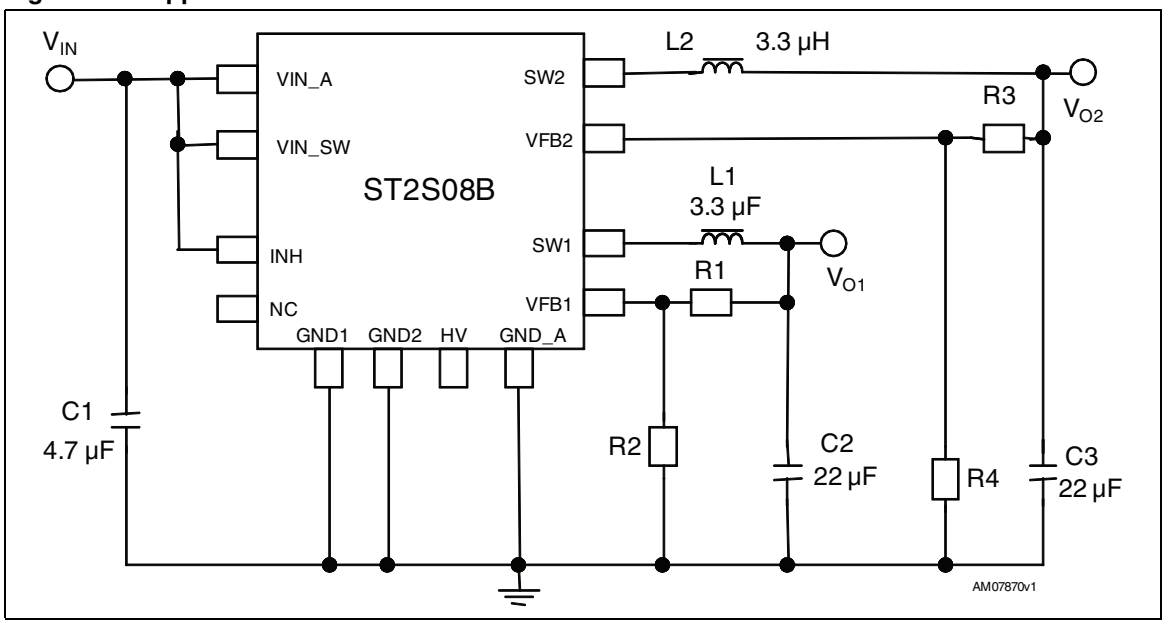
Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$FB_{1,2}$	Feedback voltage		784	800	816	mV
$I_{FB1,2}$	V_{FB} pin bias current	V_{FB} = 1 V			600	nA
I_Q	Quiescent current	V_{INH} > 1.2 V, V_{FB} = 1 V			1.5	mA
		V_{INH} = GND		20		µA
$I_{O1,2}$	Output current	V_{IN} = 3.0 to 5.5 V (1), T_J = - 30 to 85 °C	1.5			A
I_{MIN}	Minimum output current		1			mA
V_{INH}	Inhibit threshold	3.0 V < V_{IN} < 5 V	1.2			V
		3.0 V < V_{IN} < 5.5 V	1.3			
		Device OFF			0.4	
$I_{INH1,2}$	Inhibit pin current				2	µA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	3.0 V < V_{IN} < 5.5 V		0.04		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	10 mA < I_O < 1.5 A		10		mV
PWM f_S	PWM switching frequency	V_{FB} = 0.7 V, T_A = 25 °C	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7 V, T_A = 25 °C	85	94		%
I_{SWL}	Switching current limitation	(2)		2		A
I_{LKN}	NMOS leakage current	V_{FB} = 0.9 V, T_A = 25 °C		0.1		µA
I_{LKP}	PMOS leakage current	V_{FB} = 0.9 V, T_A = 25 °C		0.1		µA
R_{DSon}-N	NMOS switch on resistance	I_{SW} = 250 mA		0.15	0.3	Ω
R_{DSon}-P	PMOS switch on resistance	I_{SW} = 250 mA		0.2	0.4	Ω
η	Efficiency	I_O = 20 mA to 100 mA		75		%
		I_O = 100 mA to 1.5 A		80		%
T_{SHDN}	Thermal shutdown			150		°C
T_{HYS}	Thermal shutdown hysteresis			15		°C
I_{SC} - V_{IN}	Short-circuit V_{IN} range (2)	Output short-circuit to ground	3		5.3	V

1. V_O= 90 % of nominal value.
2. Guaranteed by design, but not tested in production.

5 Typical application

Figure 3. Application circuit



Note: R1, R2 and R3, R4 are calculated according to the following equations:

- $V_{O1} = V_{FB1} (1 + R1 / R2)$

- $V_{O2} = V_{FB2} (1 + R3 / R4)$

6 Typical performance characteristics

Figure 4. Feedback voltage vs. temperature

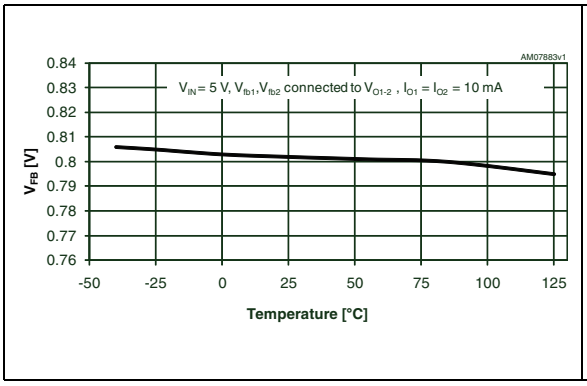


Figure 5. Efficiency vs. output current 1

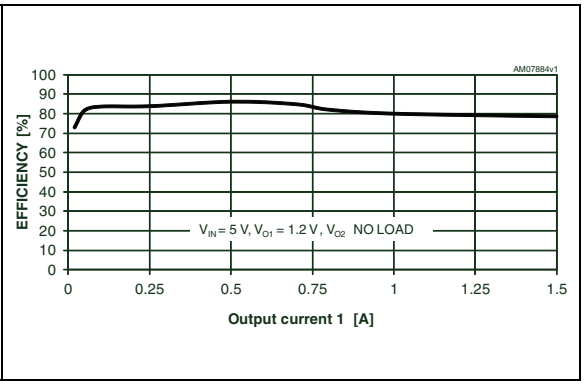


Figure 6. Efficiency vs. output current 2

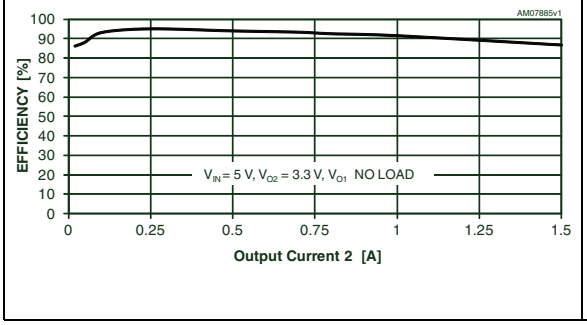


Figure 7. Switching frequency vs. temperature

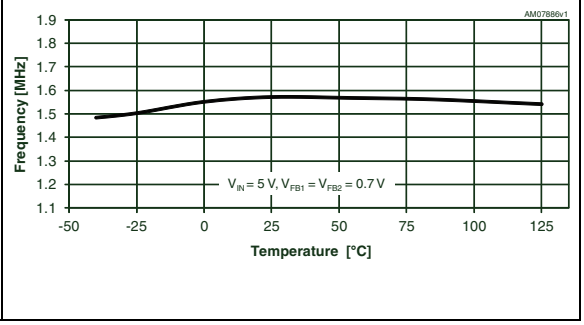


Figure 8. Duty cycle vs. temperature

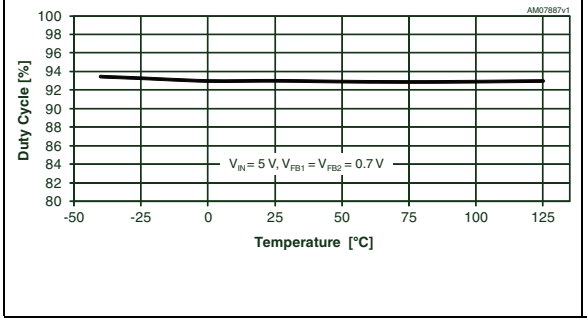


Figure 9. Inhibit threshold vs. temperature

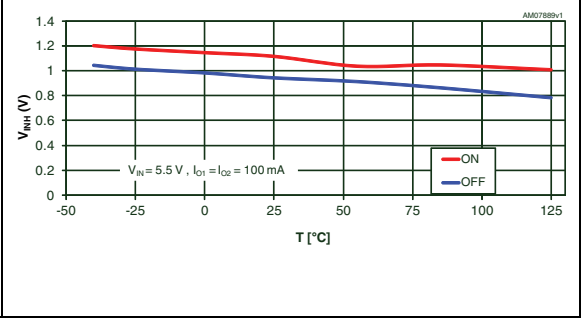


Figure 10. Switching current limitation vs. temperature

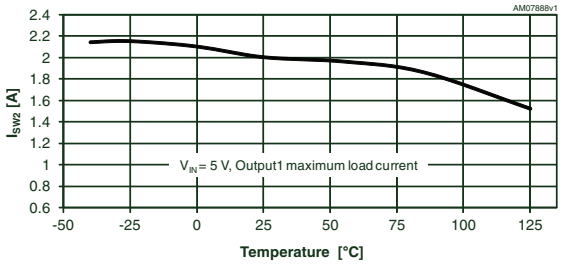
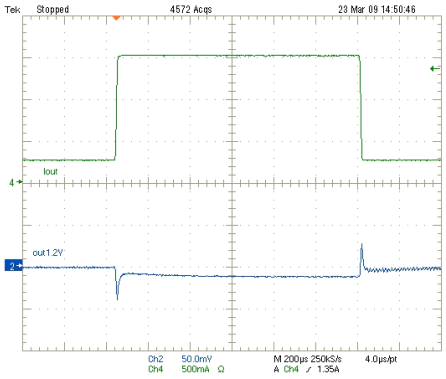
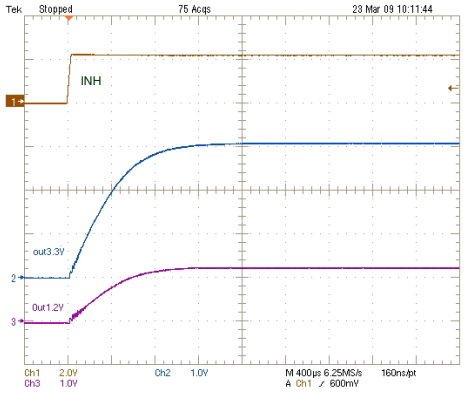


Figure 11. Load transient response



V_{IN} = 5 V, I_{O1} from 250 mA to 1.5 A V_{O1} @ 1.2 V

Figure 12. Inhibit transient



V_{INH} = from 0 V to 2 V, V_{IN} = 5.5 V, I_{O1} = I_{O2} = 1.5 A

7 General information

The ST2S08B is a dual adjustable current mode PWM step-down DC-DC converter.

It is a complete 1.5 A switching regulator with internal compensation that eliminates the need for additional components.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors, results in low, predictable output ripple.

To clamp the error amplifier reference voltage, a soft-start control block, generating a voltage ramp, has been implemented. Other circuits fitted to the device protection are the thermal shut-down block, which turns off the regulator when the junction temperature exceeds 150 °C (typ.), and cycle-by-cycle switching current limiting.

Operation of the device requires few components: 2 inductors, 3 capacitors, and a resistor divider. The chosen inductor must be capable of not saturating at the peak current level. Its value should be selected keeping in mind that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce package size and total application cost.

Finally, the ST2S08 has been designed to work properly with X5R or X7R SMD ceramic capacitors both at input and at output. These types of capacitors, due to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used, according to the needs of the application, without compromising the correct functioning of the device.

8 Application information

8.1 Introduction

The following technical information is used for estimating typical external component characteristics using standard equations. Nevertheless, it is strongly recommended to validate the suitability of external components to the application requirements by thoroughly testing any solution at bench level on a real evaluation circuit.

8.2 Programming the output voltage

The output voltage for both channels can be adjusted from 0.8 V up to 85 % of the input voltage value by connecting a resistor divider between V_O and GND, the middle point of the divider must be connected to the feedback (FB) pin, as shown in *Figure 3*.

The resistor divider must be chosen according to the following equations:

Equation 1

$$V_{O1} = V_{FB1} \times \left(1 + \frac{R1}{R2}\right)$$

Equation 2

$$V_{O2} = V_{FB2} \times \left(1 + \frac{R3}{R4}\right)$$

Using a resistor with a value in the range of 1 kΩ to 50 kΩ is recommended. Lower values are also suitable, but increase current consumption.

8.3 Inductor selection

The inductor is the key passive component for switching converters.

The critical inductance values can then be obtained according to the following formulas:

Equation 3

$$L_{MIN} = \frac{V_O \times (V_{IN\_MAX} - V_O)}{V_{IN\_MAX} \times F_{SW} \times \Delta I_L}$$

F_{SW} = switching frequency

ΔI_L = the peak-to-peak inductor ripple current. As a rule of thumb, the peak-to-peak ripple can be set at 20 % - 40 % of the output current.

The peak current of the inductor can be calculated as:

Equation 4

$$I_{PEAK} = (I_O / 0.8) + \frac{V_O \times (V_{IN\_MAX} - V_O)}{2 \times V_{IN\_MAX} \times F_{SW} \times L}$$

In addition to the inductance value, in order to avoid saturation, the maximum saturation current of the inductor must be higher than that of the I_{PEAK}.

8.4 Input and output capacitor selection

It is recommended to use ceramic capacitors with X5R or X7R dielectric and low ESR as input and output capacitors, in order to filter any disturbance present in the input line and to obtain stable operation. The output capacitor is very important for satisfying the output voltage ripple requirements.

The output voltage ripple (V_{O_RIPPLE}), in continuous mode, for the step-down channel, can be calculated as:

Equation 5

$$V_{O\_RIPPLE} = \Delta I_L \times \left[ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right]$$

where ΔI_L is the ripple current and F_{SW} is the switching frequency.

The use of ceramic capacitors with voltage ratings in the range higher than 1.5 times the maximum input or output voltage is recommended.

8.5 Layout considerations

Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. Important parameters (efficiency, output voltage ripple, switching noise immunity, etc.) can be affected if the PCB layout is not designed paying close attention to the following DC-DC general layout rules:

- Short, wide traces must be implemented for mains current and for power ground paths. The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor.
- The FB pin connection to the external resistor divider is a high impedance node, so interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce pick-up noise, the resistor divider must be placed very close to the device.
- A common ground node minimizes ground noise.
- The exposed pad of the package must be connected to the common ground node.

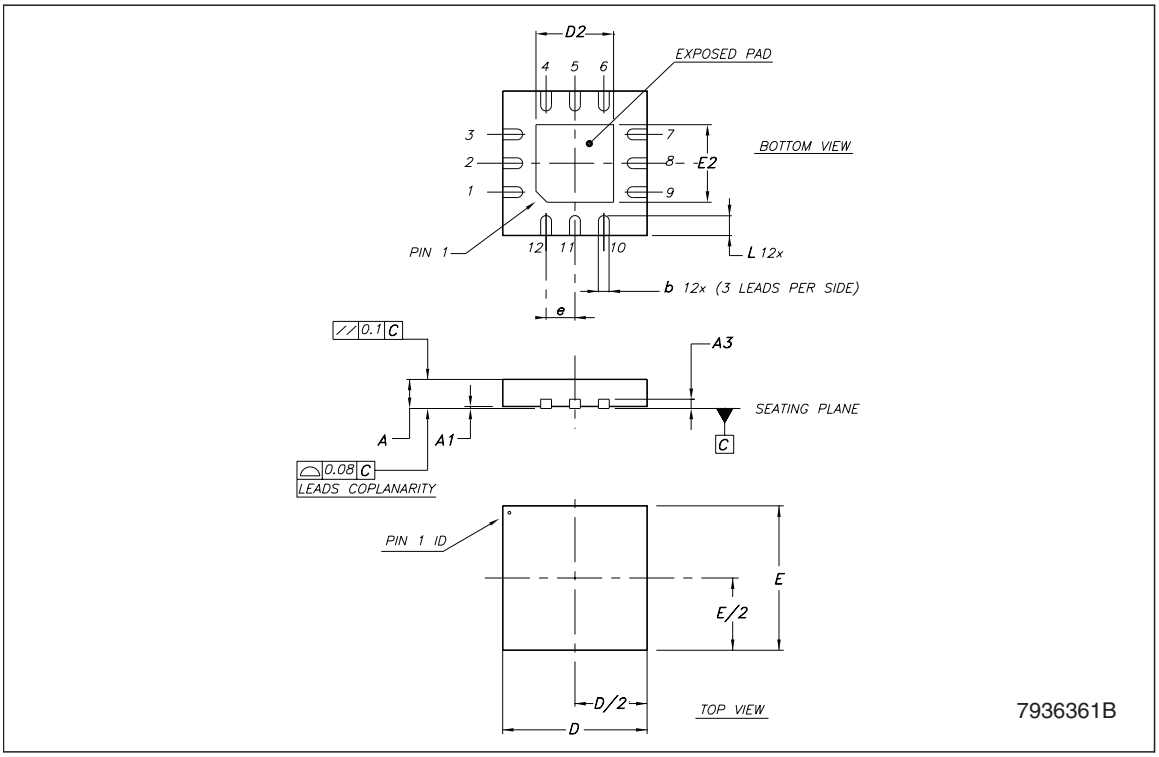
Moreover, the exposed pad ground connection must be properly designed in order to facilitate heat dissipation from the exposed pad to the ground layer using PCB vias.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: *www.st.com*. ECOPACK is an ST registered trademark.

QFN12L (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.00	2.15	2.25	0.079	0.085	0.089
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.00	2.15	2.25	0.079	0.085	0.089
e		0.80			0.031	
L	0.45	0.55	0.65	0.018	0.022	0.026



Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

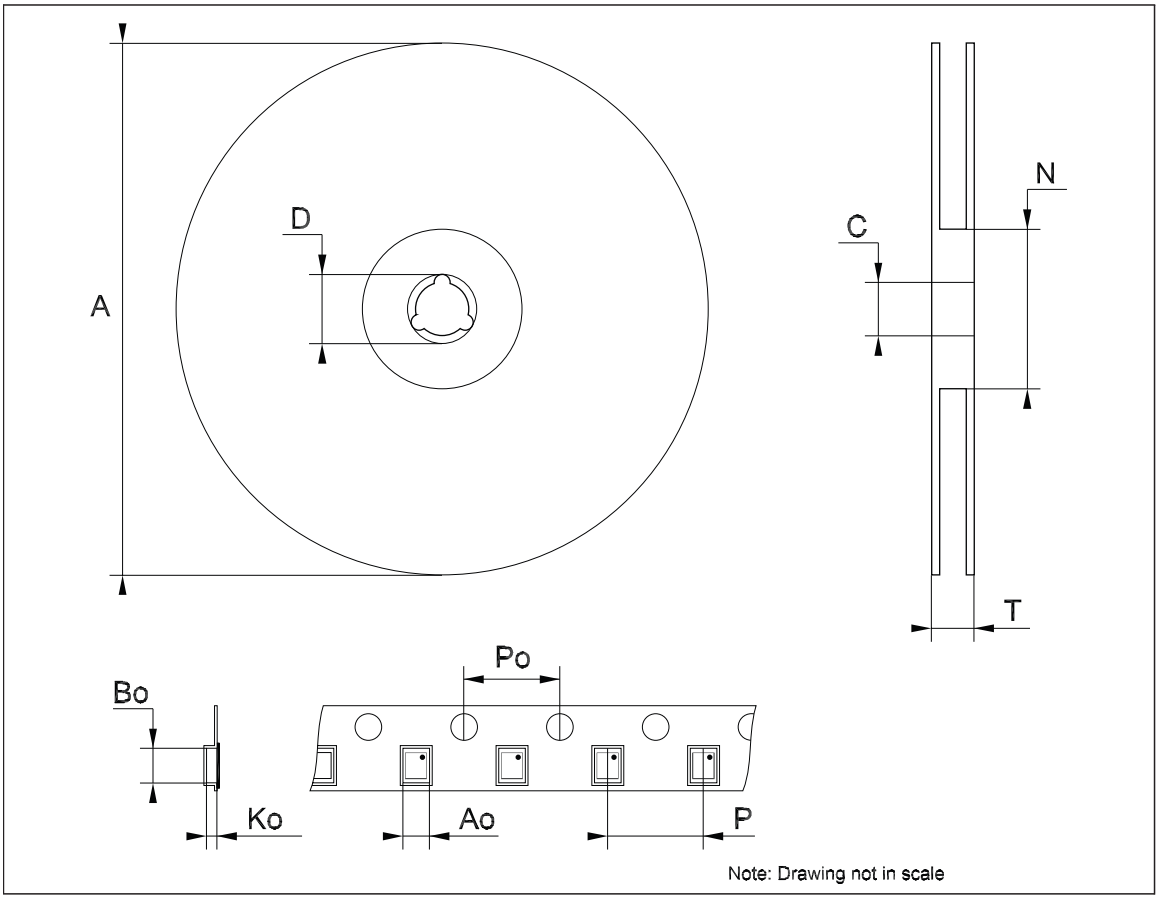
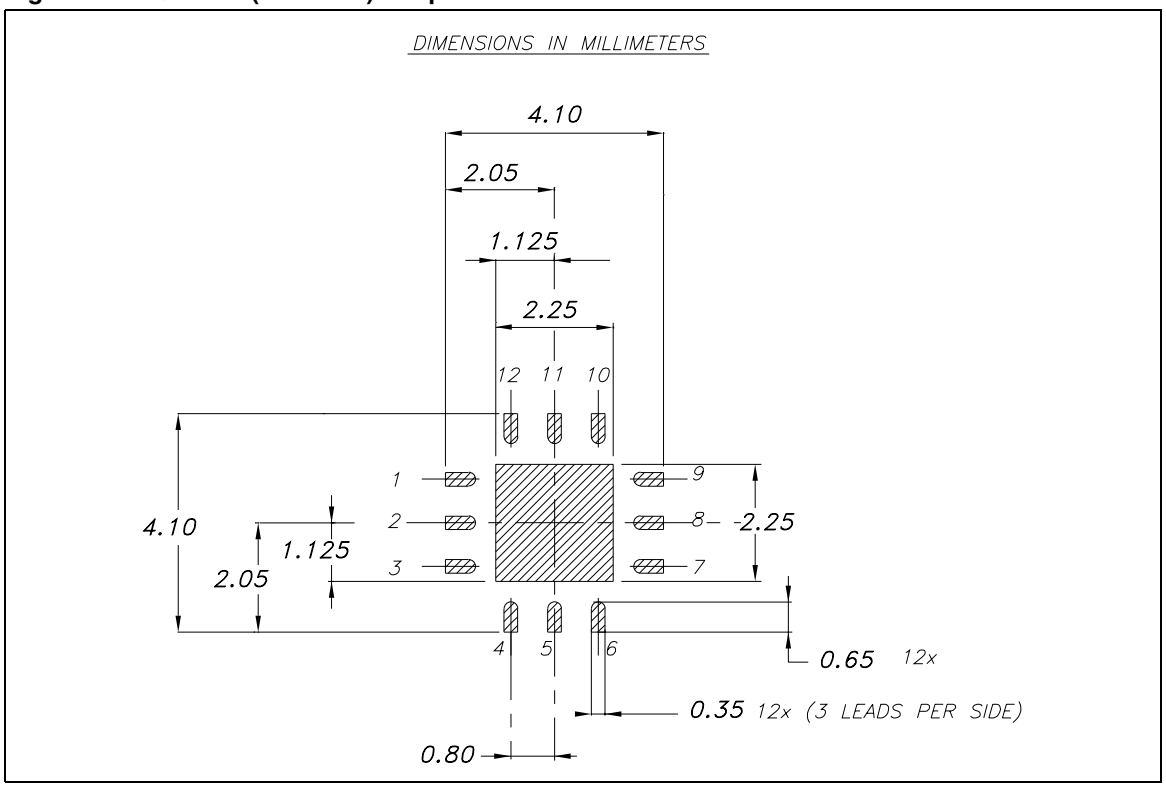


Figure 13. QFN12L (4 x 4 mm) footprint recommended data



10 Revision history

Table 7. Document revision history

Date	Revision	Changes
30-Nov-2010	1	Initial release.

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