

## Features

- Very high-speed: 45 ns
- Temperature ranges:
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - Typical standby current: 1 μA
  - Maximum standby current: 4 μA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 32-pin small outline integrated circuit (SOIC), 32-pin thin small outline package (TSOP I), and 32-pin STSOP packages

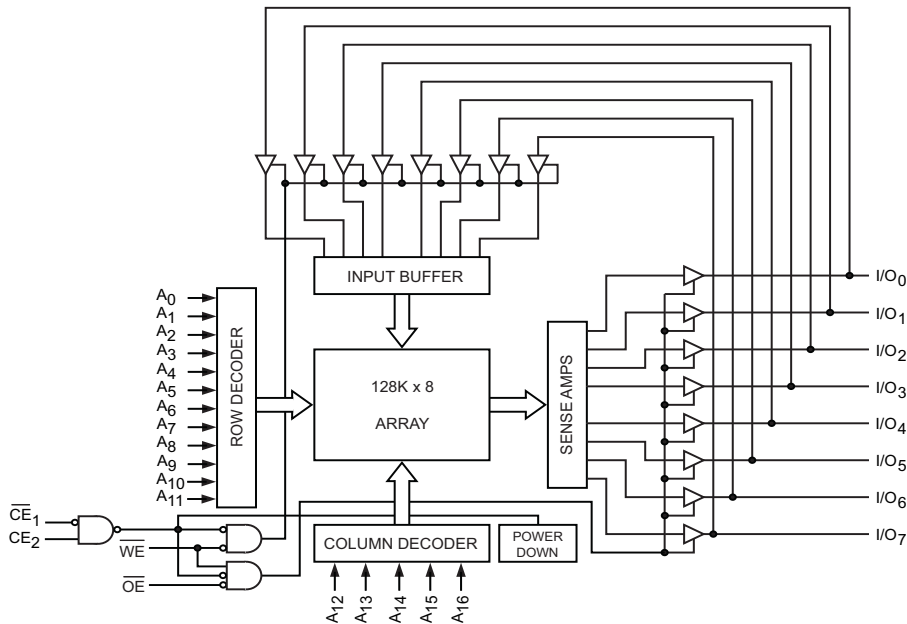
## Functional Description

The CY62128EV30<sup>[1]</sup> is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW). The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $CE_1$  LOW and  $CE_2$  HIGH and  $WE$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $WE$ ) inputs LOW. Data on the eight I/O pins is then written into the location specified on the Address pin ( $A_0$  through  $A_{16}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $WE$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

## Logic Block Diagram



### Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

## Contents

<b>Pin Configuration</b> .....	<b>3</b>	Ordering Code Definition .....	9
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>10</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>12</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>12</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	12
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>13</b>
<b>Data Retention Characteristics</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>14</b>
<b>Switching Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	14
<b>Switching Waveforms</b> .....	<b>7</b>	Products .....	14
Truth Table .....	8	PSoC Solutions .....	14
<b>Ordering Information</b> .....	<b>9</b>		

### Pin Configuration

Figure 1. 32-Pin STSOP [2]

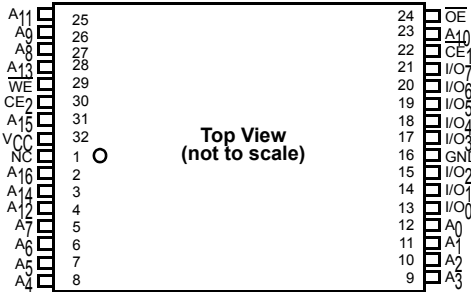


Figure 2. 32-Pin TSOP I [2]

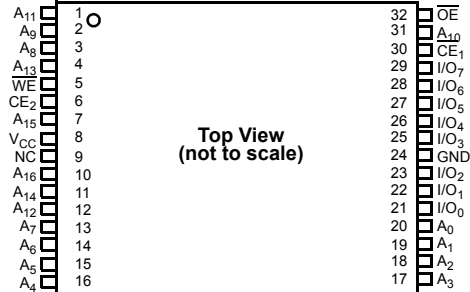


Figure 3. 32-Pin SOIC [2]

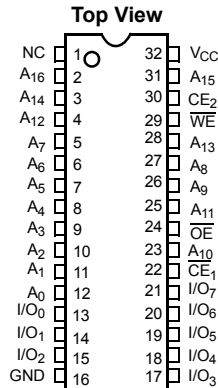


Table 1. Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
						f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max			
CY62128EV30LL	Auto-A	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4
CY62128EV30LL	Auto-E	2.2	3.0	3.6	55	1.3	4.0	11	35	1	30

Table 2. Pin Definitions

Input	A <sub>0</sub> –A <sub>16</sub> . Address inputs
Input/output	I/O <sub>0</sub> –I/O <sub>7</sub> . Data lines. Used as input or output lines depending on operation
Input/control	$\overline{WE}$ . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	$\overline{CE}_1$ . Chip Enable 1, Active LOW.
Input/control	CE <sub>2</sub> . Chip Enable 2, Active HIGH.
Input/control	OE. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	GND. Ground for the device
Power supply	V <sub>CC</sub> . Power supply for the device

Notes

2. NC pins are not connected on the die.

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC voltage applied to outputs in High-Z state<sup>[4, 5]</sup> ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC input voltage<sup>[4, 5]</sup> ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62128EV30LL	Auto-A	-40 °C to +85 °C	2.2 V to 3.6 V
	Auto-E	-40 °C to +125 °C	

## Electrical Characteristics

(Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ <sup>[7]</sup>	Max	Min	Typ <sup>[7]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> ≤ 2.70 V	2.0	-	-	2.0	-	-	V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70 V	2.4	-	-	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 0.1 mA	-	-	0.4	-	-	0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70 V	-	-	0.4	-	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> = 2.2 V to 2. V	1.8	-	V <sub>CC</sub> + 0.3V	1.8	-	V <sub>CC</sub> + 0.3V	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.2	-	V <sub>CC</sub> + 0.3V	2.2	-	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 2.2 V to 2.7 V	-0.3	-	0.6	-0.3	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-0.3	-	0.8	-0.3	-	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	-4	-	+4	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-1	-	+1	-4	-	+4	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub> f = 1 MHz	-	11	16	-	11	35	mA
		V <sub>CC</sub> = V <sub>CCmax</sub> I <sub>OUT</sub> = 0 mA CMOS levels	-	1.3	2.0	-	1.3	4.0	mA
I <sub>SB1</sub>	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ , CE <sub>2</sub> < 0.2 V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V f = f <sub>max</sub> (address and data only), f = 0 (OE and WE), V <sub>CC</sub> = 3.60 V	-	1	4	-	1	35	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ , CE <sub>2</sub> < 0.2 V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> < 0.2 V, f = 0, V <sub>CC</sub> = 3.60 V	-	1	4	-	1	30	μA

### Notes

4. V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.

5. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.

6. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C

8. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) must be at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

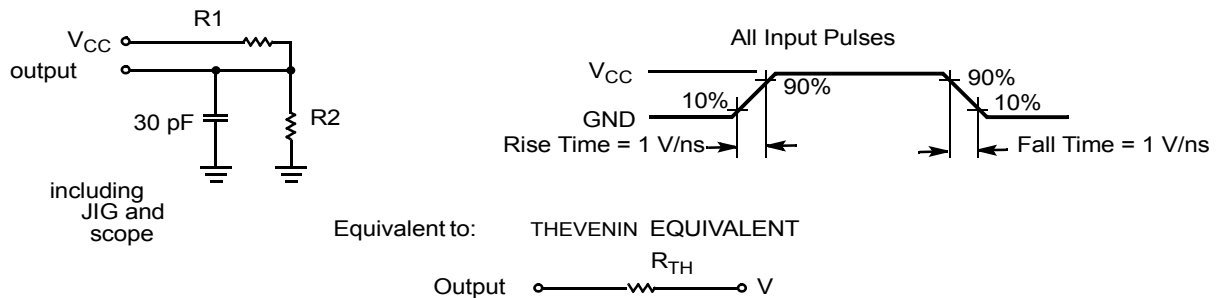
## Capacitance

Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	TSOP I	SOIC	STSOP	Unit
Θ <sub>JA</sub>	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C / W
Θ <sub>JC</sub>	Thermal resistance (Junction to case)		3.42	25.86	3.59	°C / W

Figure 4. AC Test Loads and Waveforms



Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

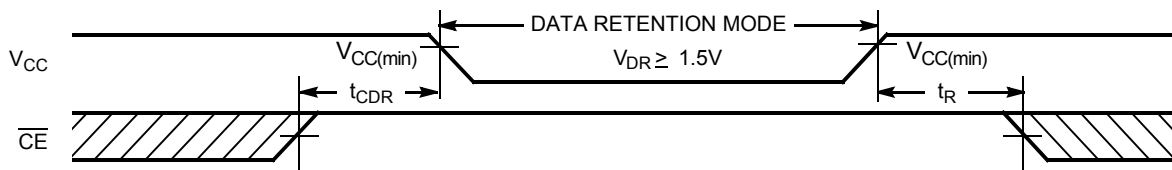
## Data Retention Characteristics

(Over the Operating Range)

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	–	–	V
I <sub>CCDR</sub> <sup>[11]</sup>	Data retention current	V <sub>CC</sub> = 1.5 V, CE <sub>1</sub> ≥ V <sub>CC</sub> – 0.2 V or CE <sub>2</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> ≤ 0.2 V				
		Auto-A	–	–	3	μA
		Auto-E	–	–	30	μA
t <sub>CDR</sub> <sup>[12]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[13]</sup>	Operation recovery time					
		CY62128EV30LL-45	45	–	–	ns
		CY62128EV30LL-55	55	–	–	ns

### Note

9. Tested initially and after any design or process changes that may affect these parameters
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
11. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) must be at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters
13. Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

**Figure 5. Data Retention Waveform<sup>[14]</sup>**


## Switching Characteristics

(Over the Operating Range)

Parameter <sup>[14, 15]</sup>	Description	45 ns (Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	45	–	55	–	ns
$t_{AA}$	Address to data valid	–	45	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[16]</sup>	5	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[16, 17]</sup>	–	18	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[16]</sup>	10	–	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[16, 17]</sup>	–	18	–	20	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-down	–	45	–	55	ns
<b>Write Cycle<sup>[18]</sup></b>						
$t_{WC}$	Write cycle time	45	–	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	40	–	ns
$t_{AW}$	Address setup to write end	35	–	40	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	40	–	ns
$t_{SD}$	Data setup to write end	25	–	25	–	ns
$t_{HD}$	Data Hold from write end	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[16, 17]</sup>	–	18	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[16]</sup>	10	–	10	–	ns

### Notes

14.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" on page 5.
16. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Figure 6. Read Cycle 1 Address transition controlled [20, 21]

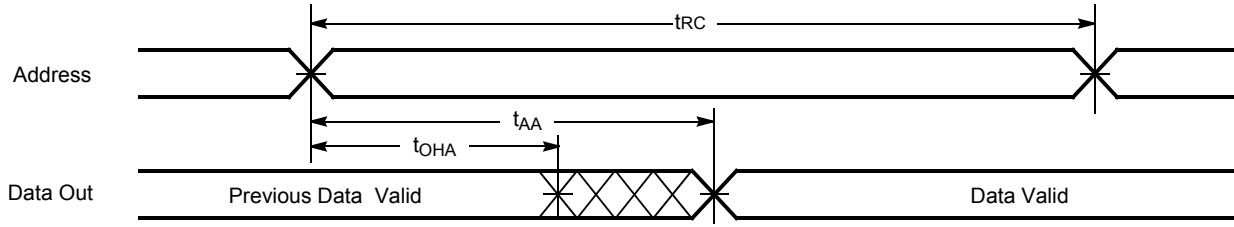


Figure 7. Read Cycle No. 2 OE controlled [21, 22, 23]

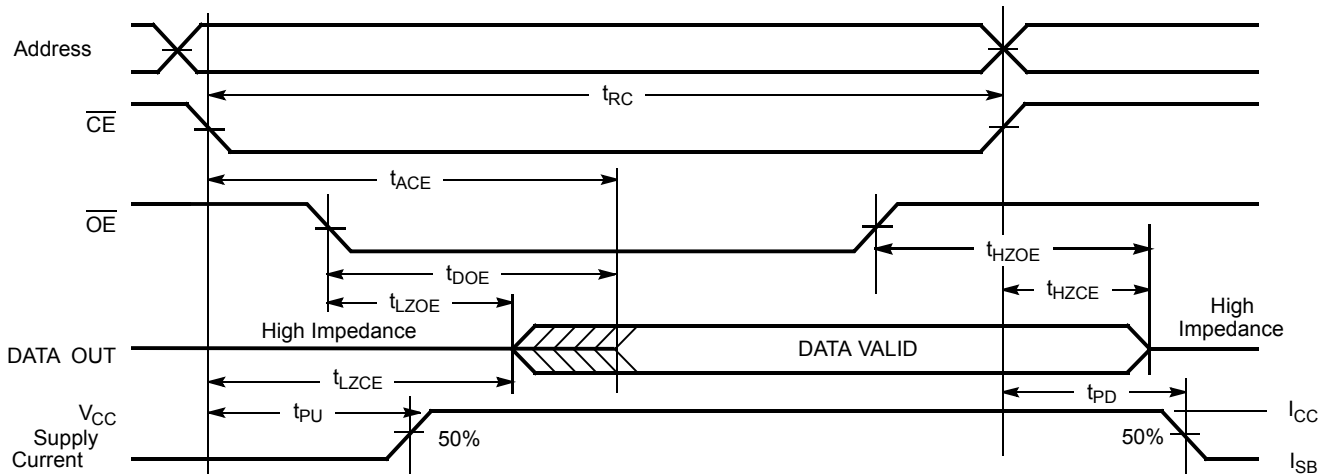
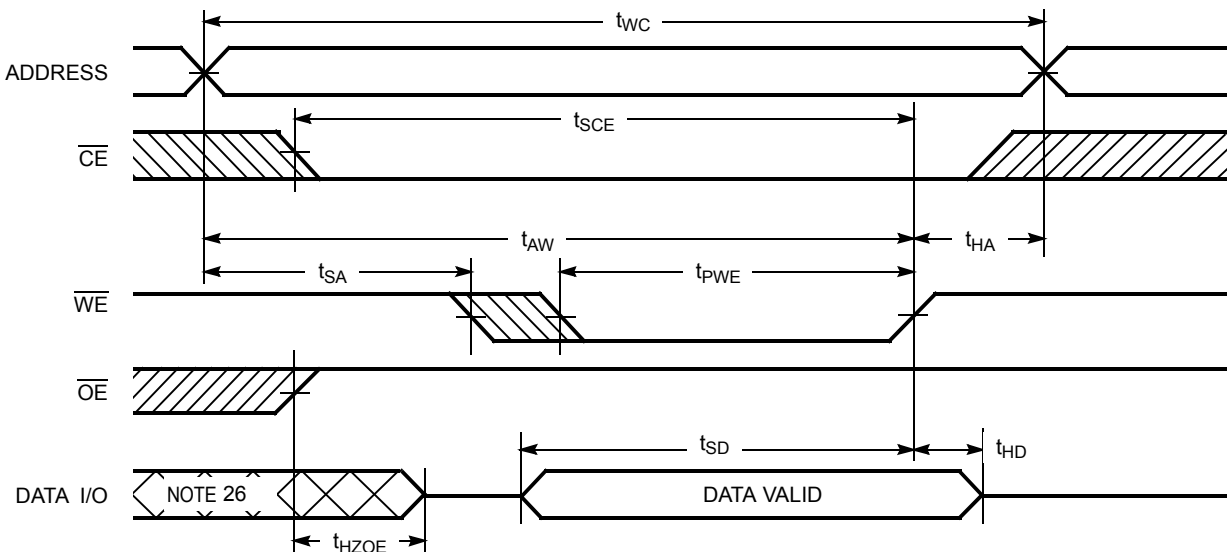


Figure 8. Write Cycle No. 1 WE controlled [19, 22, 24, 25]



**Notes**

- 19. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 20. The device is continuously selected.  $\overline{OE}$ ,  $CE_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 21.  $\overline{WE}$  is HIGH for read cycle.
- 22.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 23. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 24. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 25. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2  $\overline{CE}_1$  or  $\overline{CE}_2$  controlled [27, 28, 29, 30]

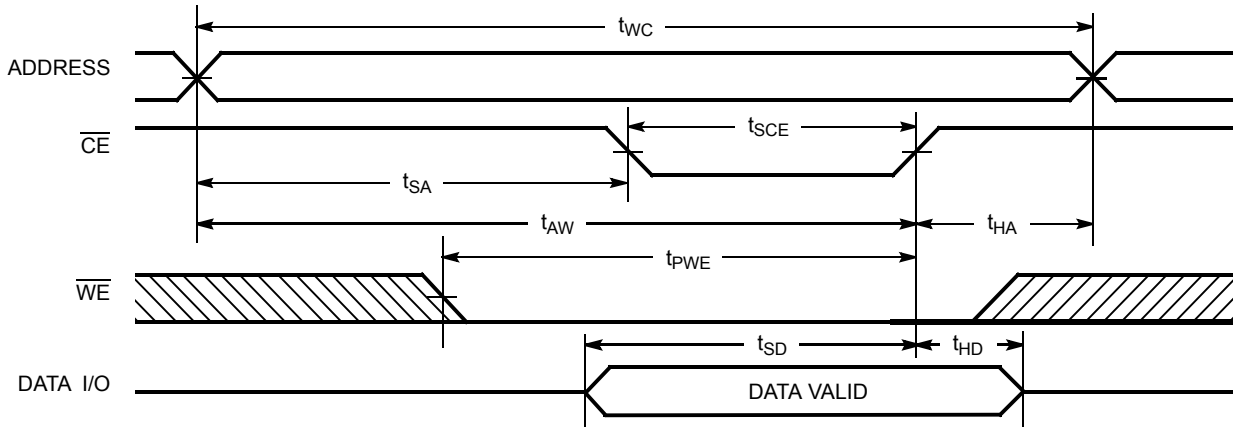
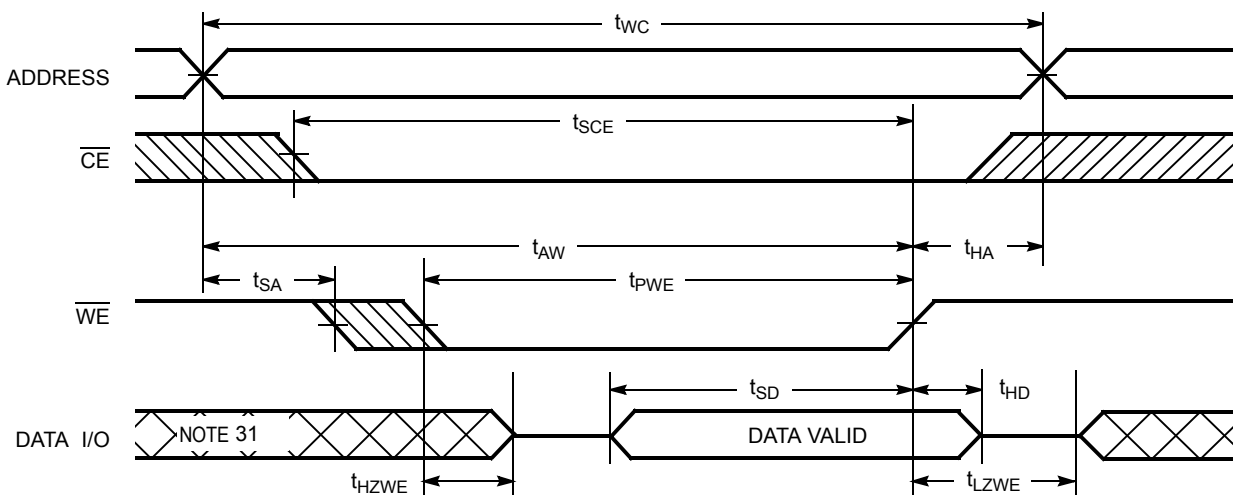


Figure 10. Write Cycle No. 3  $\overline{WE}$  controlled,  $\overline{OE}$  LOW [27, 30]



Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X <sup>[32]</sup>	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	L	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data out	Read	Active ( $I_{CC}$ )
L	H	L	X	Data in	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

Notes

- 27.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . When  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW,  $\overline{CE}$  is HIGH.
- 28. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 29. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 30. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 31. During this period, the I/Os are in output state. Do not apply input signals.
- 32. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



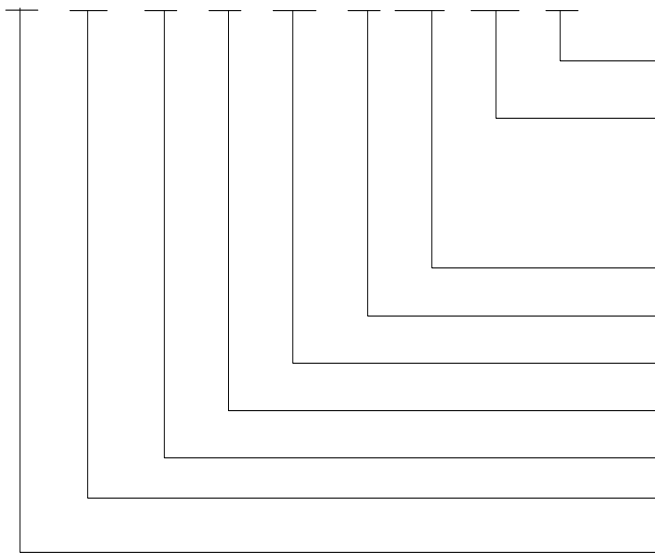
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXA	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-A
	CY62128EV30LL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	
55	CY62128EV30LL-55ZXE	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-E
	CY62128EV30LL-55SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definition

CY 621 2 8E V30 LL 45/55 XXX X



Temperature Grades

E = Automotive-E A: Automotive-A

Package Type:

SXA: 32-pin 450-Mil SOIC(Pb-free)

ZXA: 32-pin TSOP Type I (Pb-free)

ZXE: 32-pin TSOP Type I (Pb-free)

SXE: 32-pin 450-Mil SOIC (Pb-free)

ZAX: 32-pin STSOP (Pb-free)

Speed Grade

Low Power

Voltage Range = 3 V typical

Bus Width = x8

E=Technology = 90 nm

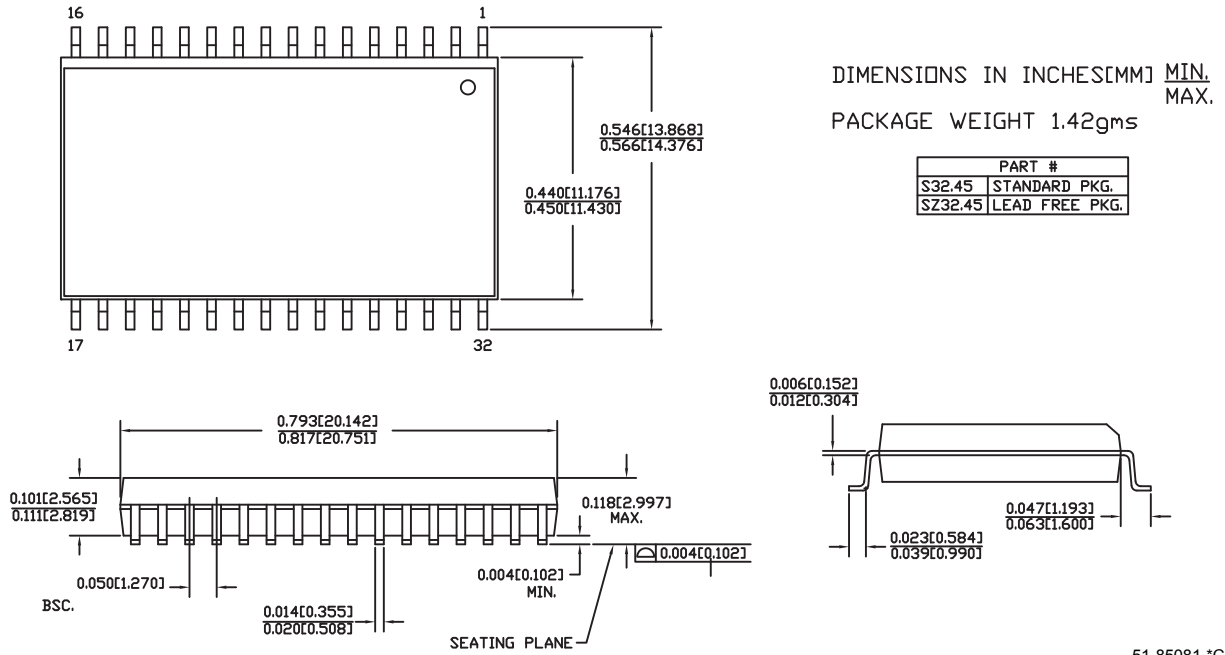
Density = 1 Mbit

MoBL SRAM Family

Company ID: CY = Cypress

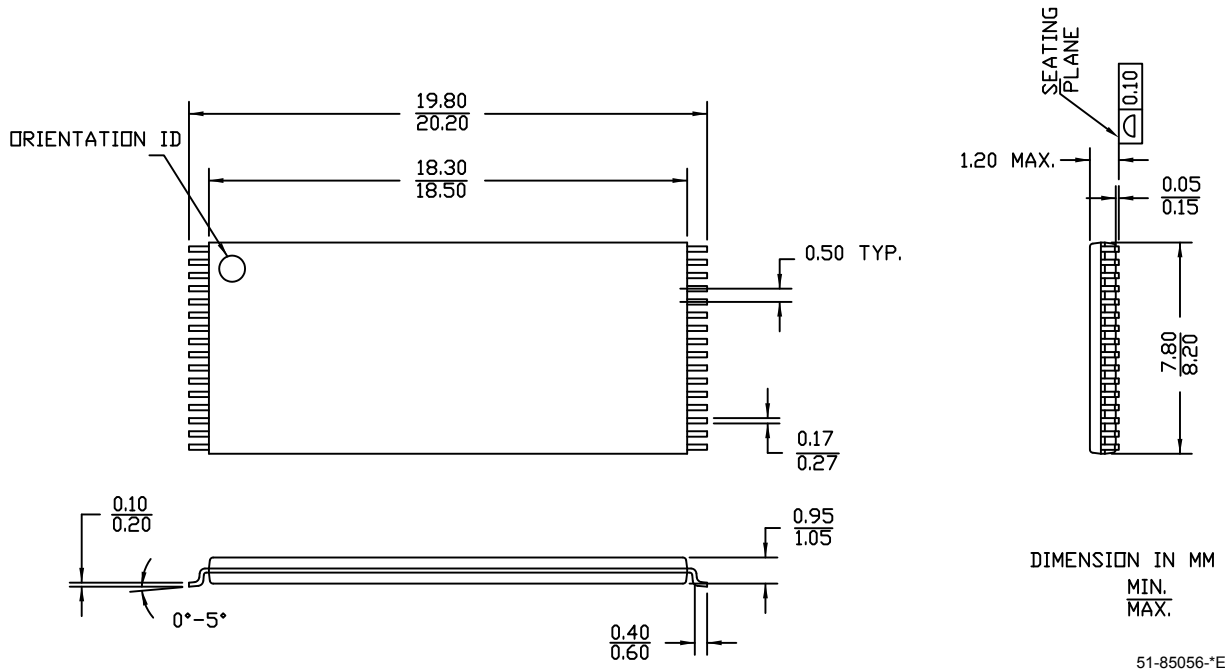
Package Diagrams

Figure 11. 32-Pin (450 Mil) Molded SOIC, 51-85081



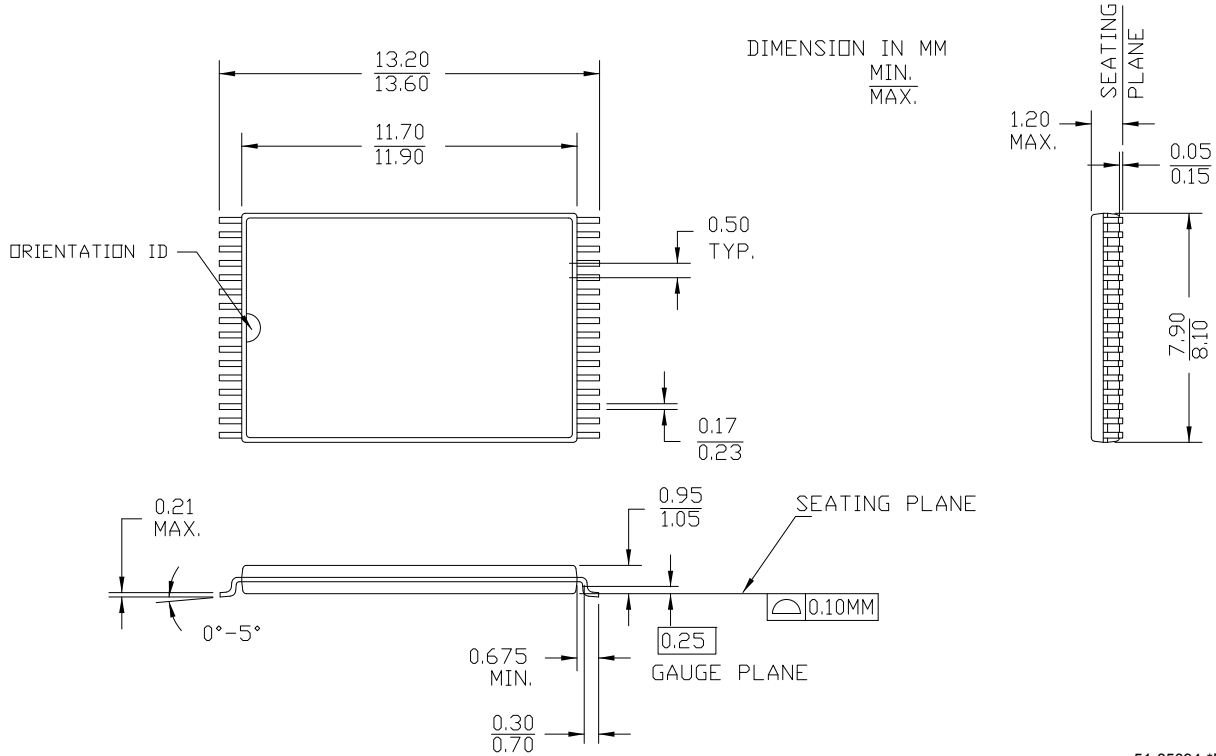
Package Diagrams (continued)

Figure 12. 32-Pin Thin Small Outline Package Type I (8 x 20 mm), 51-85056



**Package Diagrams** (continued)

**Figure 13. 32-Pin Shrunken Thin Small Outline Package (8 x 13.4 mm), 51-85094**



51-85094-\*E

**Acronyms**

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

## Document History Page

Document Title: CY62128EV30 MoBL <sup>®</sup> Automotive 1-Mbit (128K x 8) Static RAM				
Document Number: 001-65528				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	3115909	01/06/2011	RAME	New Datasheet for Automotive SRAM parts. Created separate datasheet for Automotive SRAM parts from Document no. 38-05579 Rev. *H

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/Rf	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

---

© Cypress Semiconductor Corporation, 2004-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.