CY62128EV30 MoBL® Automotive

1-Mbit (128K x 8) Static RAM

Features

- Very high-speed: 45 ns
- Temperature ranges:
  - Automotive-A: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 32-pin small outline integrated circuit (SOIC), 32-pin thin small outline package (TSOP I), and 32-pin STSOP packages

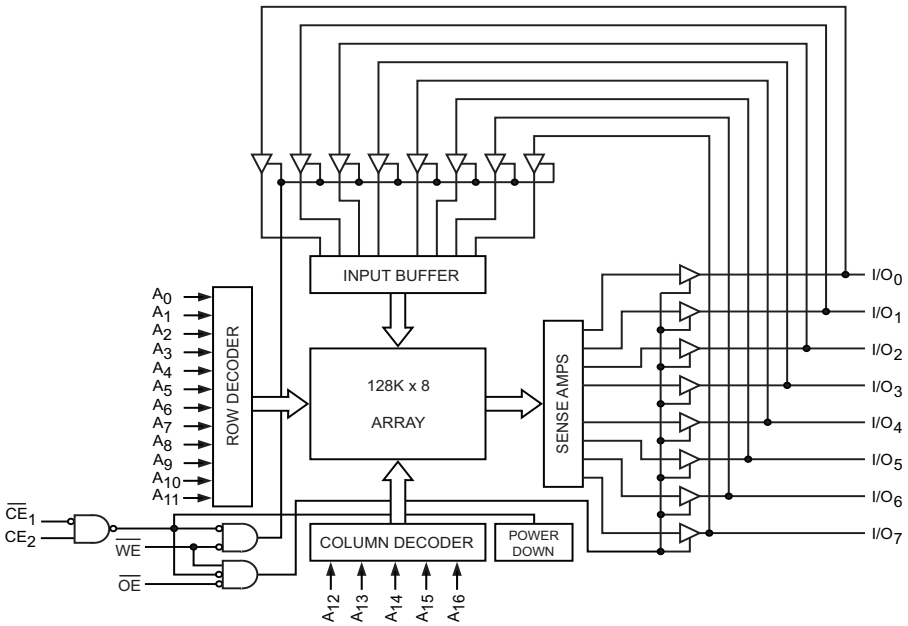
Functional Description

The CY62128EV30[1] is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The eight input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins is then written into the location specified on the Address pin (A_0 through A_{16}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

Logic Block Diagram



Note
1. For best practice recommendations, refer to the Cypress application note *"System Design Guidelines"* at http://www.cypress.com.

Contents

Pin Configuration

Figure 1. 32-Pin STSOP [2]

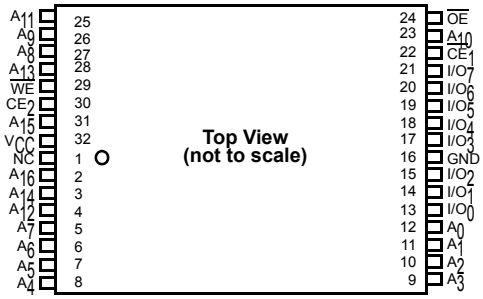


Figure 2. 32-Pin TSOP I [2]

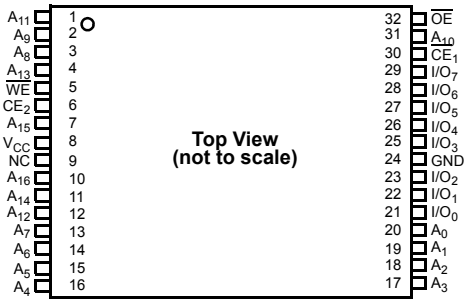


Figure 3. 32-Pin SOIC [2]

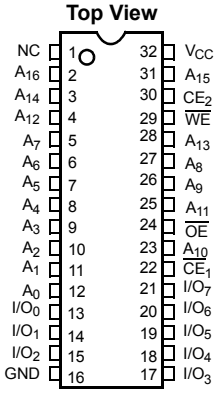


Table 1. Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62128EV30LL	Auto-A	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4
CY62128EV30LL	Auto-E	2.2	3.0	3.6	55	1.3	4.0	11	35	1	30

Table 2. Pin Definitions

Input	**A_0–A_{16}**. Address inputs
Input/output	**I/O_0–I/O_7**. Data lines. Used as input or output lines depending on operation
Input/control	**$\overline{WE}$**. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	**$\overline{CE_1}$**. Chip Enable 1, Active LOW.
Input/control	**CE_2**. Chip Enable 2, Active HIGH.
Input/control	**$\overline{OE}$**. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	**GND**. Ground for the device
Power supply	**V_{CC}**. Power supply for the device

Notes
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z state[4, 5] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage[4,5].....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (MIL-STD-883, Method 3015)

Latch up current.....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62128EV30LL	Auto-A	–40 °C to +85 °C	2.2 V to 3.6 V
	Auto-E	–40 °C to +125 °C	

Electrical Characteristics

(Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ[7]	Max	Min	Typ[7]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA, $V_{CC} \le$ 2.70 V	2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \ge$ 2.70 V	2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	–	–	0.4	–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \ge$ 2.70 V	–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2. V	1.8	–	V_{CC} + 0.3V	1.8	–	V_{CC} + 0.3V	V
		V_{CC}= 2.7 V to 3.6 V	2.2	–	V_{CC} + 0.3V	2.2	–	V_{CC} + 0.3V	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V	–0.3	–	0.6	–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V	–0.3	–	0.8	–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\le V_I \le V_{CC}$	–1	–	+1	–4	–	+4	µA
I_{OZ}	Output leakage current	GND $\le V_O \le V_{CC}$, output disabled	–1	–	+1	–4	–	+4	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels	–	11	16	–	11	35	mA
		f = 1 MHz; V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels	–	1.3	2.0	–	1.3	4.0	mA
I_{SB1}	Automatic CE power-down current — CMOS inputs	$\overline{CE_1} \ge V_{CC}$–0.2 V, CE_2 < 0.2 V $V_{IN} \ge V_{CC}$–0.2 V, $V_{IN} \le$ 0.2 V) f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V	–	1	4	–	1	35	µA
I_{SB2}[8]	Automatic CE power-down current — CMOS inputs	$\overline{CE_1} \ge V_{CC}$ – 0.2 V, CE_2 < 0.2 V $V_{IN} \ge V_{CC}$ – 0.2 V or V_{IN} < 0.2 V, f = 0, V_{CC} = 3.60 V	–	1	4	–	1	30	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC}+0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C
8. Chip enables ($\overline{CE_1}$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

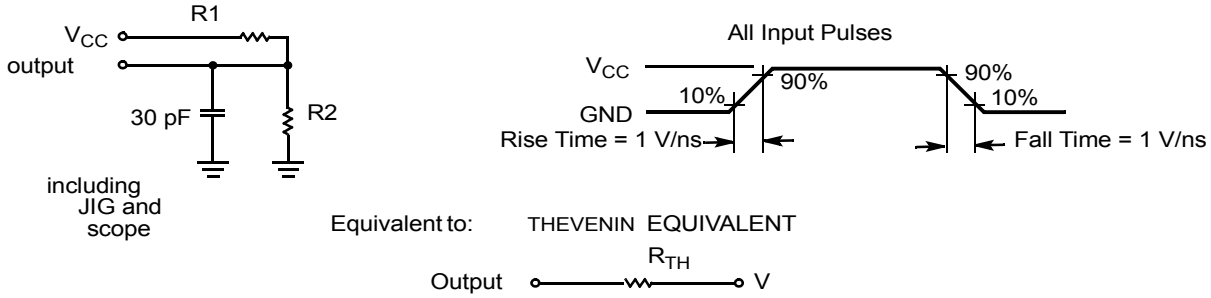
Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[9]	Description	Test Conditions	TSOP I	SOIC	STSOP	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C / W
Θ_{JC}	Thermal resistance (Junction to case)		3.42	25.86	3.59	°C / W

Figure 4. AC Test Loads and Waveforms



Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

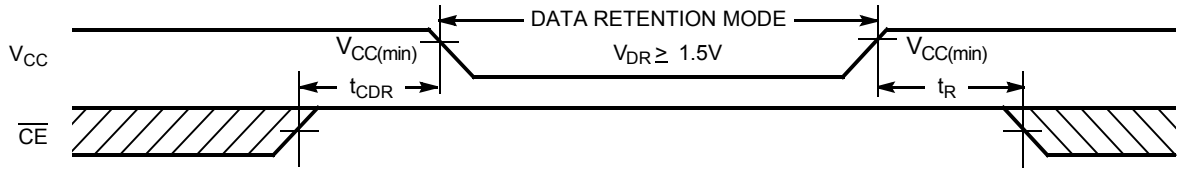
(Over the Operating Range)

Parameter	Description	Conditions		Min	Typ[10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[11]	Data retention current	$\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Auto-A	–	–	3	µA
			Auto-E	–	–	30	µA
t_{CDR}[12]	Chip deselect to data retention time			0	–	–	ns
t_R[13]	Operation recovery time		CY62128EV30LL-45	45	–	–	ns
			CY62128EV30LL-55	55			

Note

9. Tested initially and after any design or process changes that may affect these parameters
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enables ($\overline{CE_1}$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters
13. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Figure 5. Data Retention Waveform [14]



Switching Characteristics

(Over the Operating Range)

Parameter[14, 15]	Description	45 ns (Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[16]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16,17]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[16]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[16, 17]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power-down	–	45	–	55	ns
Write Cycle[18]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data Hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[16, 17]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[16]	10	–	10	–	ns

Notes

14. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 5.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 6. Read Cycle 1 Address transition controlled [20, 21]

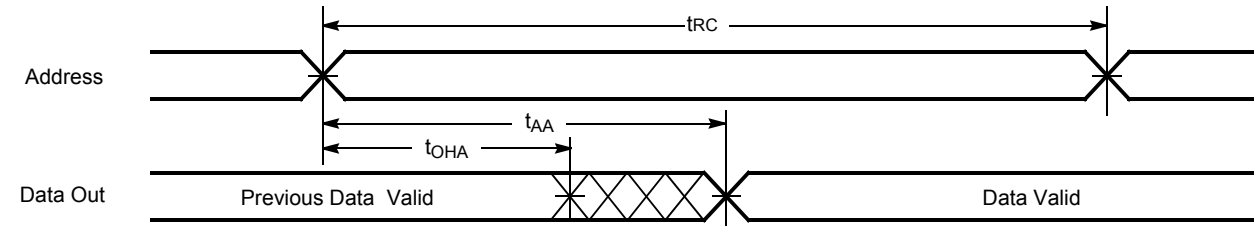


Figure 7. Read Cycle No. 2 $\overline{OE}$ controlled [21, 22, 23]

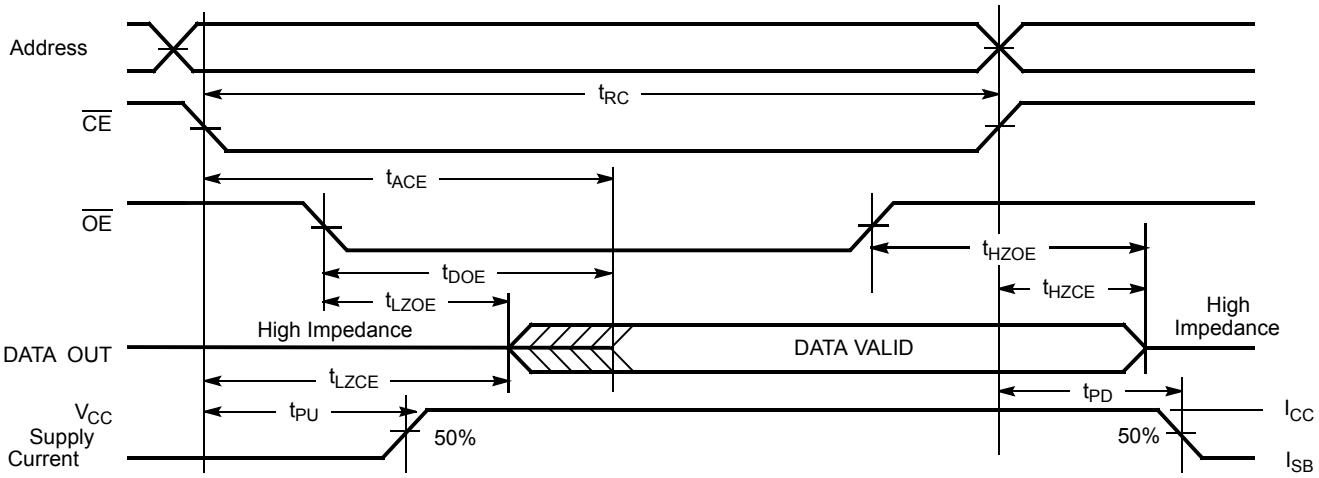
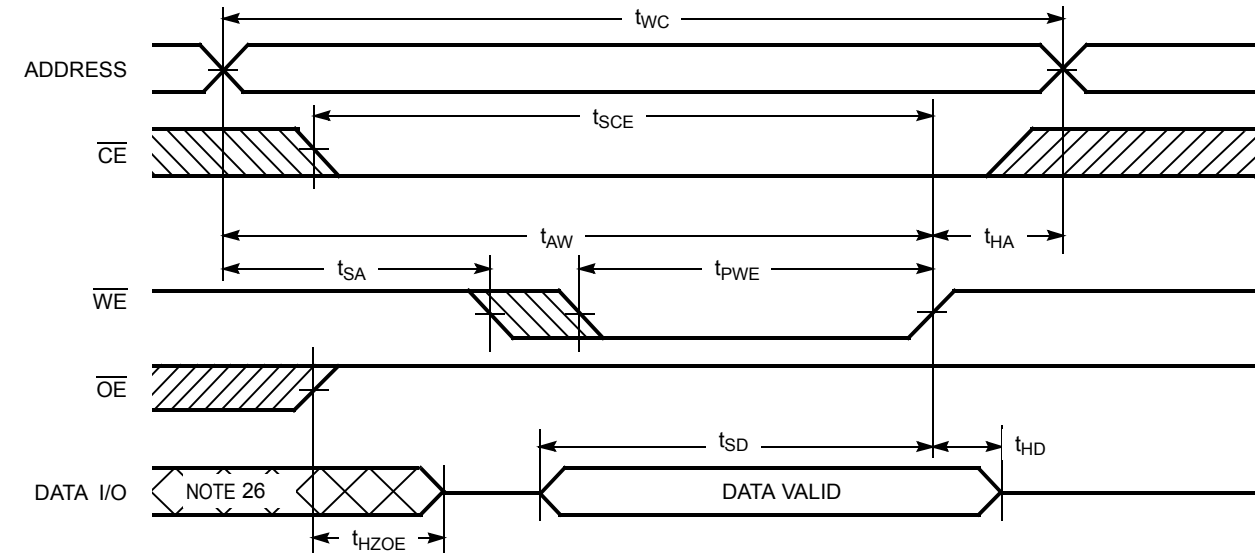


Figure 8. Write Cycle No. 1 $\overline{WE}$ controlled [19, 22, 24, 25]



Notes

19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
21. $\overline{WE}$ is HIGH for read cycle.
22. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
23. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 $\overline{CE1}$ or CE2 controlled [27, 28, 29, 30]

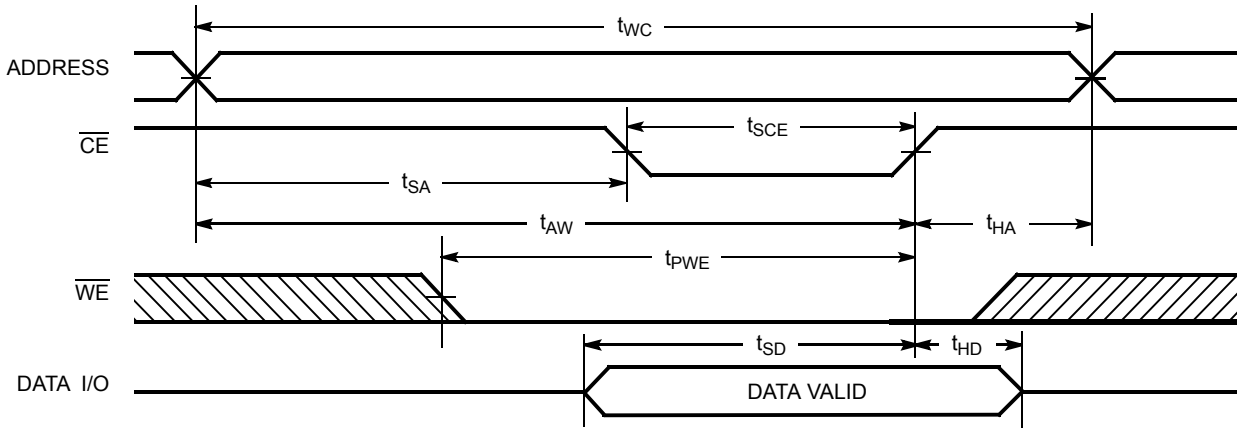
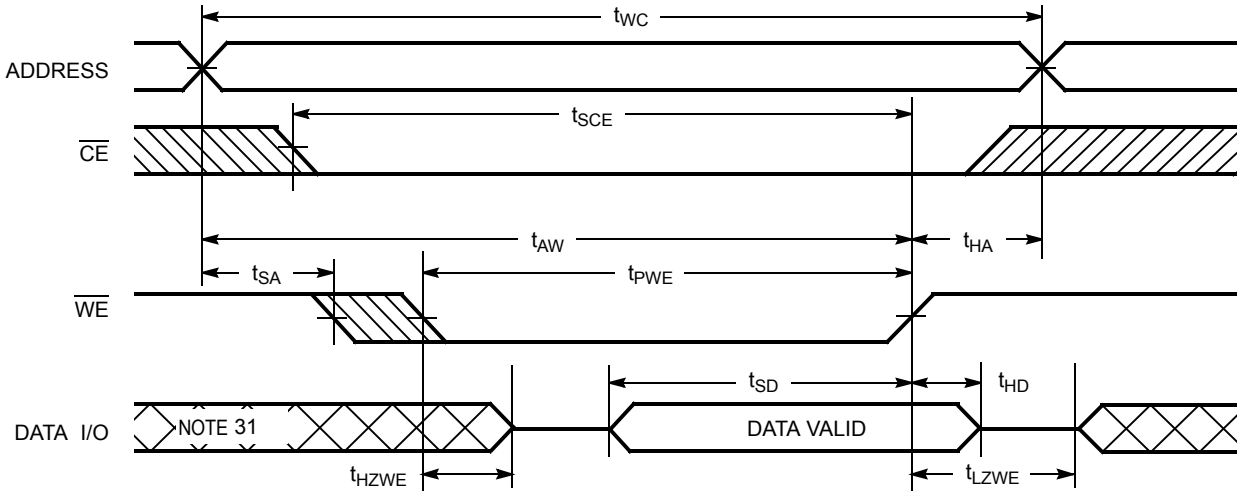


Figure 10. Write Cycle No. 3 $\overline{WE}$ controlled, $\overline{OE}$ LOW [27, 30]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X[32]	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

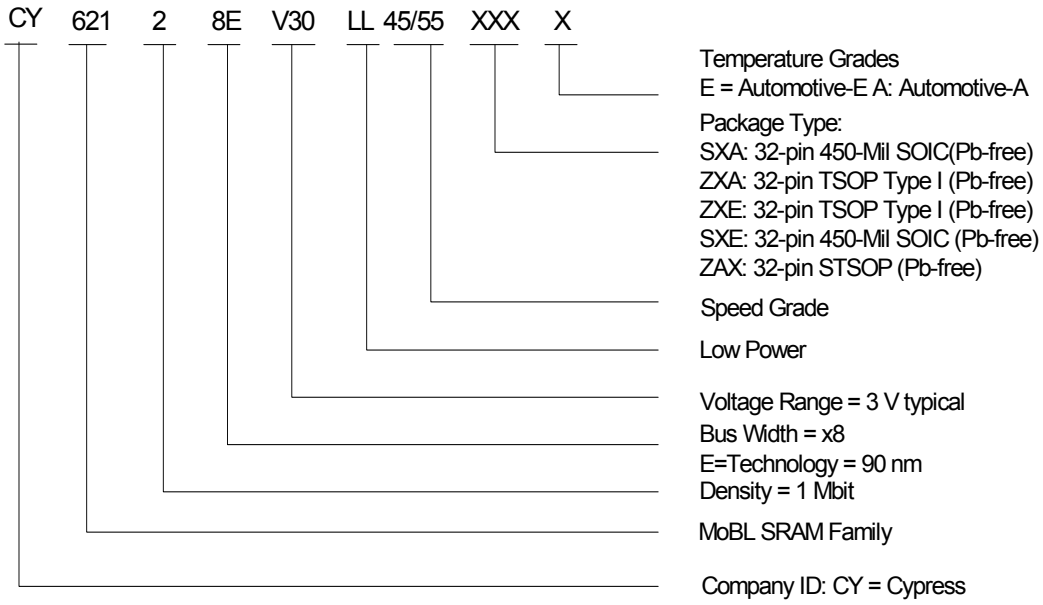
Notes
27. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH
28. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
29. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
30. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
31. During this period, the I/Os are in output state. Do not apply input signals.
32. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXA	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-A
	CY62128EV30LL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	
55	CY62128EV30LL-55ZXE	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-E
	CY62128EV30LL-55SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	

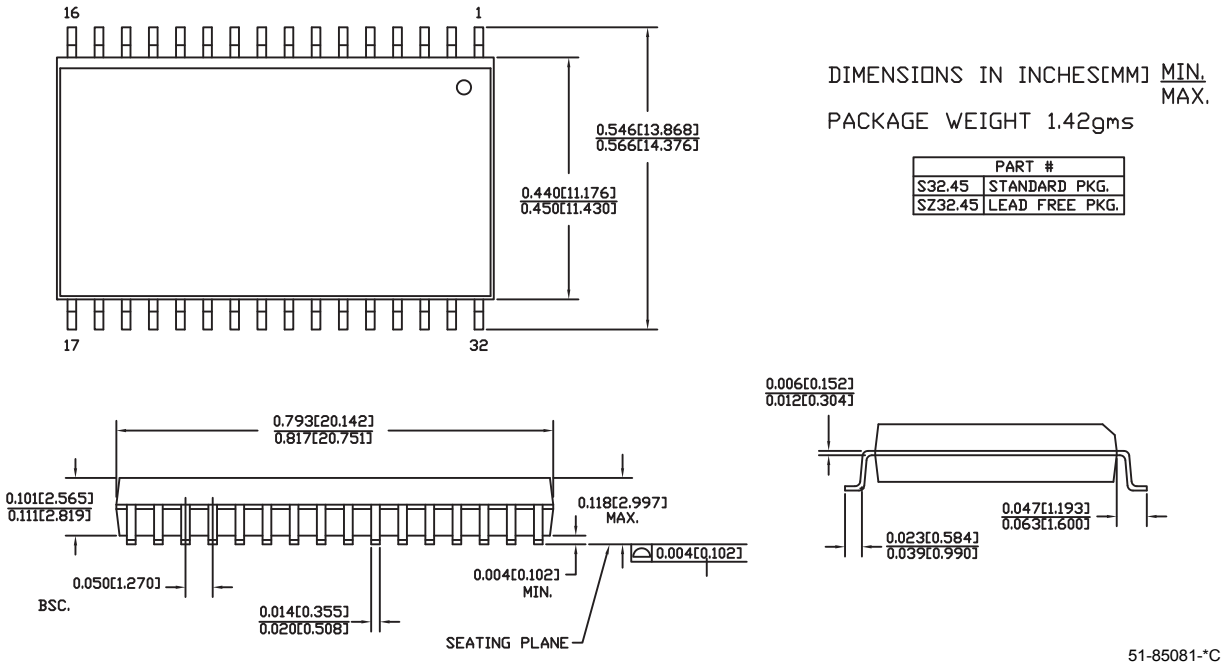
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definition



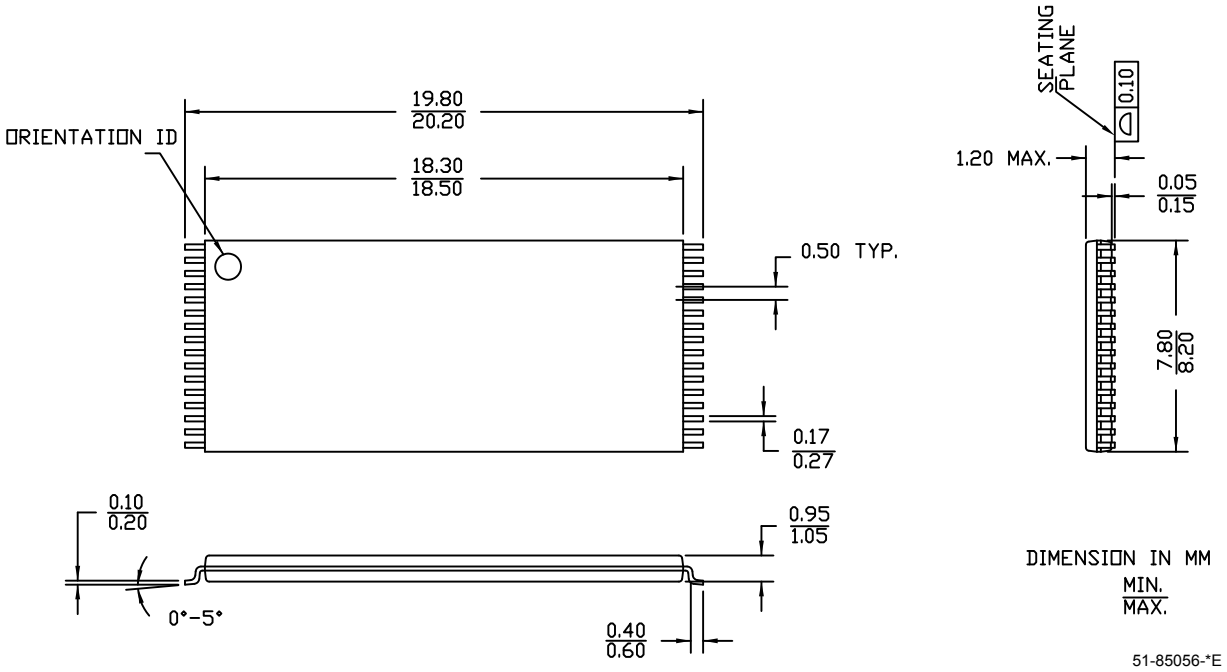
Package Diagrams

Figure 11. 32-Pin (450 Mil) Molded SOIC, 51-85081



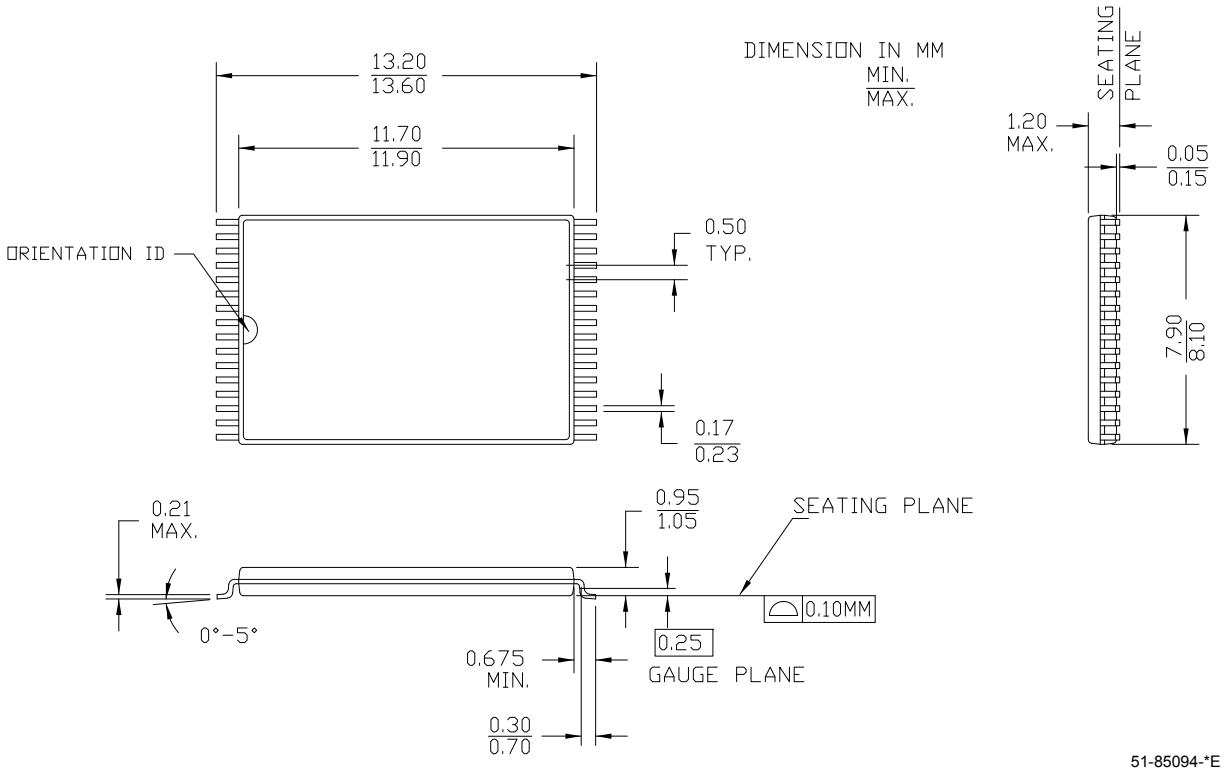
Package Diagrams (continued)

Figure 12. 32-Pin Thin Small Outline Package Type I (8 x 20 mm), 51-85056



Package Diagrams (continued)

Figure 13. 32-Pin Shrunk Thin Small Outline Package (8 x 13.4 mm), 51-85094



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62128EV30 MoBL® Automotive 1-Mbit (128K x 8) Static RAM Document Number: 001-65528				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3115909	01/06/2011	RAME	New Datasheet for Automotive SRAM parts. Created separate datasheet for Automotive SRAM parts from Document no. 38-05579 Rev. *H

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5