

# Intel® 5520 and Intel® 5500 Chipsets

Thermal/Mechanical Design Guidelines

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*November 2009*

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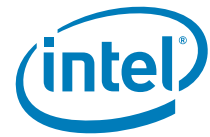
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## Revision History

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Document Number	Revision Number	Description	Date
321330	001	<ul style="list-style-type: none"><li>Public release</li></ul>	March 2009
321330	002	<ul style="list-style-type: none"><li>Updated Table 3-1, post Si idle power from 8W to 10W</li><li>Updated supplier part number information in Appendix A</li></ul>	April 2009
321330	003	<ul style="list-style-type: none"><li>Updated Table 3-1, post Si idle power from 10W to 13W</li></ul>	November 2009

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# 1 Introduction

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As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® 5520 and Intel® 5500 Chipsets.
- Describe reference thermal solutions that meet the specifications of the Intel® 5520 and Intel® 5500 Chipsets.

Properly designed thermal solutions provide adequate cooling to maintain the Intel 5520 and Intel 5500 chipsets case temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining Intel 5520 and Intel 5500 chipsets' case temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the IOH. Operation outside the functional limits can cause data corruption or permanent damage to the component.

The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

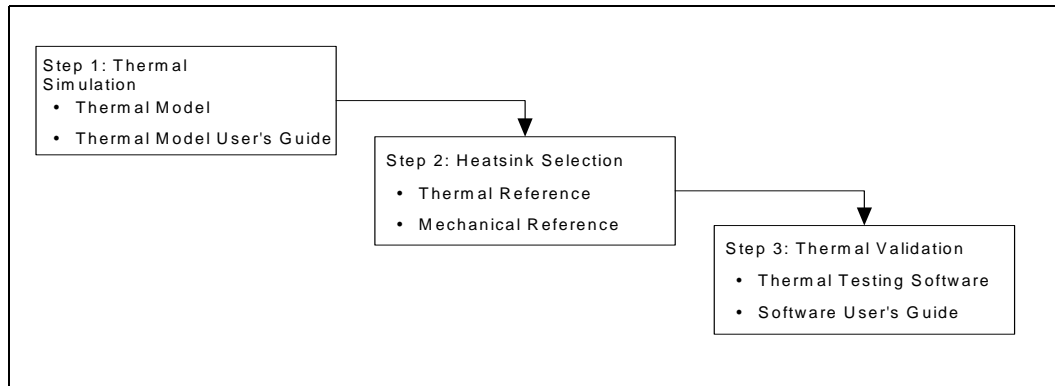
This document addresses thermal design and specifications for the Intel 5520 and Intel 5500 chipsets component only. For thermal design information on other chipset components, refer to the respective component TMDG. For the ICH9, refer to the *Intel® I/O Controller Hub 9 (ICH9) Family Thermal and Mechanical Design Guidelines*.

**Note:** Unless otherwise specified, the term "IOH" refers to the Intel® 5520 and Intel® 5500 Chipsets.

## 1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. [Figure 1-1](#) illustrates the design process implicit to this document and the tools appropriate for each step.

**Figure 1-1. Thermal Design Process**



## 1.2 Definition of Terms

FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
BLT	Bond Line Thickness. Final settled thickness of the thermal interface material after installation of heatsink.
Intel <sup>®</sup> QuickPath Interconnect	The Physical layer of Intel <sup>®</sup> QuickPath Interconnect is a link based interconnect specification for Intel processors, chipset and I/O bridge components.
IOH	Input Output Hub. The IO Controller Hub component that contains the Intel <sup>®</sup> QuickPath technology to the processor, and PCI Express* interface. It communicates with the ICH9 over a proprietary interconnect called the Enterprise South Bridge Interface (ESI).
ICH9	I/O Controller Hub 9.
$T_{case\_max}$	Die temperature allowed. This temperature is measured at the geometric center of the top of the die.
TDP	Thermal design power. Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the IOH can dissipate.





### 1.3 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Title	Document #	Location
Intel® 5520 and Intel® 5500 Chipsets Datasheet	321328	www.intel.com
Intel® 5520 and Intel® 5500 Chipset Specification Update	321329	www.intel.com
Various system thermal design suggestions ( <a href="http://www.formfactors.org">http://www.formfactors.org</a> )		

**Note:** Unless otherwise specified, these documents are available through your Intel field sales representative. Some documents may not be available at this time.

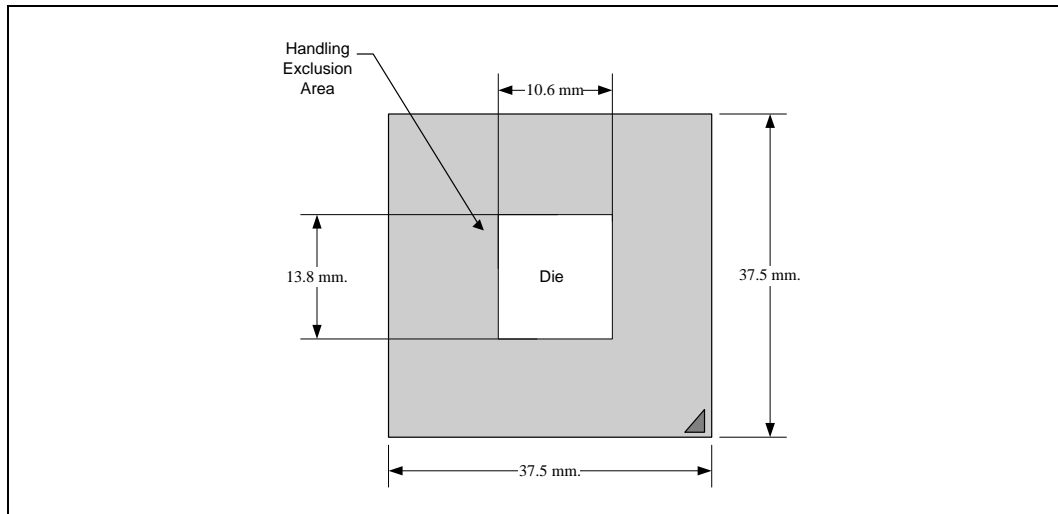
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# 2 Packaging Technology

The Intel 5520 and Intel 5500 chipsets component uses a 37.5 mm, 8-layer flip chip ball grid array (FC-BGA) package (see Figure 2-1, Figure 2-2, and Figure 2-3). For information on the ICH9 package, refer to the *Intel® I/O Controller Hub 9 (ICH9) Family Thermal and Mechanical Design Guidelines*.

**Figure 2-1. IOH Package Dimensions (Top View)**



**Figure 2-2. IOH Package Dimensions (Side View)**

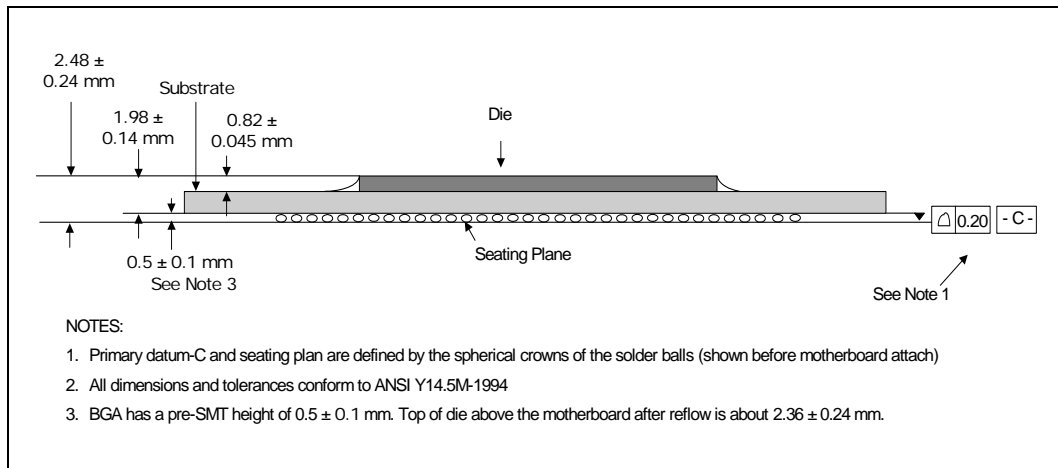
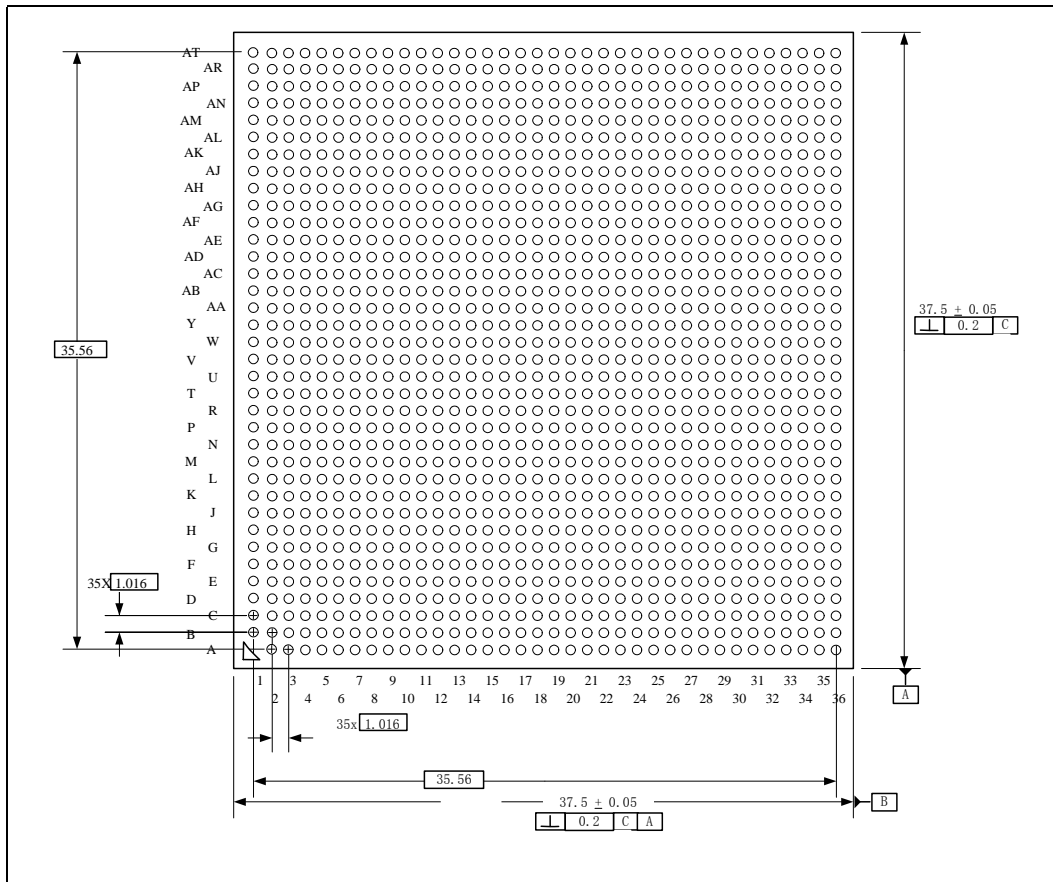


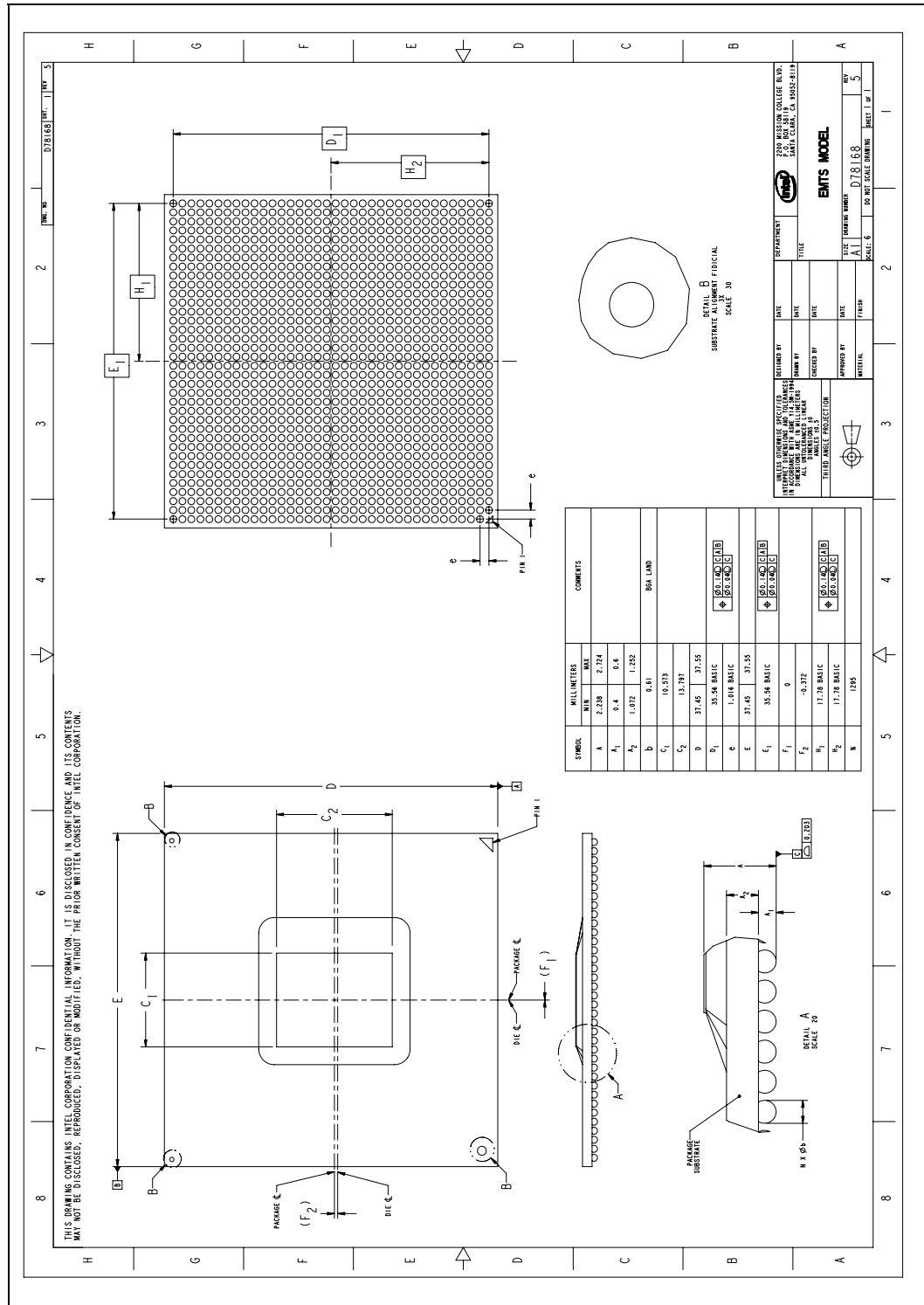
Figure 2-3. IOH Package Dimensions (Bottom View)



- Notes:**
1. All dimensions are in millimeters.
  2. All dimensions and tolerances conform to ANSI Y14.5M-1994.

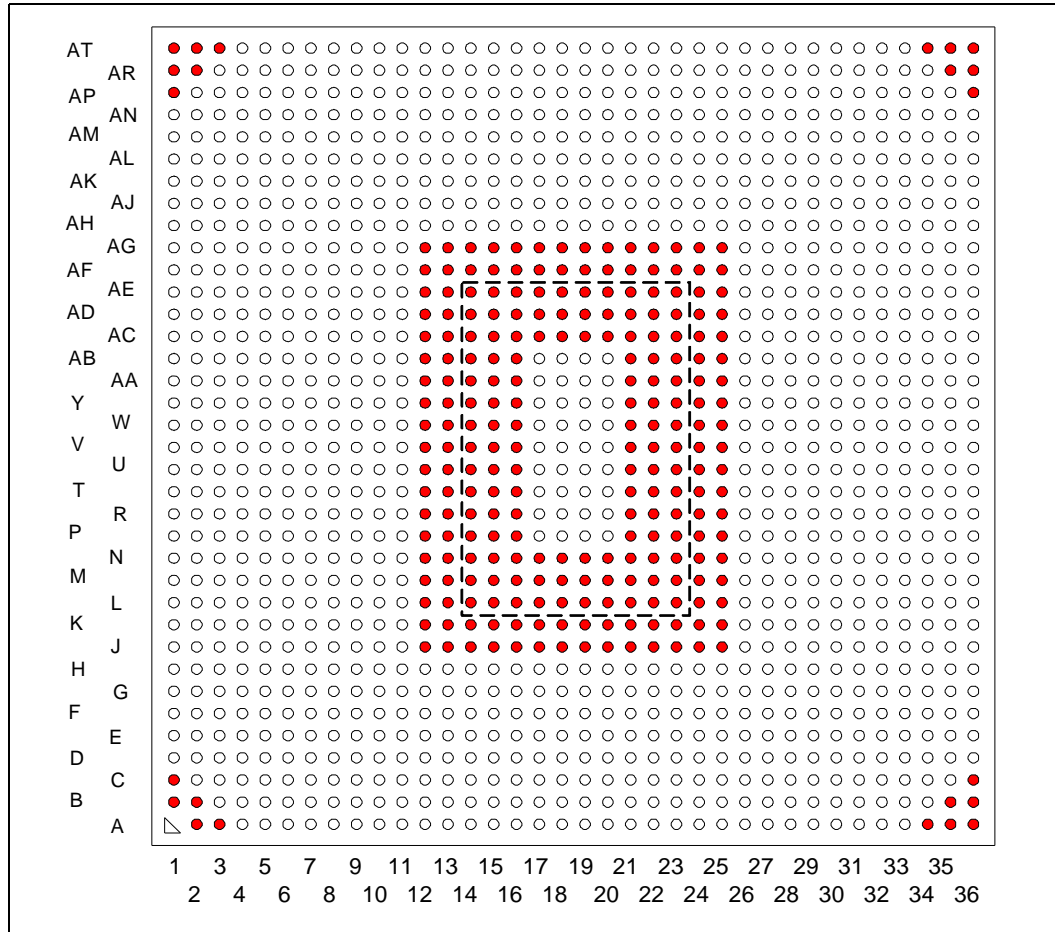


Figure 2-4. IOH Package Drawing



## 2.1 Non-Critical to Function Solder Joints

Figure 2-5. Non-Critical to Function Solder Joints



Intel has defined selected solder joints of the IOH as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The IOH signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. [Figure 2-5](#) identifies the NCTF solder joints of the IOH package.



## 2.2 Package Mechanical Requirements

The Intel 5520 and Intel 5500 chipsets package has a bare die that is capable of sustaining a maximum static normal load of 15 lbf (67N). These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition.

**Note:** The heatsink attach solutions must not induce continuous stress to the IOH package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.

**Note:** These specifications apply to uniform compressive loading in a direction perpendicular to the die top surface.

**Note:** These specifications are based on limited testing for design characterization. Loading limits are for the package only.

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# 3 Thermal Specifications

## 3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the IOH component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the target power level to which the thermal solutions should be designed. TDP is not the maximum power that the IOH can dissipate.

For TDP specifications, see [Table 3-1](#) for the Intel 5520 and Intel 5500 chipsets. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solution. Intel recommends that system designers plan for a heatsink with Intel 5520 and Intel 5500 chipsets.

## 3.2 Case Temperature

To ensure proper operation and reliability of Intel 5520 and Intel 5500 chipsets, the case temperature must comply with the thermal profile as specified in [Table 3-2](#). System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to [Chapter 5](#) for guidelines on accurately measuring package case temperatures.

**Table 3-1. Intel® 5520 and Intel® 5500 Chipsets Thermal Design Power**

Product	TDP	Idle	Notes
Intel® 5520 and Intel® 5500 Chipsets	27.1W	13W	1, 2, 3, 4

**Notes:**

1. These specifications are based on post-silicon measurement and subject to change.
2. TDP assumes the following configuration: 36 PCIe\* Gen 2.0 and ESI link with ICH9 and the Intel® QuickPath Interconnect operating at 6.4 GT/s.
3. The Idle Power for the IOH is 13 W, please refer to the Intel® 5520 and Intel® 5500 Chipsets NDA Specification Update (Erratum 62) for more details.
4. The idle power assumes the case temperature is at or below 95°C.



Table 3-2. Intel® 5520 and Intel® 5500 Chipsets Thermal Specification

Parameter	Value
Tcase_max	95.1°C
Tcase_min	5°C
Tcontrol	92
Target Psi_ca	1.41°C/W Tla=53°C Tall HS 1.92°C/W Tla=43°C Short HS

**Notes:**

1. Refer to the *Intel® 5520 and Intel® 5500 Chipsets Datasheet* for thermal management mechanism and Tcontrol usage.
2. TSFSC = TSTHRHI - IOH Thermal sensor reading
3. Tcontrol = TSTHRHI - Threshold TSFSC
4. TSFSC: The "head-room" between the die temperature and the maximum allowable die temperature is reported in degrees Centigrade through TSFSC. When TSFSC goes to zero, it throttles.
5. TSTHRHI is used to determine throttling point as the temperature increases, and the threshold TSFSC is an offset between the throttling point and the fan speed control point.
6. Threshold TSFSC value is 3.
7. The Tcontrol of 92 is a conceptual threshold value to be compared against the thermal sensor reading.
8. When TSFSC > 3, which means IOH thermal sensor reading is less than Tcontrol of 92, system can run under acoustic condition.
9. When TSFSC <=3, which means IOH thermal sensor reading is larger than Tcontrol, The fans must increase as necessary to try to maintain the TSFSC reading >=3. In the cases where maximum fan speed is reached and TSFSC cannot be maintained at >=3, the Tcase must still be maintained to be less than or equal to Tcase\_max.
10. Target Psi\_ca for tall HS is assuming a Tla of 53 °C, target Psi\_ca for short HS is assuming a Tla of 43°C. Please identify your specific Psi\_ca based on your system's high fan speed Boundary Condition.
11. The reference Tall Heatsink is described in [Chapter 6, "Reference Thermal Solution"](#) and the reference Short Heatsink is described in [Chapter 7, "Reference Thermal Solution 2"](#).

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## 4 Thermal Simulation

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Intel provides thermal simulation models of Intel 5520 and Intel 5500 chipsets and associated users' guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOTHERM\* (version 5.1 or higher) by Flomerics, Inc. Contact your Intel field sales representative to order the thermal models and users' guides.

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# 5 Thermal Metrology

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The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the IOH die temperatures. [Section 5.1](#) provides guidelines on how to accurately measure the IOH die temperatures. [Section 5.2](#) contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in [Figure 5-1](#) offers useful guidelines for thermal performance and evaluation.

## 5.1 Die Temperature Measurements

To ensure functionality and reliability, the  $T_{\text{case}}$  of the IOH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in [Table 3-1](#). The surface temperature at the geometric center of the die corresponds to  $T_{\text{case}}$ . Measuring  $T_{\text{case}}$  requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the 0° thermocouple attach approach is recommended.

### 5.1.1 Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see [Figure 5-2](#)).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see [Figure 5-3](#)).
6. Attach heatsink assembly to the IOH and route thermocouple wires out through the milled slot.

Figure 5-1. Thermal Solution Decision Flow Chart

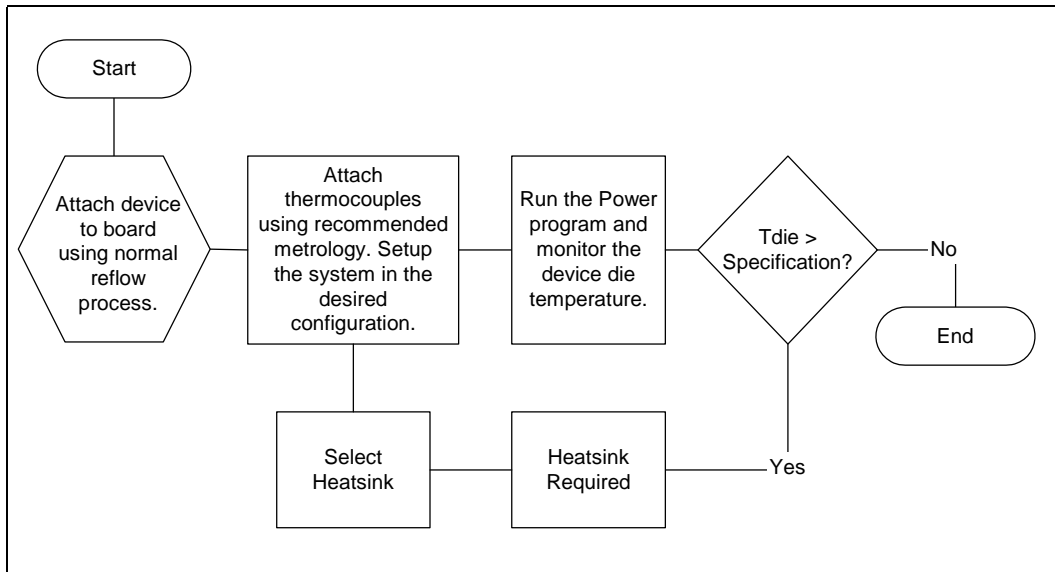
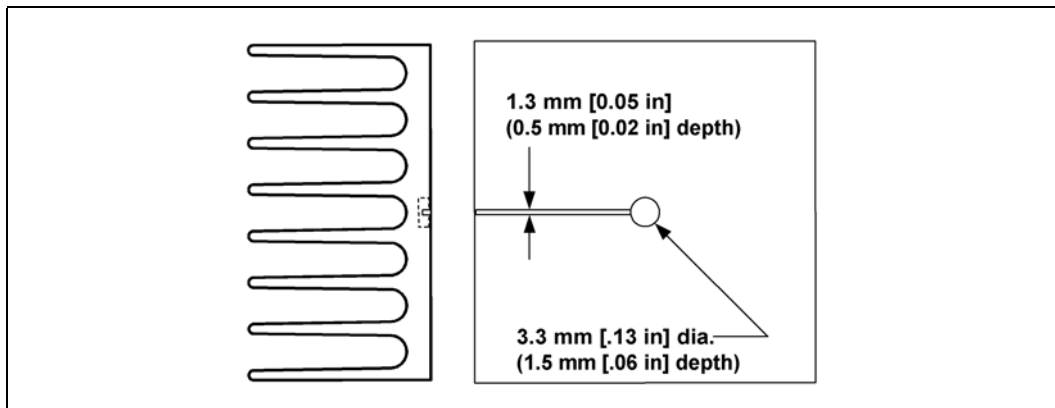
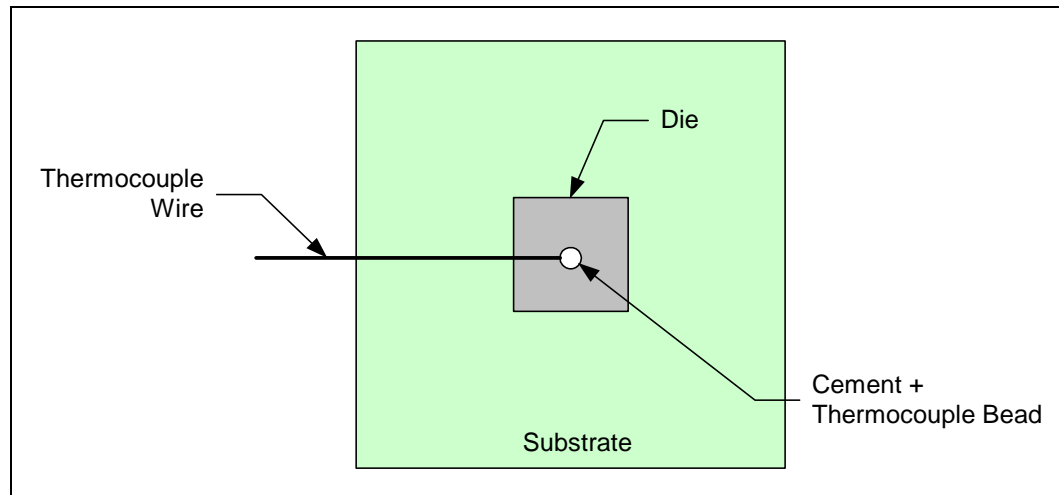


Figure 5-2. Zero Degree Angle Attach Heatsink Modifications



NOTE: Not to scale.

**Figure 5-3. Zero Degree Angle Attach Methodology (Top View)**



**NOTE:** Not to scale.

## 5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on Intel 5520 and Intel 5500 chipsets when used in conjunction with the Intel® Xeon® processor 5500 series. The combination of the above mentioned processor(s) and the higher bandwidth capability of Intel 5520 and Intel 5500 chipsets enable higher levels of system performance. To assess the thermal performance of the chipset thermal solution under “worst case realistic application” conditions, Intel is developing a software utility that operate the chipset at near worst-case thermal power dissipation.

The power simulation software being developed should only be used to test thermal solutions at or near the thermal design power. Figure 5-1 shows a decision flowchart for determining thermal solution needs. Real world applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, please refer to each component's datasheet for the ICC (max power supply current) specification. Contact your Intel field sales representative to order the software and the user's guide.

**Note:** To dissipate Intel 5520 and Intel 5500 chipsets at or near TDP, some PCIe test card with high I/O traffic might be needed. Contact your Intel field sales representative for more detail information.

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## 6 Reference Thermal Solution

Intel has developed reference thermal solutions to meet the cooling needs of the Intel 5520 and Intel 5500 chipsets under operating environments and specifications defined in this document. This section describes the overall requirements for the tall torsional clip heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions depending on your specific system local-ambient operating conditions. For information on the ICH9, refer to thermal specification in the *Intel® I/O Controller Hub 9 (ICH9) Family Thermal and Mechanical Design Guidelines*.

### 6.1 Operating Environment

The reference thermal solution was designed assuming: under the high fan speed condition, a maximum local-ambient temperature of 53°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 3 m/S; under the acoustic fan speed condition, a maximum local-ambient temperature of 57°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 1.5 m/S.

The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35°C external-ambient temperature at 1500 m altitude. (External-ambient refers to the environment external to the system.)

### 6.2 Heatsink Performance

Figure 6-1 depicts the *simulated* thermal performance of the reference thermal solution versus approach air velocity. Since this data was modeled at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

The following equation can be used to correct any altitude:

$$\theta_{ca} = \alpha + \beta \times Q_{alt}^{-\gamma} \left( \frac{\rho_{alt}}{\rho_0} \right)^{-\gamma}$$

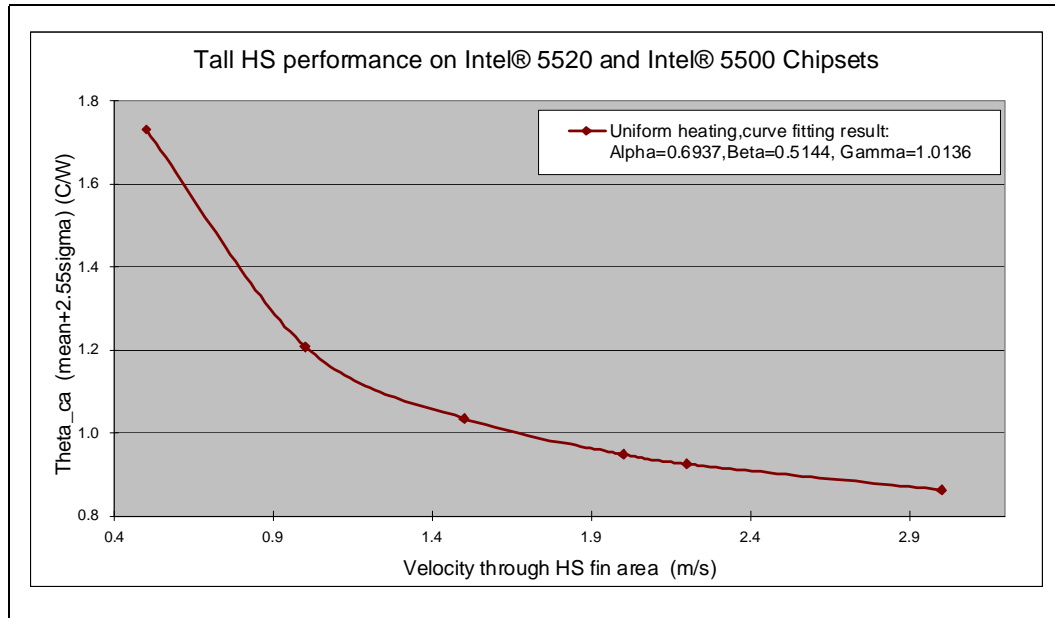
$\alpha$ ,  $\beta$  and  $\gamma$  can be obtained from Figure 6-1.

$Q$  - "velocity through heatsink fin area (m/s)". Velocity is the value on X axis of Figure 6-1.

$\rho_{alt}$  - Air density at given altitude.

$\rho_0$  - Air density at sea level.

Figure 6-1. Tall Torsional Clip Heatsink Measured Thermal Performance versus Approach Velocity



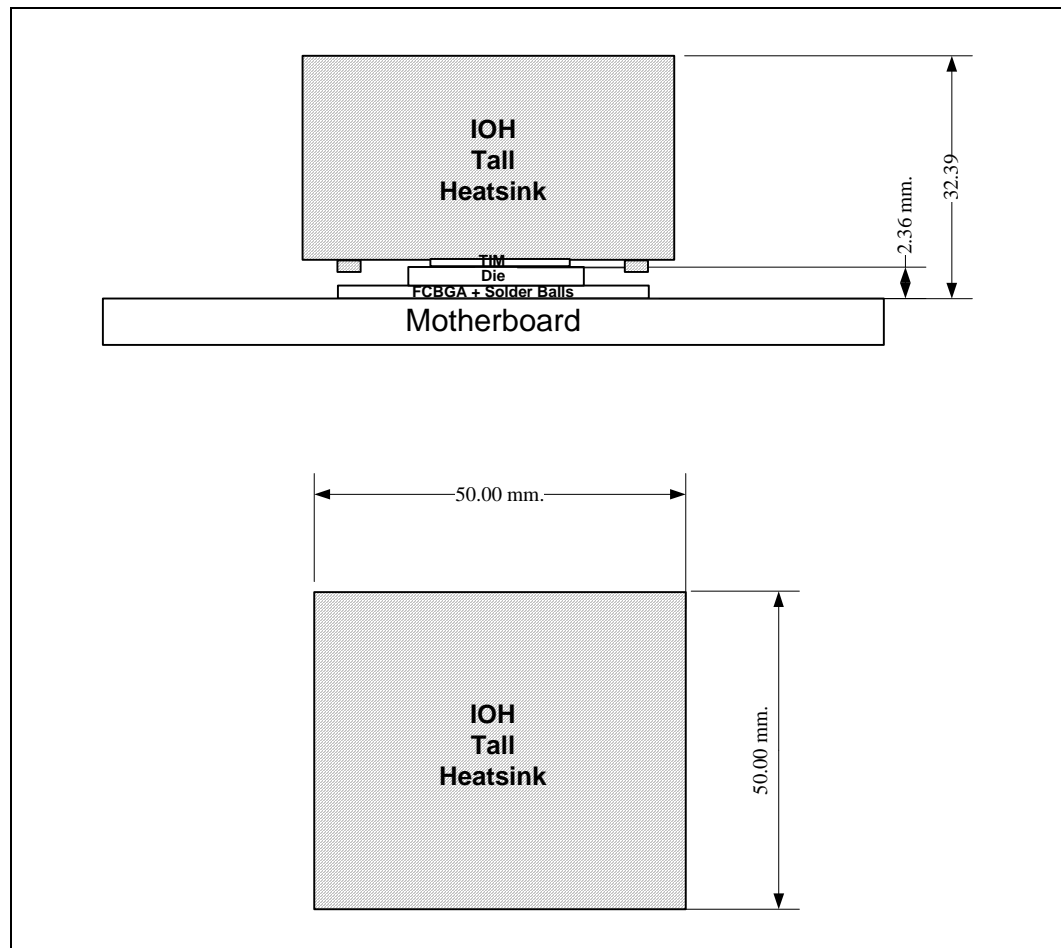
**Note:** 8.6% power through board at high fan speed and 10.5% power through board at acoustic fan speed are assumed.

### 6.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the Intel 5520 and Intel 5500 chipsets thermal solution are shown in [Figure 6-2](#).

When using heatsinks that extend beyond the IOH reference heatsink envelope shown in [Figure 6-2](#), any motherboard components placed between the heatsink and motherboard cannot exceed 1.60 mm (0.063 in.) in height.

**Figure 6-2. Tall Torsional Clip Heatsink Volumetric Envelope for the IOH**



## 6.4 Board-Level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in [Figure 6-3](#) and [Figure 6-4](#).

## 6.5 Tall Torsional Clip Heatsink Thermal Solution Assembly

The reference thermal solution for the IOH is a passive extruded heatsink with thermal interface. It is attached using a clip with each end hooked through an anchor soldered to the board. [Figure 6-6](#) shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in [Appendix B](#). [Appendix A](#) contains vendor information for each thermal solution component.

Figure 6-3. Tall Torsional Clip Heatsink Board Component Keepout

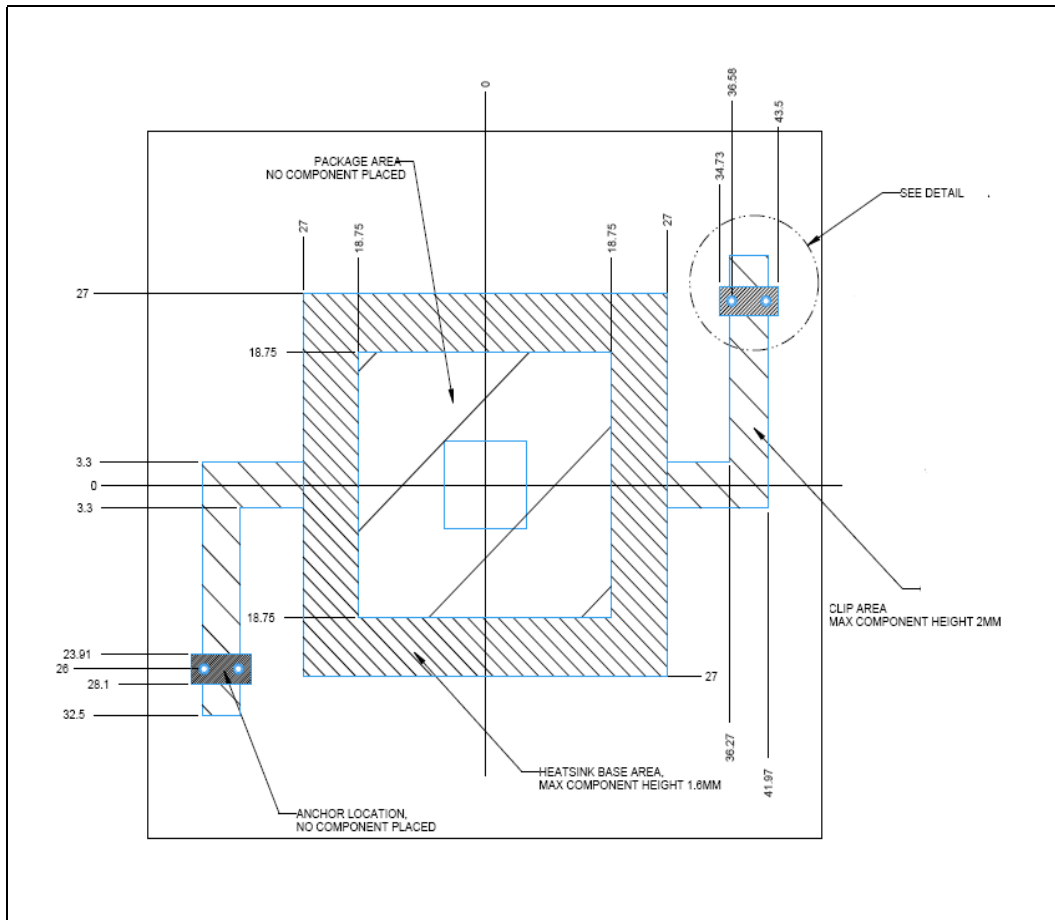


Figure 6-4. Retention Mechanism Component Keepout Zone

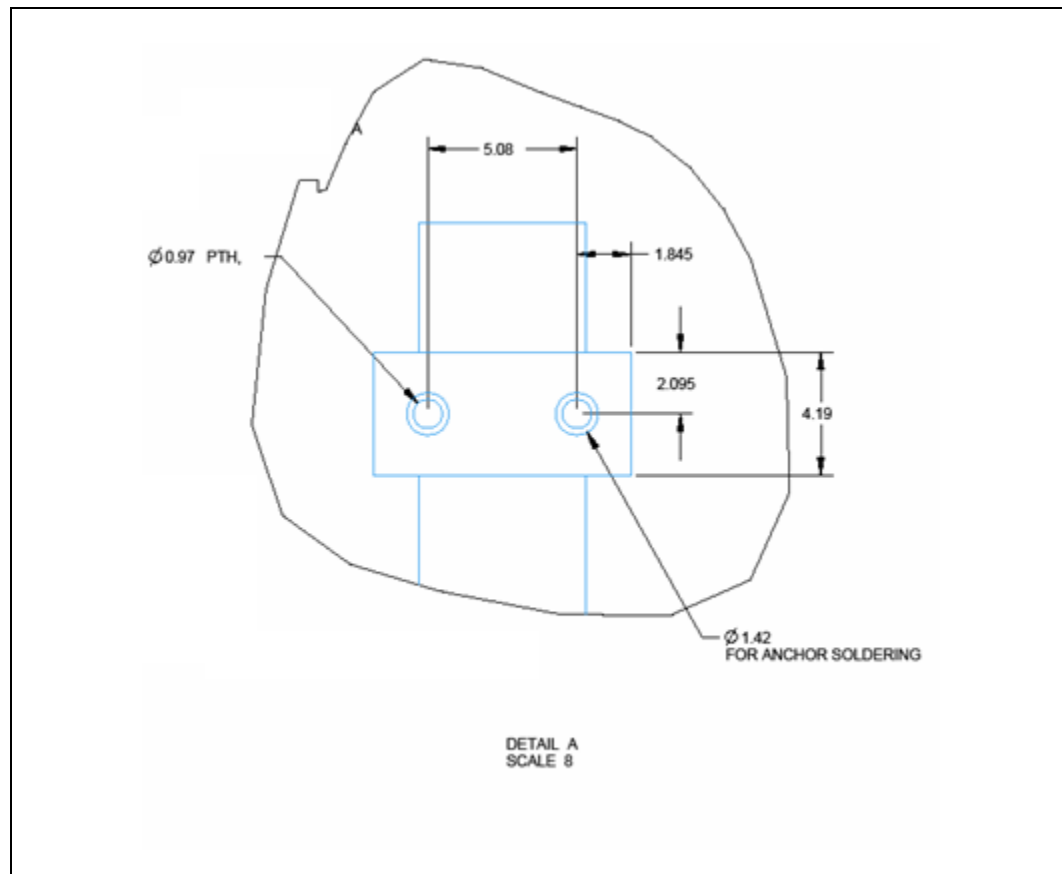
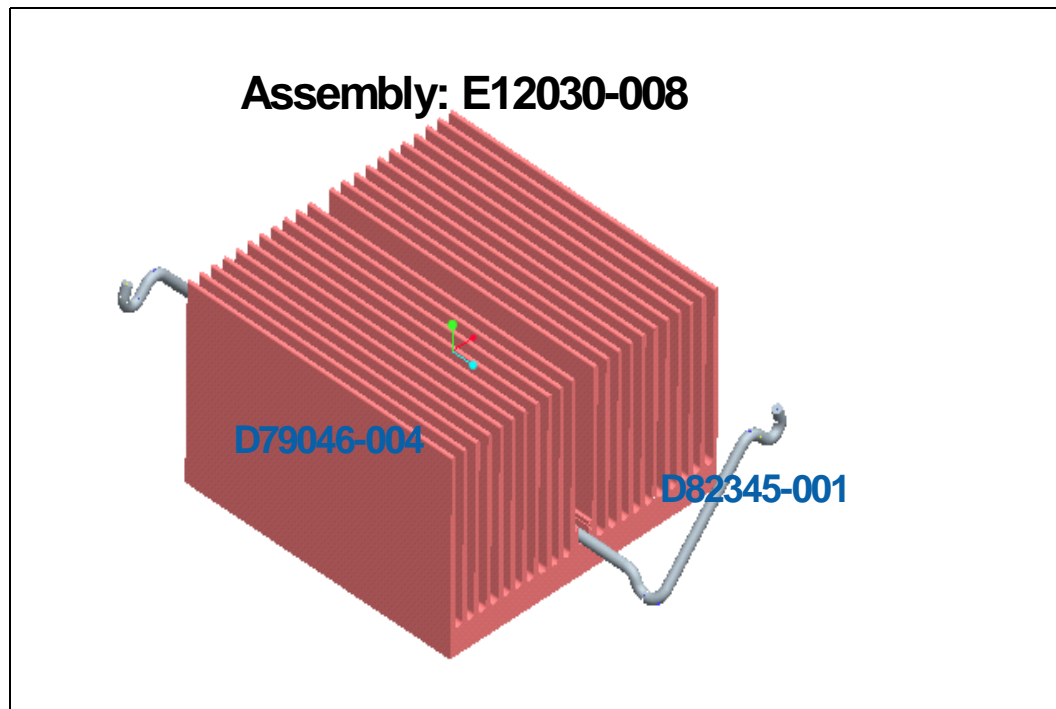


Figure 6-5. Tall Torsional Heatsink Assembly



### 6.5.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the heatsink fins.

### 6.5.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the IOH. [Figure 6-6](#) shows the heatsink profile. [Appendix A](#) lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawing of this heatsink is provided in [Appendix B](#).

### 6.5.3 Mechanical Interface Material

No mechanical interface material is associated with this reference solution.

### 6.5.4 Thermal Interface Material

A thermal interface material (TIM) provides improved conductivity between the IHS and heatsink. The reference thermal solution uses Honeywell PCM45 F\*, 0.25 mm (0.010 in.) thick, 20 mm x 20 mm (1.0 in. x 1.0 in.) square.

**Note:** Unflowed or “dry” Honeywell PCM45 F has a material thickness of 0.010 inch. The flowed or “wet” Honeywell PCM45F has a material thickness of ~0.003 inch after it reaches its phase change temperature.



### 6.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F TIM is shown in Table 6-1.

Intel provides both End of Line and End of Life TIM thermal resistance values of Honeywell PCM45F. End of Line and End of Life TIM thermal resistance values are obtained through measurement on a Test Vehicle similar to Intel 5520 and Intel 5500 chipsets' physical attributes using an extruded aluminum heatsink. The End of Line value represents the TIM performance post heatsink assembly while the End of Life value is the predicted TIM performance when the product and TIM reaches the end of its life. The heatsink clip provides enough pressure for the TIM to achieve End of Line thermal resistance of 0.19C x cm<sup>2</sup>/W and End of Life thermal resistance of 0.39C x cm<sup>2</sup>/W.

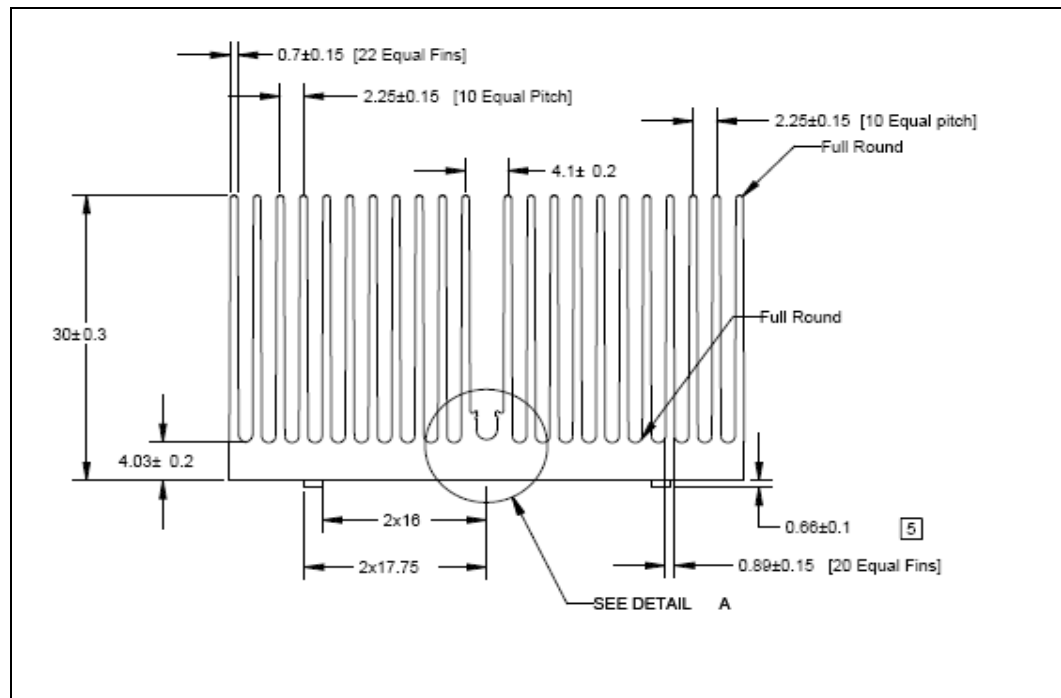
**Table 6-1. Honeywell PCM45 F\* TIM Performance as a Function of Attach Pressure**

Pressure on Thermal Solution and Package Interface (PSI)	Thermal Resistance (C* x cm <sup>2</sup> )/W	
	End of Line	End of Life
40	0.19	0.39

### 6.5.5 Heatsink Clip

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See Appendix B for a mechanical drawing of the clip.

**Figure 6-6. Tall Torsional Clip Heatsink Extrusion Profile**





### 6.5.6 Clip Retention Anchors

A clip retention anchor has been developed to minimize the impact of clip retention on the board for Intel 5520 and Intel 5500 chipset-based platforms that have limited board space. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See [Appendix A](#) for the part number and supplier information.

## 6.6 Alternative Tall Heatsink Clip

Intel has developed an alternative tall heatsink clip that will result in a smaller keep-out zone area. Both the thermal boundary condition requirements and mechanical boundary condition will not change with the use of this alternative tall heatsink clip. [Figure 6-7](#) and [Figure 6-8](#) shows the board level keep-zone requirement with alternative reference tall heatsink clip while [Figure 6-9](#) shows the tall heatsink and the alternative clip assembly. Full mechanical drawings of this alternative heatsink clip are provided in [Appendix B](#).



Figure 6-7. Tall Heatsink with Alternative Clip Board Component Keepout

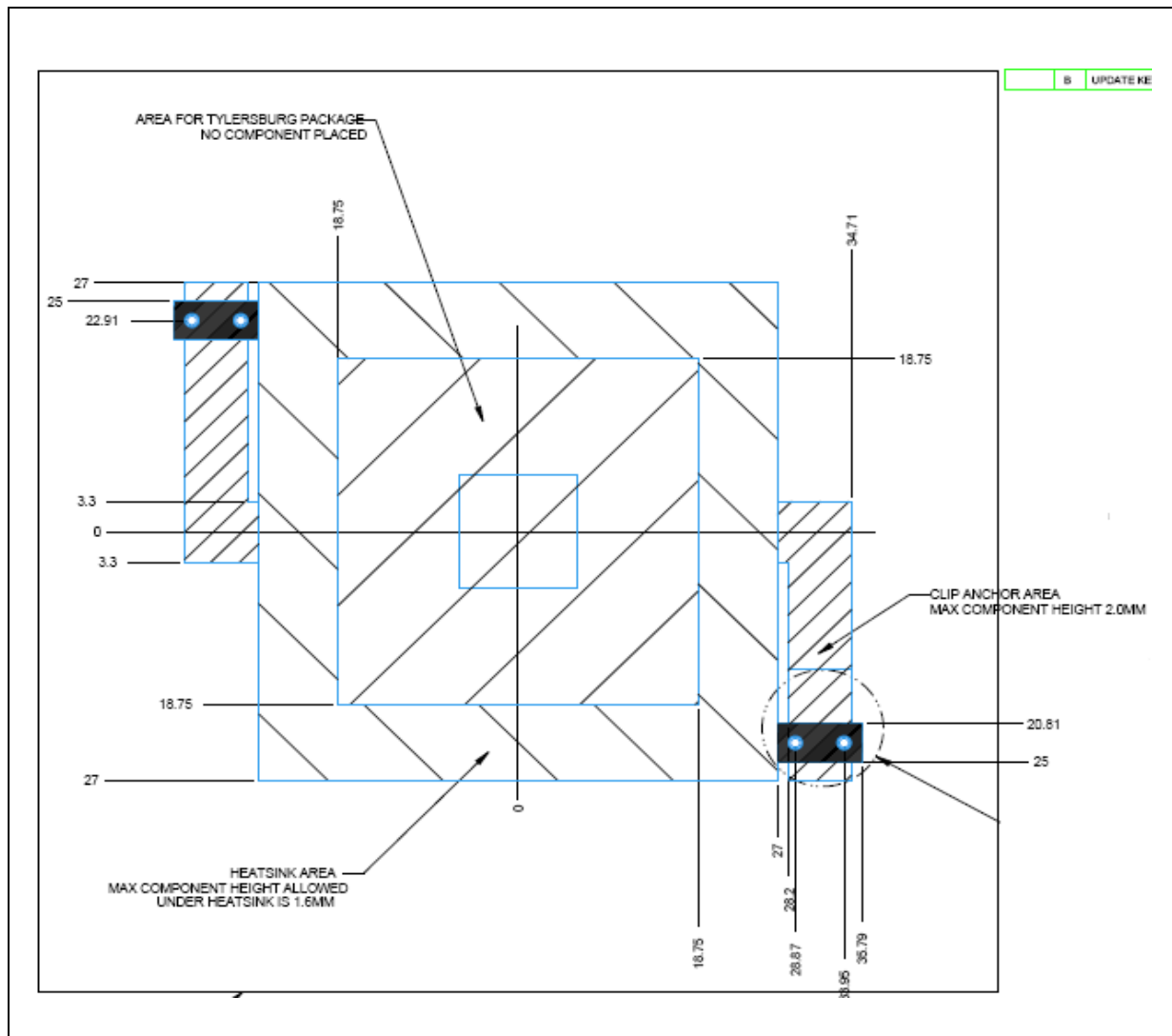


Figure 6-8. Retention Mechanism Component Keepout Zone for Alternative Clip

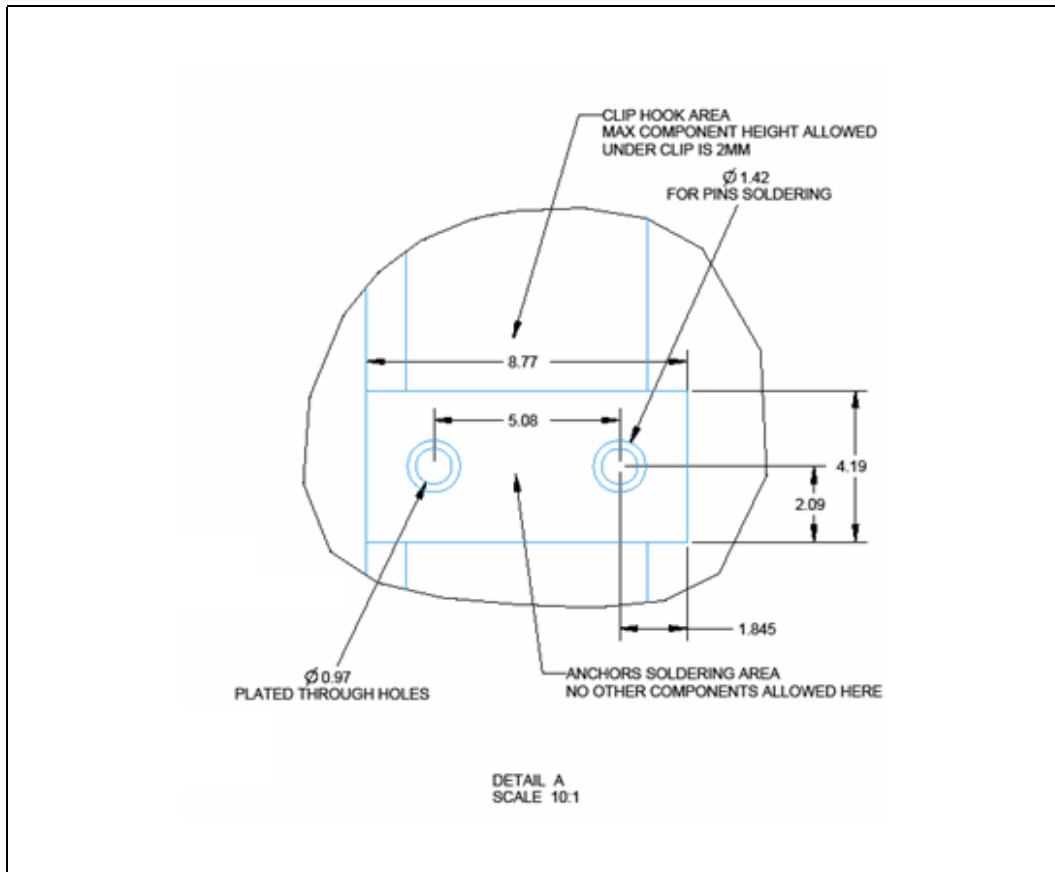
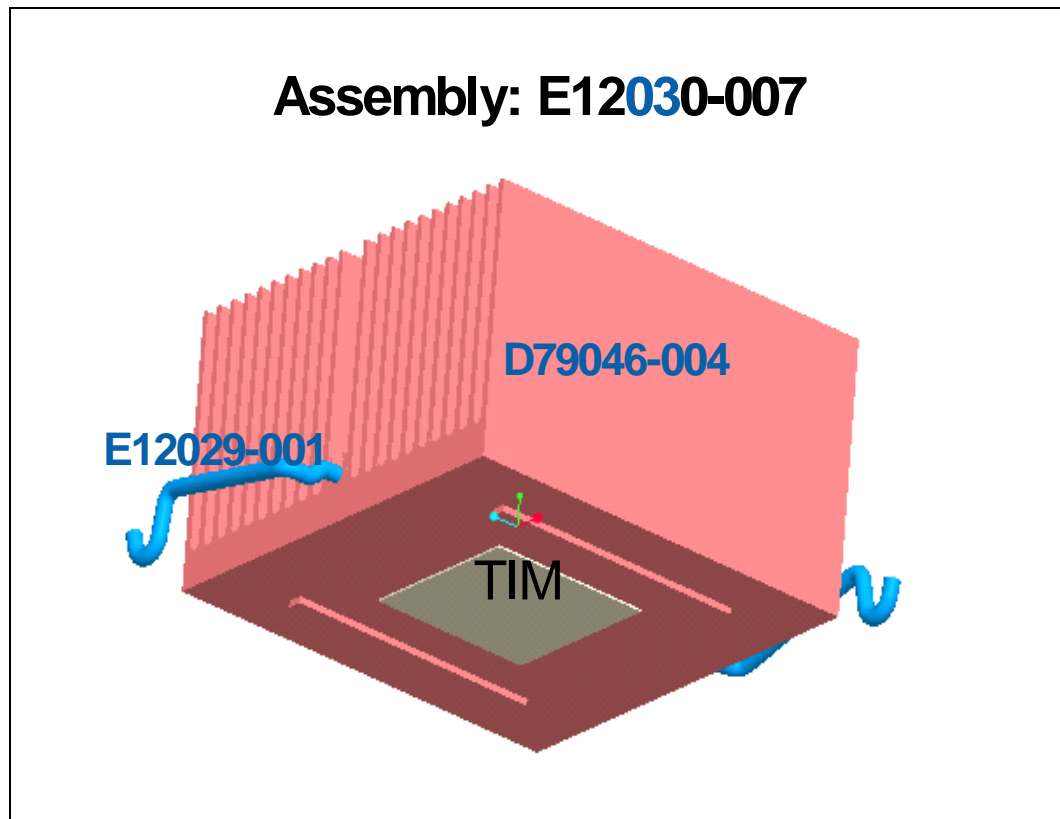


Figure 6-9. Tall Heatsink and Alternative Clip Assembly



## 6.7 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading to the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume.

The test profiles for the Intel 5520 and Intel 5500 chipsets reference solution are unpackaged system level limits. The reference solution is to be mounted to a fully configured system. The environmental reliability requirements for the reference thermal solution are shown in [Table 6-2](#). These could be considered as general guidelines.



**Table 6-2. Reliability Guidelines**

Test <sup>(1)</sup>	Requirement	Pass/Fail Criteria <sup>(2)</sup>
Mechanical Shock	System level unpackaged profile: 25G 2 drops in all 6 orientations	Visual Check and Electrical Functional Test
Random Vibration	System level unpackaged Duration: 10 min/axis, 3axes Power Spectral Density Profile: 2.20g RMS	Visual Check and Electrical Functional Test
Thermal Cycling	-40°C to +85°C, in conformance to JEDEC	Visual Check and Electrical Functional Test

**Notes:**

1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.

**§**



# 7 Reference Thermal Solution 2

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Intel has developed two different reference thermal solutions to meet the cooling needs of Intel 5520 and Intel 5500 chipsets under operating environments and specifications defined in this document. This section describes the overall requirements for the short torsional clip heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions depending on your specific system local-ambient operating conditions. For information on the ICH9, refer to thermal specification in the *Intel® I/O Controller Hub 9 (ICH9) Family Thermal and Mechanical Design Guidelines*.

## 7.1 Operating Environment

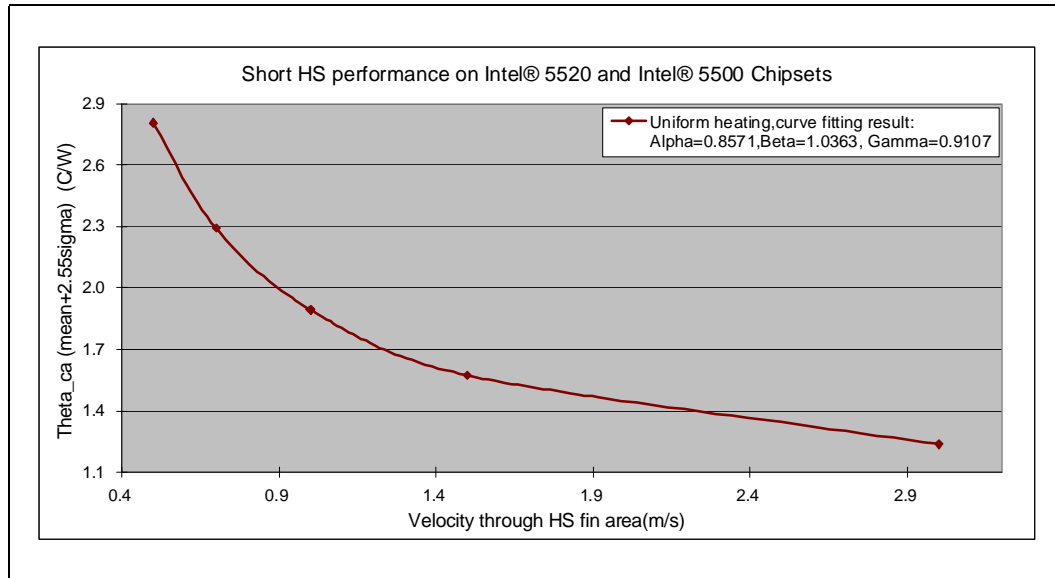
The reference thermal solution was designed assuming: under the high fan speed condition, a maximum local-ambient temperature of 43°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 0.8 m/s; under the acoustic fan speed condition, a maximum local-ambient temperature of 40°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 0.53 m/s.

The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35°C external-ambient temperature at 1500m altitude. (External-ambient refers to the environment external to the system.)

## 7.2 Heatsink Performance

Figure 7-1 depicts the *simulated* thermal performance of the reference thermal solution versus approach air velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

**Figure 7-1. Short Torsional Clip Heatsink Measured Thermal Performance versus Approach Velocity**



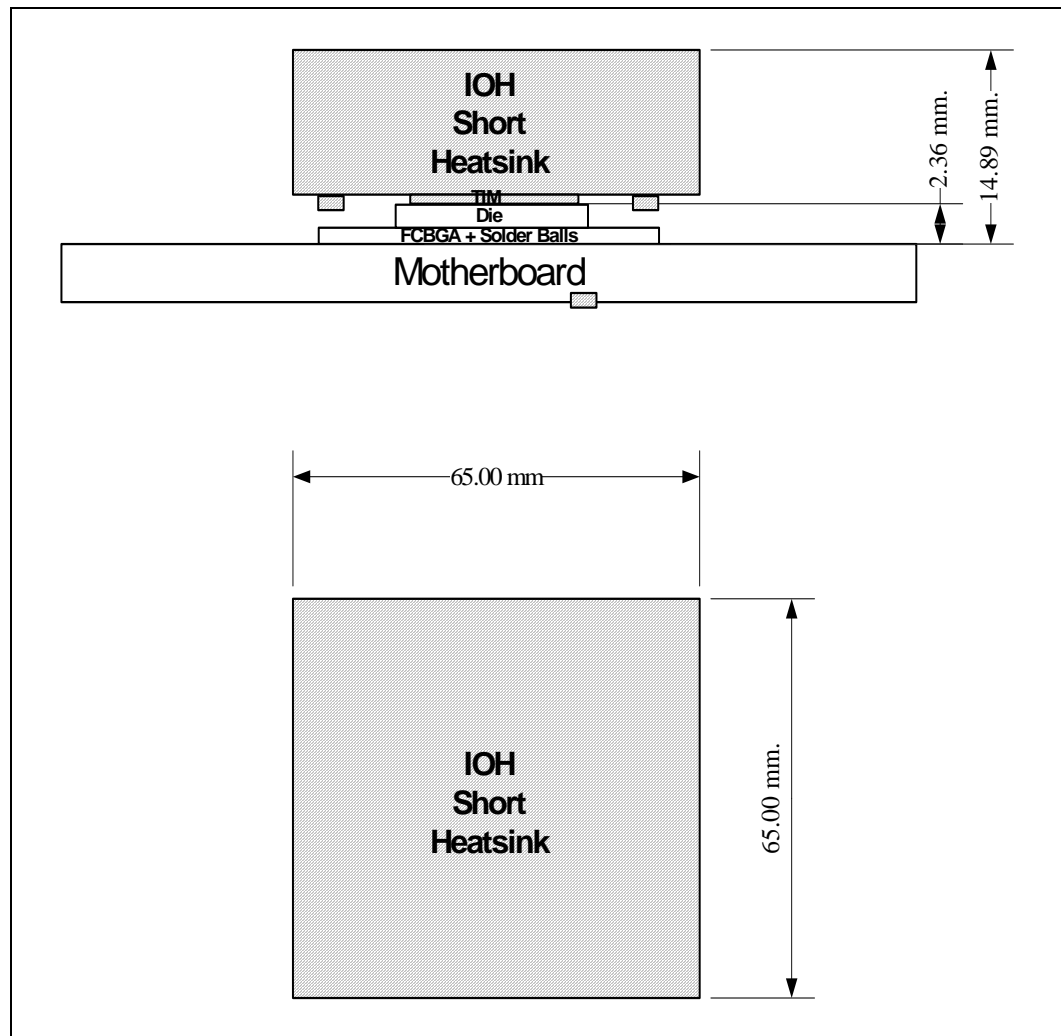
**Note:** 20.5% power through board at high fan speed and 25.7% power through board at acoustic fan speed are assumed.

### 7.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on Intel 5520 and Intel 5500 chipset thermal solutions are shown in [Figure 7-2](#).

When using heatsinks that extend beyond the IOH reference heatsink envelope shown in [Figure 7-2](#), any motherboard components placed between the heatsink and motherboard cannot exceed 1.60 mm (0.063 in.) in height.

**Figure 7-2. Short Torsional Clip Heatsink Volumetric Envelope for the IOH**



## 7.4 Board-Level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in [Figure 7-3](#) and [Figure 7-4](#).

## 7.5 Short Torsional Clip Heatsink Thermal Solution Assembly

The reference thermal solution for the IOH is a passive extruded heatsink with thermal interface. It is attached using a clip with each end hooked through an anchor soldered to the board. [Figure 7-5](#) shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in [Appendix B](#). [Appendix A](#) contains vendor information for each thermal solution component.

Figure 7-3. Short Torsional Clip Heatsink Board Component Keepout

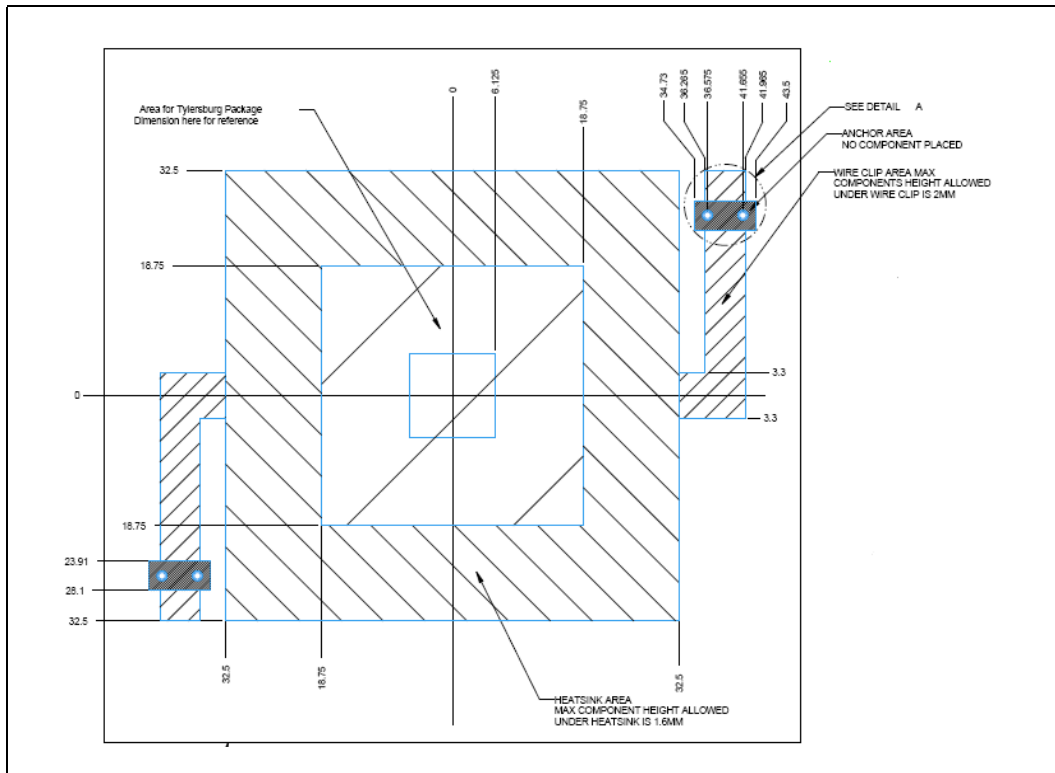
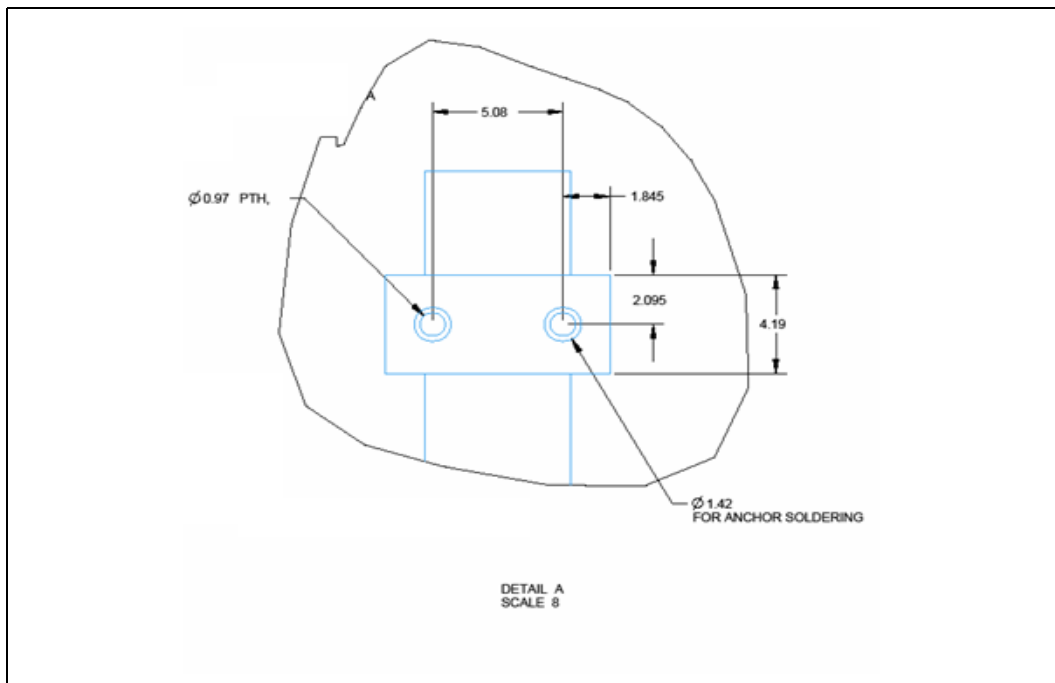


Figure 7-4. Retention Mechanism Component Keepout Zones

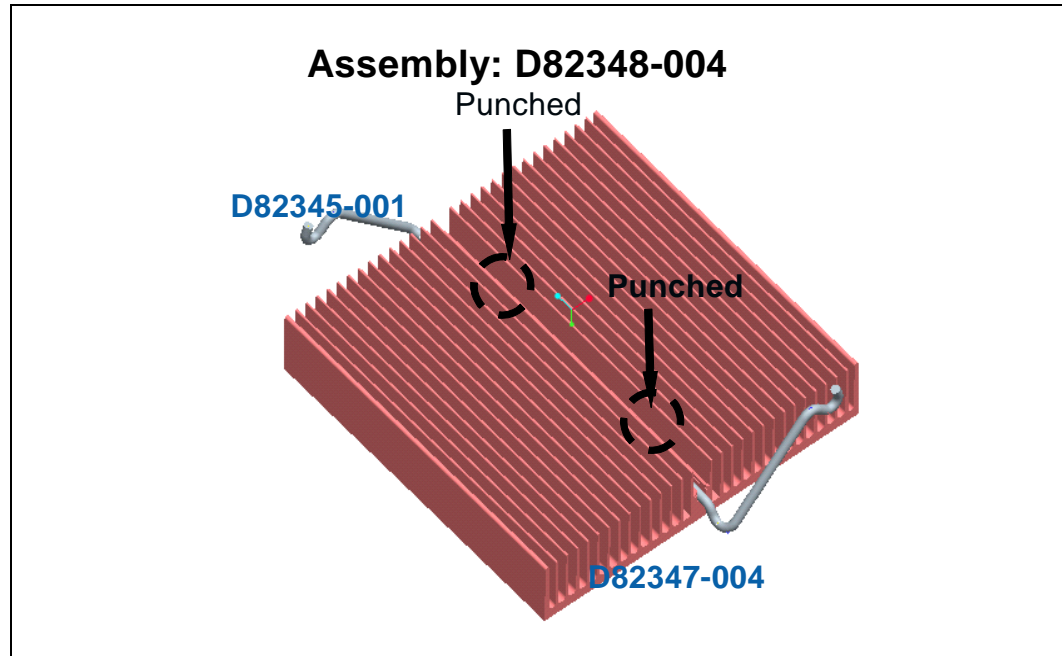




### 7.5.1 Heatsink Orientation

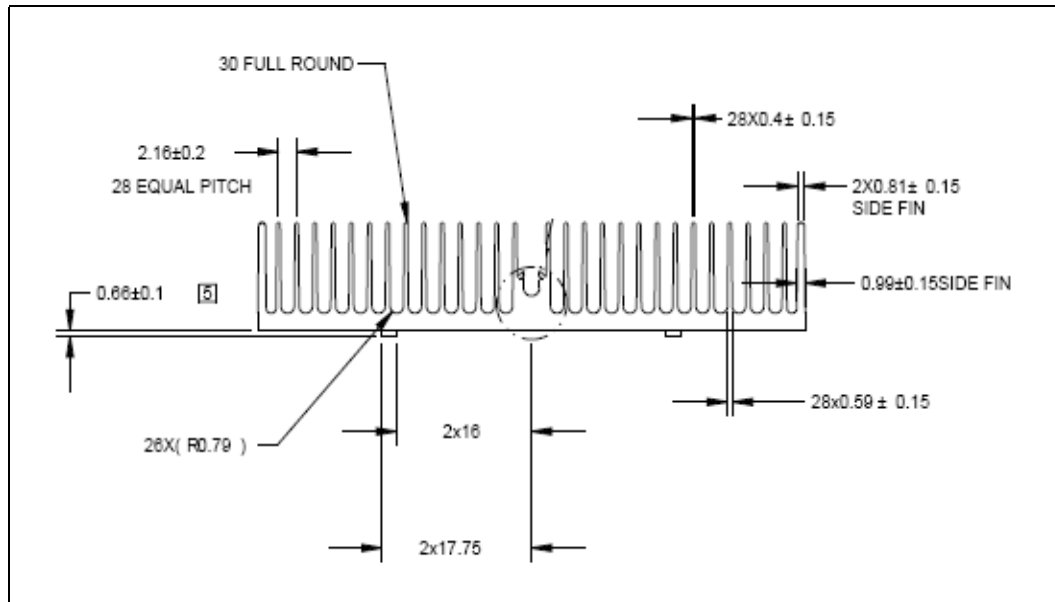
Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the heatsink fins.

**Figure 7-5. Short Torsional Clip Heatsink Assembly**



### 7.5.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the IOH. [Figure 7-6](#) shows the heatsink profile. [Appendix A](#) lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawings of this heatsink are provided in [Appendix B](#).

**Figure 7-6. Short Torsional Clip Heatsink Extrusion Profile**


### 7.5.3 Heatsink Surface Treatment

The short torsional heatsink is adopted due to volumetrical constraint. In addition, the heatsink is anodized for electrical insulation considerations in case there is any accidental contact with other components nearby.

### 7.5.4 Thermal Interface Material

A thermal interface material (TIM) provides improved conductivity between the IHS and heat sink. The reference thermal solution uses Honeywell PCM45 F\*, 0.25 mm (0.010 in.) thick, 20 mm x 20 mm (0.79 in. x 0.79 in.) square.

**Note:** Unflowed or “dry” Honeywell PCM45 F has a material thickness of 0.010 inch. The flowed or “wet” Honeywell PCM45F has a material thickness of ~0.003 inch after it reaches its phase change temperature.

#### 7.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F TIM is shown in [Table 7-1](#).

Intel provides both End of Line and End of Life TIM thermal resistance values of Honeywell PCM45F. End of Line and End of Life TIM thermal resistance values are obtained through measurement on a Test Vehicle similar to Intel 5520 and Intel 5500 chipsets’ physical attributes using an extruded aluminum heatsink. The End of Line value represents the TIM performance post heatsink assembly while the End of Life value is the predicted TIM performance when the product and TIM reaches the end of its life. The heatsink clip provides enough pressure for the TIM to achieve End of Line thermal resistance of  $0.19 \text{ x cm}^2/\text{W}$  and End of Life thermal resistance of  $0.39 \text{ x cm}^2/\text{W}$ .



**Table 7-1. Honeywell PCM45 F\* TIM Performance as a Function of Attach Pressure**

Pressure on Thermal Solution and Package Interface (PSI)	Thermal Resistance ( $^{\circ}\text{C} \times \text{in}^2$ )/W	
	End of Line	End of Life
40	0.19	0.39

### 7.5.5 Heatsink Clip

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See [Appendix B](#) for a mechanical drawing of the clip.

### 7.5.6 Clip Retention Anchors

A clip retention anchor has been developed to minimize the impact of clip retention on the board for Intel 5520 and Intel 5500 chipset-based platforms that have limited board space. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See [Appendix A](#) for the part number and supplier information.

## 7.6 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume.

The test profiles for Intel 5520 and Intel 5500 chipsets reference solutions are unpackaged system level limits. The reference solution is to be mounted to a fully configured system. The environmental reliability requirements for the reference thermal solution are shown in [Table 7-2](#). These could be considered as general guidelines.

**Table 7-2. Reliability Guidelines**

Test <sup>(1)</sup>	Requirement	Pass/Fail Criteria <sup>(2)</sup>
Mechanical Shock	System level unpackaged profile: 25G 2 drops in all 6 orientations	Visual Check and Electrical Functional Test
Random Vibration	System level unpackaged Duration: 10 min/axis, 3axes Power Spectral Density Profile: 2.20g RMS	Visual Check and Electrical Functional Test
Thermal Cycling	-40°C to +85°C, in conformance to JEDEC	Visual Check and Electrical Functional Test

**Notes:**

1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.







# 8 Design Recommendations for Solder Joint Reliability

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Solder Joint Reliability (SJR) remains a major topic of concern in designing systems especially for surface mounted components. Solder ball cracking and fracture is a failure mode associated with overstressing the surface mounted component on the motherboard. The over-stressing typically occurs when the motherboard is subjected to bending deflection. The deflection of the motherboard applies loads to these surface mounted components that attempt to peel the component from the board. These loads stress the solder balls of the component and either initiate cracks, which grow through the solder during thermal and power cycling, or cause fracture, which results in an electrical open.

Loading conditions such as shock typically stress the motherboard and generate stresses at the solder joints that leads to either crack initiation or complete fracture of the balls. This section will discuss guidance specific to the Intel 5520 and Intel 5500 chipsets. Please refer to the *System Mechanical Design Guidance for Dynamic Events - Application Notes / Briefs* for more information on system design guidance, and best practices.

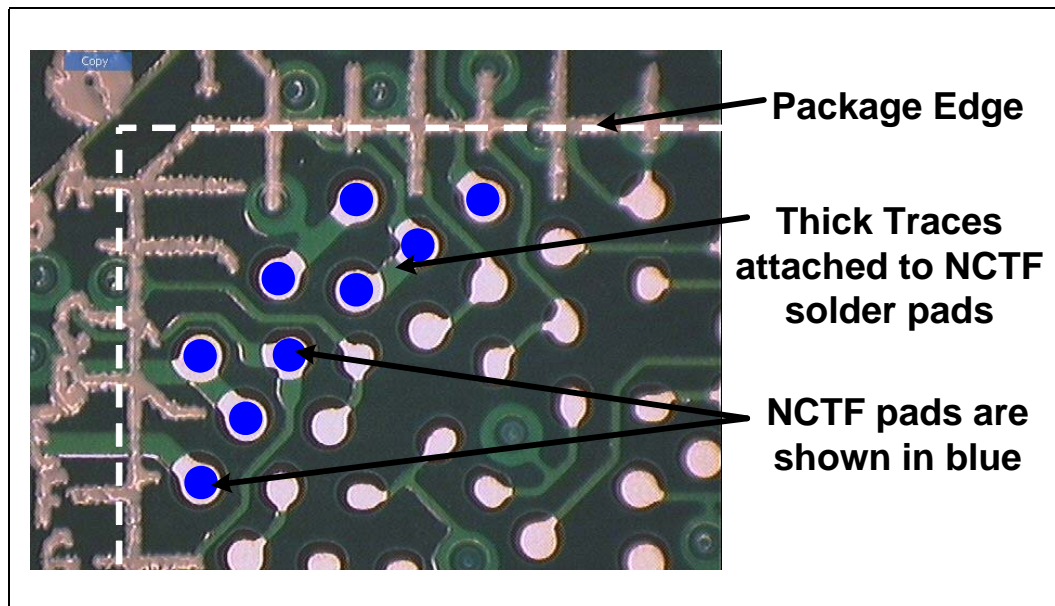
[Section 2.1](#) describes the function of the Non-Critical to Function (NCTF) Solder Balls. These balls are located in the corners of the ball grid array, where they are most susceptible to stressing from motherboard flexure, and under the die shadow. These NCTF balls mitigate degradation to component performance once damage has occurred at the solder balls. Monitoring of these NCTF balls during shock testing is described in the Platform Design Guide. General design guidance is available in the *System Mechanical Design Guidance for Dynamic Events - Application Notes / Briefs*. The NCTF solder balls provide for load shedding during solder ball loading events.

## 8.1 Solder Pad Recommendation

Additional protection from pad cratering on the motherboard has been demonstrated through the usage of thick traces at the corner NCTF ball locations. The NCTF trace thicknesses from 60-80% of the pad diameter were tested in board level shock tests with metal define pads and reduced the occurrence of pad cratering failures. Pad cratering is the failure mode in which solder pads in the motherboard separate from the PCB.

The thick traces shown in [Figure 8-1](#) are an example of how thick traces may be used at NCTF pads. Note the NCTF locations shown in [Figure 8-1](#) are not the NCTF locations of the name of product package and is shown to illustrate the application of thick traces. Designers are encouraged to use thick traces in designs where pad cratering has occurred along the corners of the package. The thick traces effectively increase the strength of the pad to motherboard interface and may cause a crack to initiate in a different failure mode in the NCTF solder ball while increasing the shock margin.

Figure 8-1. Example of Thick Traces used in a Desktop BGA



## 8.2 Shock Strain Guidance

A useful metric to compare the impact of design modifications to SJR and assess SJR risk during shock events is strain measurement. This strain measurement, also referred to as shock strain, utilizes strain gages to measure the surface strain of a motherboard. Please note that Intel also publishes strain guidance specifically for manufacturing. This manufacturing guidance is part of the Board Flexure Initiative (BFI) and those strain limits are commonly referred to as BFI strain. More information is available in the BFI Manufacturing Advantage Service (MAS). **DO NOT use BFI strain values for shock strain testing and DO NOT use shock strain guidance for BFI.** These two strain metrics are significantly different and are not interchangeable. Using the BFI strain values for a design metric will likely result in a poor system design.

Given parameters unique to the board of interest, such as board thickness, the board surface strain directly correlates to the amount of board curvature. The amount of motherboard curvature in the critical locations directly beneath the solder balls is indicative of the reliability of the component solder joints. This measurement is typically made at the corners of the BGA components. The shock strain results are sensitive to the application of the strain gages. Guidance for strain gage application is available in the Shock Strain Monitoring Customer Reference Document (CRD) and the local Intel Corporate Quality Engineer is also available for help with strain gage attach. This Shock Strain Monitoring CRD outlines the proper selection, application, and usage of the strain gages and strain instrumentation to attain repeatable and valid results. The Shock Strain Monitoring CRD also discusses proper reduction of the data in order to use the data to compare to the Intel strain guidance.

The strain guidelines will be developed from empirical testing under differing boundary conditions and published in a subsequent release of this document. Three strain ranges are determined to quantify associated SJR risk for the Critical to Function solder joints. The Non-Critical to Function solder balls may have some cracking and fractures when the strain measurements are within this guidance. [Table 8-1](#) lists the three ranges for the Intel 5520 and Intel 5500 chipsets.



Table 8-1. Shock Strain Guidance

Shock Strain (micro strain, $\mu\epsilon$ )	Associated Risk	Recommendation / Comments
$E_{min} < 2000$	Low	Solder joint failure is unlikely
$2000 < E_{min} < 2400$	Medium	Larger sample size and failure analysis is suggested for design validation
$2400 < E_{min}$	High	Solder joint failure is likely, consider design changes to improve reliability

**Notes:**

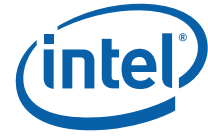
1.  $E_{min}$  is the minimum principal strain as defined in the Shock Strain Monitoring Customer Reference Document.
2. These values are for 0.062 inch nominal board thickness.
3. The strain value limits will be different for different board thicknesses. Please contact your Intel Field Sales representative if your design uses a different board thickness.

The associated risk levels correspond to the likelihood of solder joint failure. A Low level of risk is unlikely to result in critical to function solder joint failures. When strain measurements are made from a small sample of boards or systems and fall within the Medium risk range, there is insufficient information to assess the risk. It is suggested that additional systems or boards are tested and failure analysis, such as dye and peel, is conducted to assess the risk. A High risk is likely to result in a significant quantity of solder joint failures of critical solder balls. A change to the design is strongly recommended to reduce the bending of the motherboard under shock. Incorporating the Intel Reference Design Heatsink described in [Section 6](#) and [Section 7](#) into the design or adopting the design practices outlined in the *System Mechanical Design Guidance for Dynamic Events - Application Notes / Briefs* will improve the strain response and therefore reduce SJR risk.

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# A Thermal Solution Component Suppliers

## A.1 Tall Torsional Clip Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: <ul style="list-style-type: none"> <li>Unidirectional Fin Heatsink</li> <li>Thermal Interface Material</li> <li>Torsional Clip</li> </ul>	E12030-007 (with Alternative Clip) E12030-008	AVC P/N: S908B00001 (with Alternative Clip) P/N: S908B00002	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 00C95740103 (with Alternative Clip) P/N: 00C95740203	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Unidirectional Fin Heatsink	D79046-004	AVC P/N: M0908B0024	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 335C95740103	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Thermal Interface (PCM45F)	C65858-001	Honeywell PCM45 F*	Scott Miller 509-252-2206 <a href="mailto:scott.miller4@honeywell.com">scott.miller4@honeywell.com</a>
Heatsink Attach Clip	D82345-001	AVC P/N: A208000331	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 334C91590101	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>



Part	Intel Part Number	Supplier (Part Number)	Contact Information
Alternative Clip	E12029-001	AVC P/N: A208000345	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 334C95740102	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Solder-Down Anchor	A13494-007	Foxconn (HB96030-DW)*	Julia Jiang (USA) 408-919-6178 <a href="mailto:juliaj@foxconn.com">juliaj@foxconn.com</a>

**Notes:**

1. Contact the supplier directly to verify time of component availability.
2. Anchor is independent of heatsink assembly. Proper Anchor selection will protect the chipset heatsink from shock and vibration.

## A.2 Short Torsional Clip Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: <ul style="list-style-type: none"> <li>• Unidirectional Fin Heatsink</li> <li>• Thermal Interface Material</li> <li>• Torsional Clip</li> </ul>	D82348-004	AVC P/N: SL06400001	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 00C91590104	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Unidirectional Fin Heatsink	D82347-004	AVC P/N: M0L0640000	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 335C91590104	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Thermal Interface (PCM45F)	C65858-001	Honeywell PCM45 F*	Scott Miller 509-252-2206 <a href="mailto:scott.miller4@honeywell.com">scott.miller4@honeywell.com</a>



Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Attach Clip	D82345-001	AVC P/N: A208000331	Rachel Hsu (Taiwan) 886-2-2299-6930 x 7630 <a href="mailto:raichel_hsi@avc.com.tw">raichel_hsi@avc.com.tw</a> David Chao (Taiwan) 886-2-2299-6930 x 7619 <a href="mailto:david_chao@avc.com.tw">david_chao@avc.com.tw</a>
		CCI P/N: 334C91590101	Monica Chih (Taiwan) 866-2-29952666, x1131 <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> Harry Lin (U.S.A) 714-739-5797 <a href="mailto:Ackinc@aol.com">Ackinc@aol.com</a>
Solder-Down Anchor	A13494-007	Foxconn (HB96030-DW)*	Julia Jiang (USA) 408-919-6178 <a href="mailto:julij@foxconn.com">julij@foxconn.com</a>

**Notes:**

1. Contact the supplier directly to verify the component availability.
2. Anchor is independent of heatsink assembly. Proper Anchor selection will protect the chipset heatsink from shock and vibration.
3. CCI doesn't have P/N for thermal solution components' piece parts, please check with CCI on the thermal solution assembly P/N for further information.







# B Mechanical Drawings

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Table B-1 lists the mechanical drawings included in this appendix.

**Table B-1. Mechanical Drawing List**

Drawing Description	Figure Number
Tall Torsional Clip Heatsink Assembly Drawing	Figure B-1
Tall Torsional Heatsink Drawing 1 (1 of 2)	Figure B-2
Tall Torsional Heatsink Drawing 2 (2 of 2)	Figure B-3
Tall/Short Torsional Clip Heatsink Clip Drawing	Figure B-4
Short Torsional Clip Heatsink Assembly Drawing	Figure B-5
Short Torsional Heatsink Drawing	Figure B-6
Alternative Clip for Tall Torsional Heatsink	Figure B-7

Figure B-1. Tall Torsional Clip Heatsink Assembly Drawing

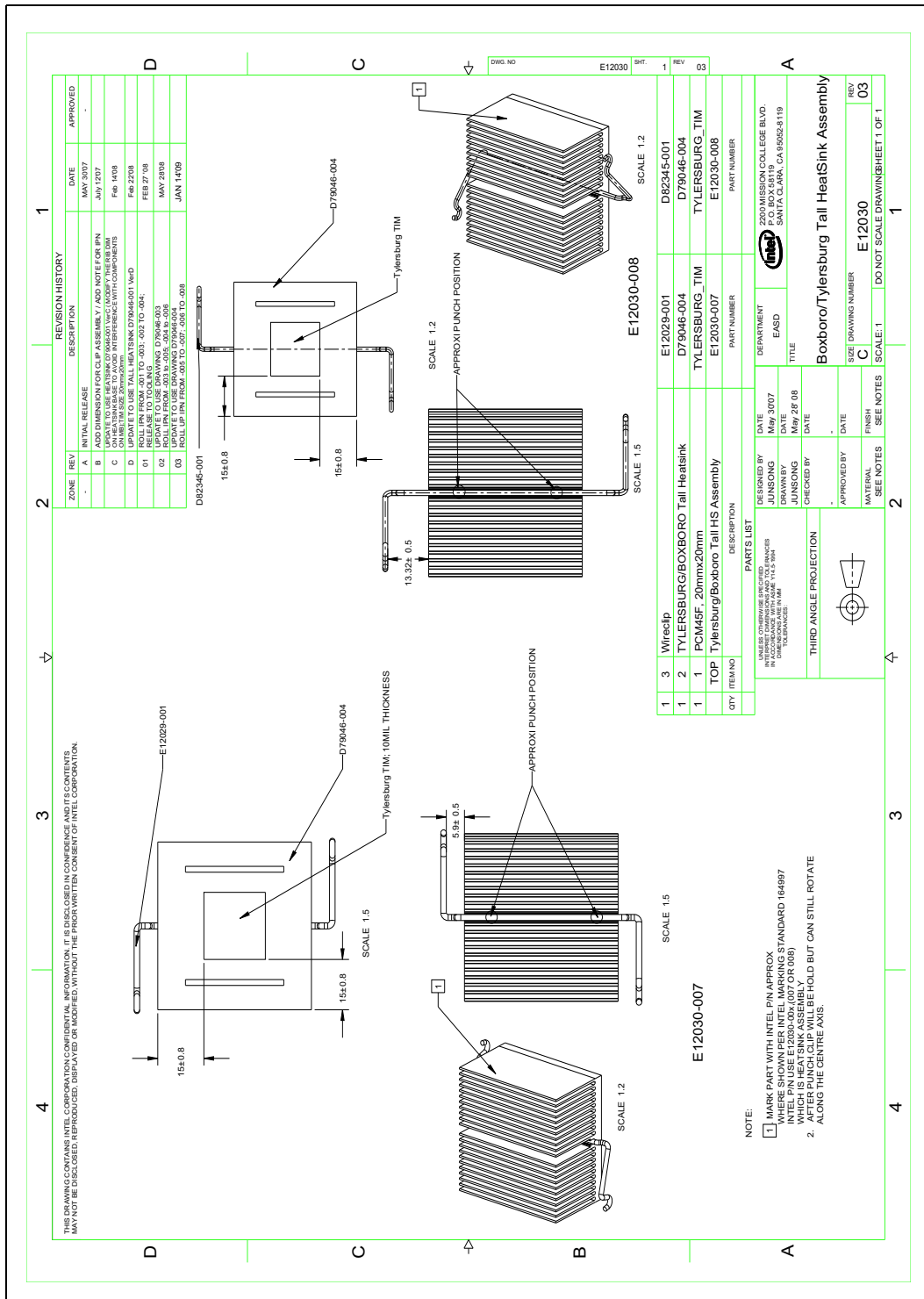




Figure B-3. Tall Torsional Heatsink Drawing 2 (2 of 2)

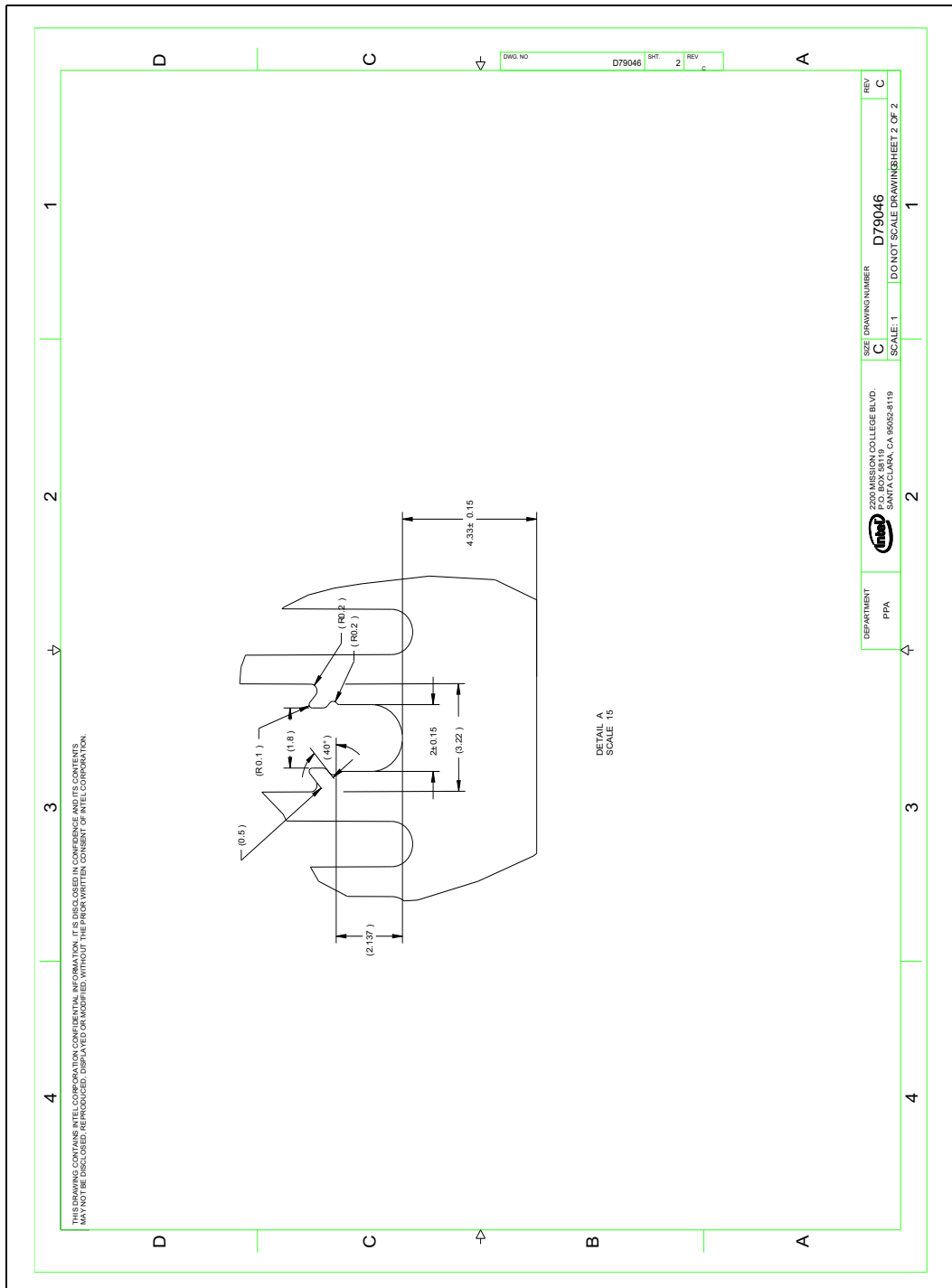






Figure B-5. Short Torsional Clip Heatsink Assembly Drawing

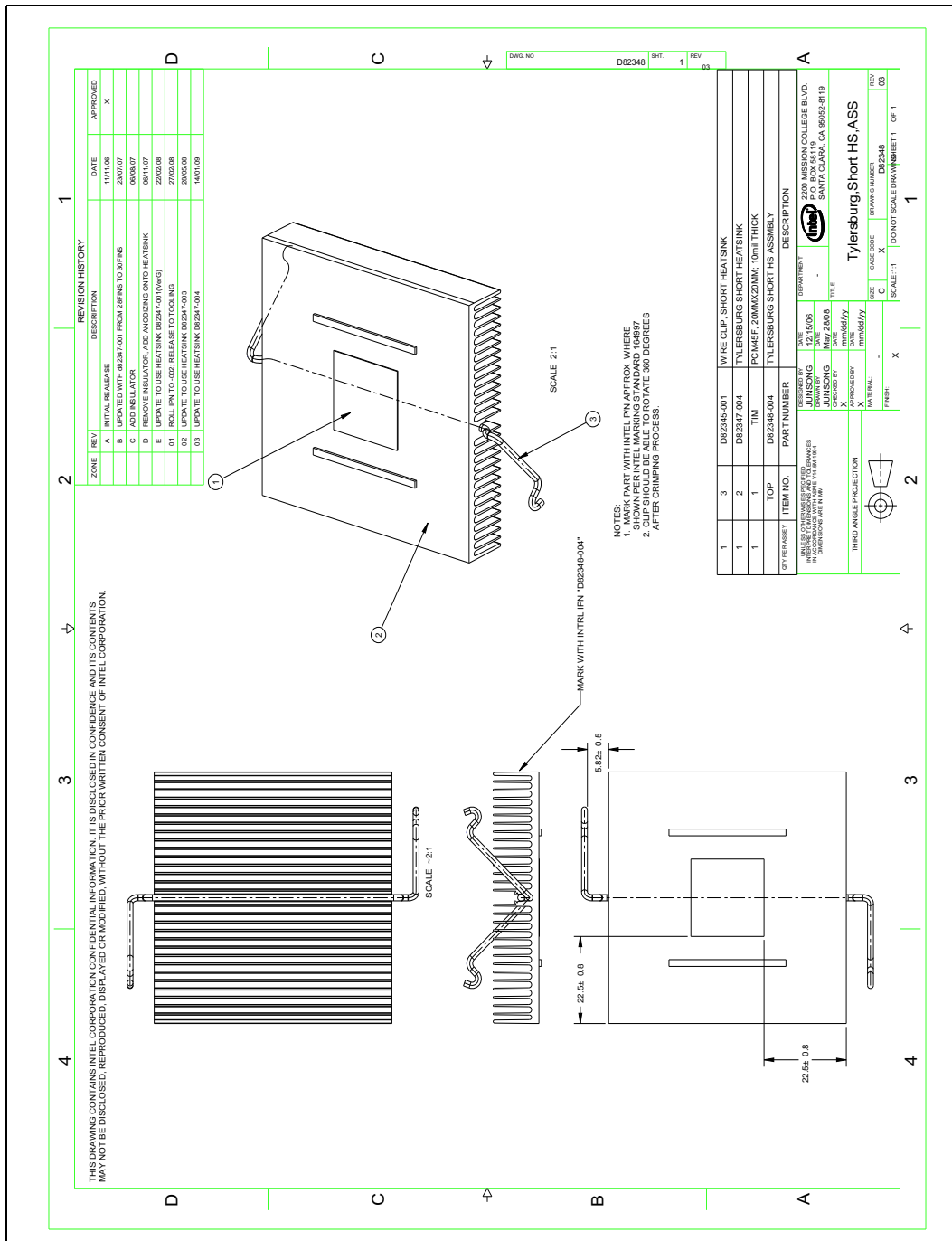




Figure B-6. Short Torsional Heatsink Drawing

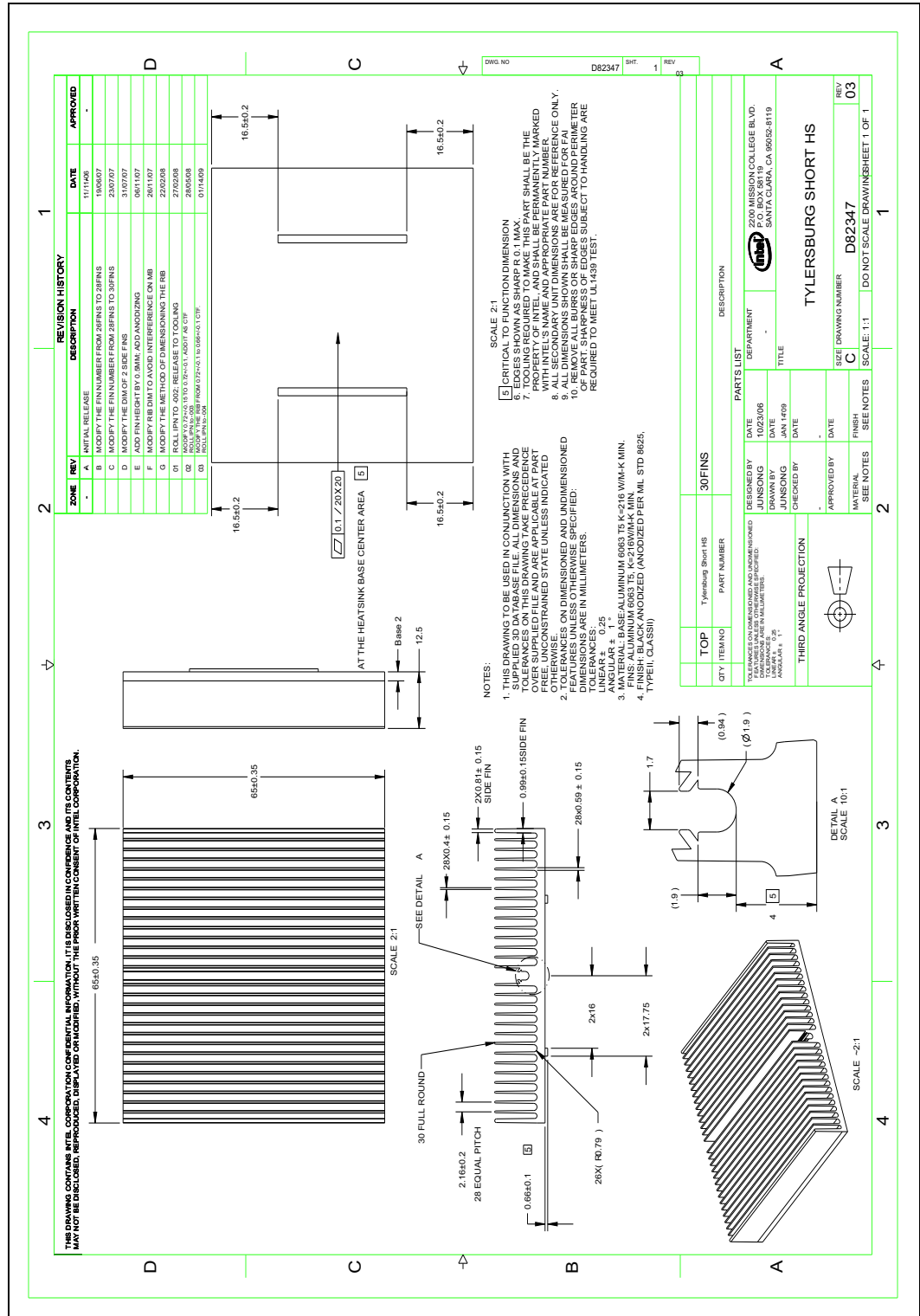
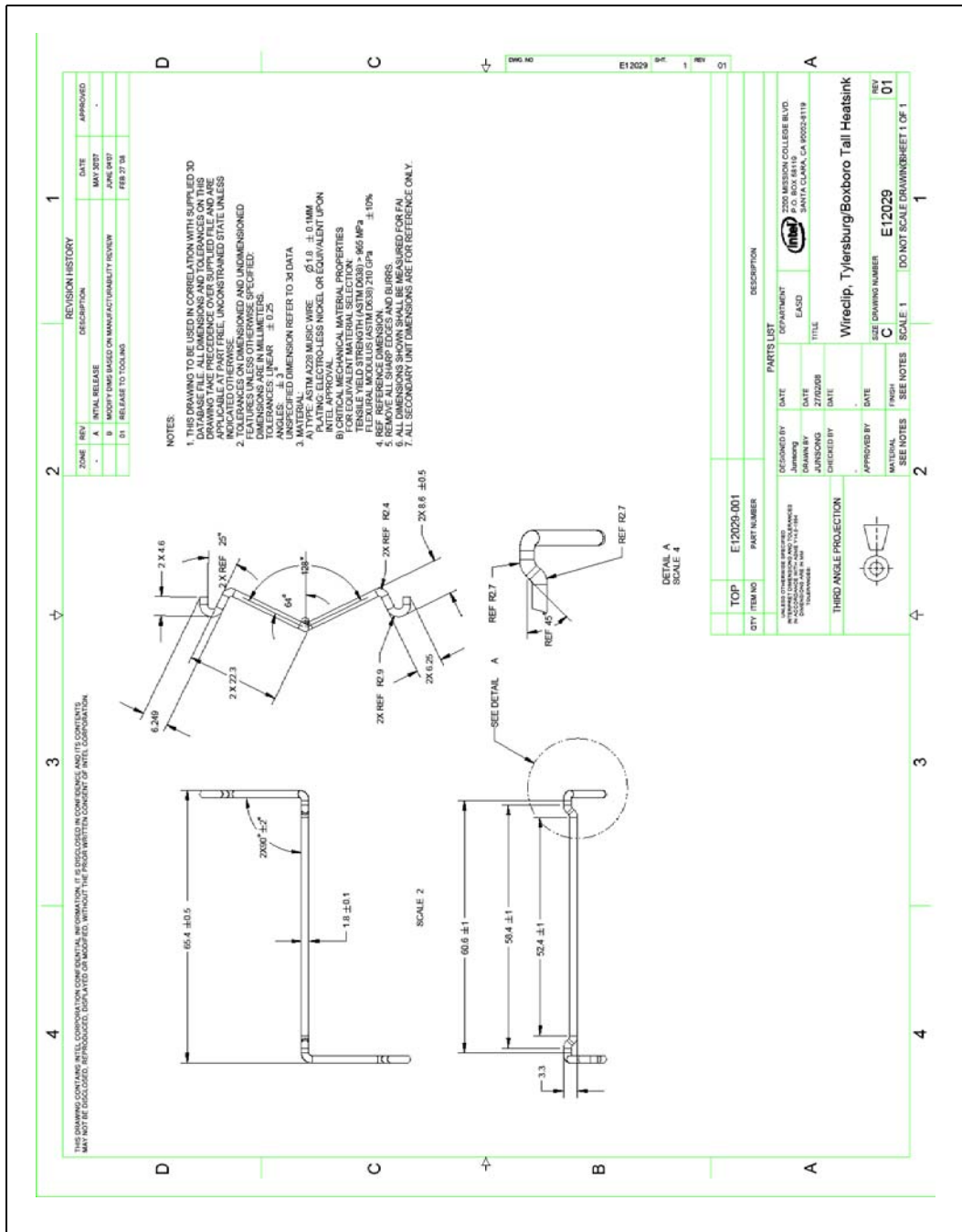


Figure B-7. Alternative Clip for Tall Torsional Heatsink



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