

DDR3 SDRAM Mini-RDIMM

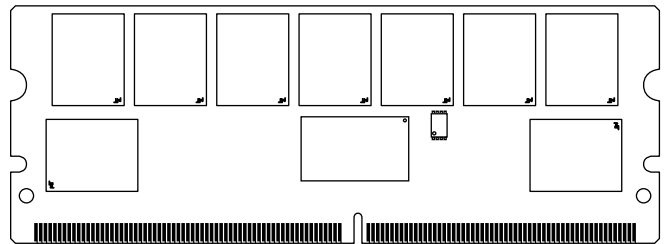
MT18JSF51272PKZ – 4GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 244-pin, registered dual in-line, 82mm, memory module (Mini-RDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 4GB (512 Meg x 72)
- $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- dual rank
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 244-Pin Mini-RDIMM (MO-244 R/C C)

Module height: 30mm (1.181in)



Options

- Operating temperature
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)¹
- Package
 - 244-pin halogen-free Mini-RDIMM
- Frequency/CAS latency
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.87ns @ CL = 7 (DDR3-1066)

Marking

None
I
Z
-1G6
-1G4
-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							t _{RCD} (ns)	t _{RP} (ns)	t _{RC} (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	4GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (256 Meg x 8)
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J256M8,¹ 2Gb DDR3 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT18JSF51272PK(I)Z-1G6__	4GB	512 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18JSF51272PK(I)Z-1G4__	4GB	512 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18JSF51272PK(I)Z-1G1__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

- Notes:
1. The data sheet for the base device can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18JSF51272PKZ-1G4D1.



Pin Assignments

Table 4: Pin Assignments

244-Pin DDR3 Mini-RDIMM Front								244-Pin DDR3 Mini-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{TT}	31	DQ24	61	V _{DD}	92	DQ40	123	V _{TT}	153	DQ29	183	A3	214	DQ45
2	V _{REFDQ}	32	DQ25	62	A2	93	DQ41	124	V _{SS}	154	V _{SS}	184	A1	215	V _{SS}
3	V _{SS}	33	V _{SS}	63	V _{DD}	94	V _{SS}	125	DQ4	155	DM3/ TDQS12	185	V _{DD}	216	DM5/ TDQS14
4	DQ0	34	DQS3#	64	NC	95	DQS5#	126	DQ5	156	NF/ TDQS12#	186	CK0	217	NF/ TDQS14#
5	DQ1	35	DQS3	65	NC	96	DQS5	127	V _{SS}	157	V _{SS}	187	CK0#	218	V _{SS}
6	V _{SS}	36	V _{SS}	66	V _{DD}	97	V _{SS}	128	DM0/ TDQS9	158	DQ30	188	V _{DD}	219	DQ46
7	DQS0#	37	DQ26	67	V _{REFCA}	98	DQ42	129	NF/ TDQS9#	159	DQ31	189	V _{DD}	220	DQ47
8	DQS0	38	DQ27	68	V _{DD}	99	DQ43	130	V _{SS}	160	V _{SS}	190	EVENT#	221	V _{SS}
9	V _{SS}	39	V _{SS}	69	Par_In	100	V _{SS}	131	DQ6	161	CB4	191	A0	222	DQ52
10	DQ2	40	CB0	70	V _{DD}	101	DQ48	132	DQ7	162	CB5	192	V _{DD}	223	DQ53
11	DQ3	41	CB1	71	A10	102	DQ49	133	V _{SS}	163	V _{SS}	193	BA1	224	V _{SS}
12	V _{SS}	42	V _{SS}	72	BA0	103	V _{SS}	134	DQ12	164	DM8/ TDQS17	194	V _{DD}	225	DM6/ TDQS15
13	DQ8	43	DQS8#	73	V _{DD}	104	DQS6#	135	DQ13	165	NF/ TDQS17#	195	RAS#	226	NF/ TDQS15#
14	DQ9	44	DQS8	74	WE#	105	DQS6	136	V _{SS}	166	V _{SS}	196	CS0#	227	V _{SS}
15	V _{SS}	45	V _{SS}	75	CAS#	106	V _{SS}	137	DM1/ TDQS10	167	CB6	197	V _{DD}	228	DQ54
16	DQS1#	46	CB2	76	V _{DD}	107	DQ50	138	NF/ TDQS10#	168	CB7	198	ODT0	229	DQ55
17	DQS1	47	CB3	77	CS1#	108	DQ51	139	V _{SS}	169	V _{SS}	199	A13	230	V _{SS}
18	V _{SS}	48	V _{SS}	78	ODT1	109	V _{SS}	140	DQ14	170	NC	200	V _{DD}	231	DQ60
19	DQ10	49	NC	79	V _{DD}	110	DQ56	141	DQ15	171	NC	201	NC	232	DQ61
20	DQ11	50	RESET#	80	NC	111	DQ57	142	V _{SS}	172	CKE1	202	NC	233	V _{SS}
21	V _{SS}	51	CKE0	81	NC	112	V _{SS}	143	DQ20	173	V _{DD}	203	V _{SS}	234	DM7/ TDQS16
22	DQ16	52	V _{DD}	82	V _{SS}	113	DQS7#	144	DQ21	174	A15	204	DQ36	235	NF/ TDQS16#
23	DQ17	53	BA2	83	DQ32	114	DQS7	145	V _{SS}	175	A14	205	DQ37	236	V _{SS}
24	V _{SS}	54	Err_Out#	84	DQ33	115	V _{SS}	146	DM2/ TDQS11	176	V _{DD}	206	V _{SS}	237	DQ62
25	DQS2#	55	V _{DD}	85	V _{SS}	116	DQ58	147	NF/ TDQS11#	177	A12	207	DM4/ TDQS13	238	DQ63
26	DQS2	56	A11	86	DQS4#	117	DQ59	148	V _{SS}	178	A9	208	NF/ TDQS13#	239	V _{SS}
27	V _{SS}	57	A7	87	DQS4	118	V _{SS}	149	DQ22	179	V _{DD}	209	V _{SS}	240	V _{DDSPD}
28	DQ18	58	V _{DD}	88	V _{SS}	119	SA0	150	DQ23	180	A8	210	DQ38	241	SA1
29	DQ19	59	A5	89	DQ34	120	SCL	151	V _{SS}	181	A6	211	DQ39	242	SDA
30	V _{SS}	60	A4	90	DQ35	121	SA2	152	DQ28	182	V _{DD}	212	V _{SS}	243	V _{SS}
				91	V _{SS}	122	V _{TT}					213	DQ44	244	V _{TT}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	Parity input: Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Reset: RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus.
CBx	I/O	Check bits: Used for system error detection and correction.
DQx	I/O	Data input/output: Bidirectional data bus.
DQSx, DQSx#	I/O	Data strobe: Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	Serial data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I ² C bus.
TDQSx, TDQSx#	Output	Redundant data strobe (x8 devices only): TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	Parity error output: Parity error found on the command and address bus.
EVENT#	Output (open drain)	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V _{DD}	Supply	Power supply: 1.5V ±0.075V. The component V _{DD} and V _{DDQ} are connected to the module V _{DD} .
V _{DDSPD}	Supply	Temperature sensor/SPD EEPROM power supply: 3.0–3.6V.
V _{REFCA}	Supply	Reference voltage: Control, command, and address V _{DD} /2.
V _{REFDQ}	Supply	Reference voltage: DQ, DM V _{DD} /2.
V _{SS}	Supply	Ground.
V _{TT}	Supply	Termination voltage: Used for control, command, and address V _{DD} /2.
NC	–	No connect: These pins are not connected on the module.
NF	–	No function: These pins are connected within the module, but provide no functionality.

DQ Map

Table 6: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	10	19	U2	0	18	28
	1	13	135		1	21	144
	2	15	141		2	23	150
	3	8	13		3	16	22
	4	14	140		4	22	149
	5	12	134		5	20	143
	6	11	20		6	19	29
	7	9	14		7	17	23
U3	0	26	37	U4	0	CB2	46
	1	29	153		1	CB5	162
	2	31	159		2	CB7	168
	3	24	31		3	CB0	40
	4	30	158		4	CB6	167
	5	28	152		5	CB4	161
	6	27	38		6	CB3	47
	7	25	32		7	CB1	41
U5	0	34	89	U6	0	42	98
	1	37	205		1	45	214
	2	39	211		2	47	220
	3	32	83		3	40	92
	4	38	210		4	46	219
	5	36	204		5	44	213
	6	35	90		6	43	99
	7	33	84		7	41	93
U7	0	50	107	U8	0	2	10
	1	53	223		1	5	126
	2	55	229		2	7	132
	3	48	101		3	0	4
	4	54	228		4	6	131
	5	52	222		5	4	125
	6	51	108		6	3	11
	7	49	102		7	1	5

Table 6: Component-to-Module DQ Map, Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	58	116				
	1	61	232				
	2	63	238				
	3	56	110				
	4	62	237				
	5	60	231				
	6	59	117				
	7	57	111				

Table 7: Component-to-Module DQ Map, Back

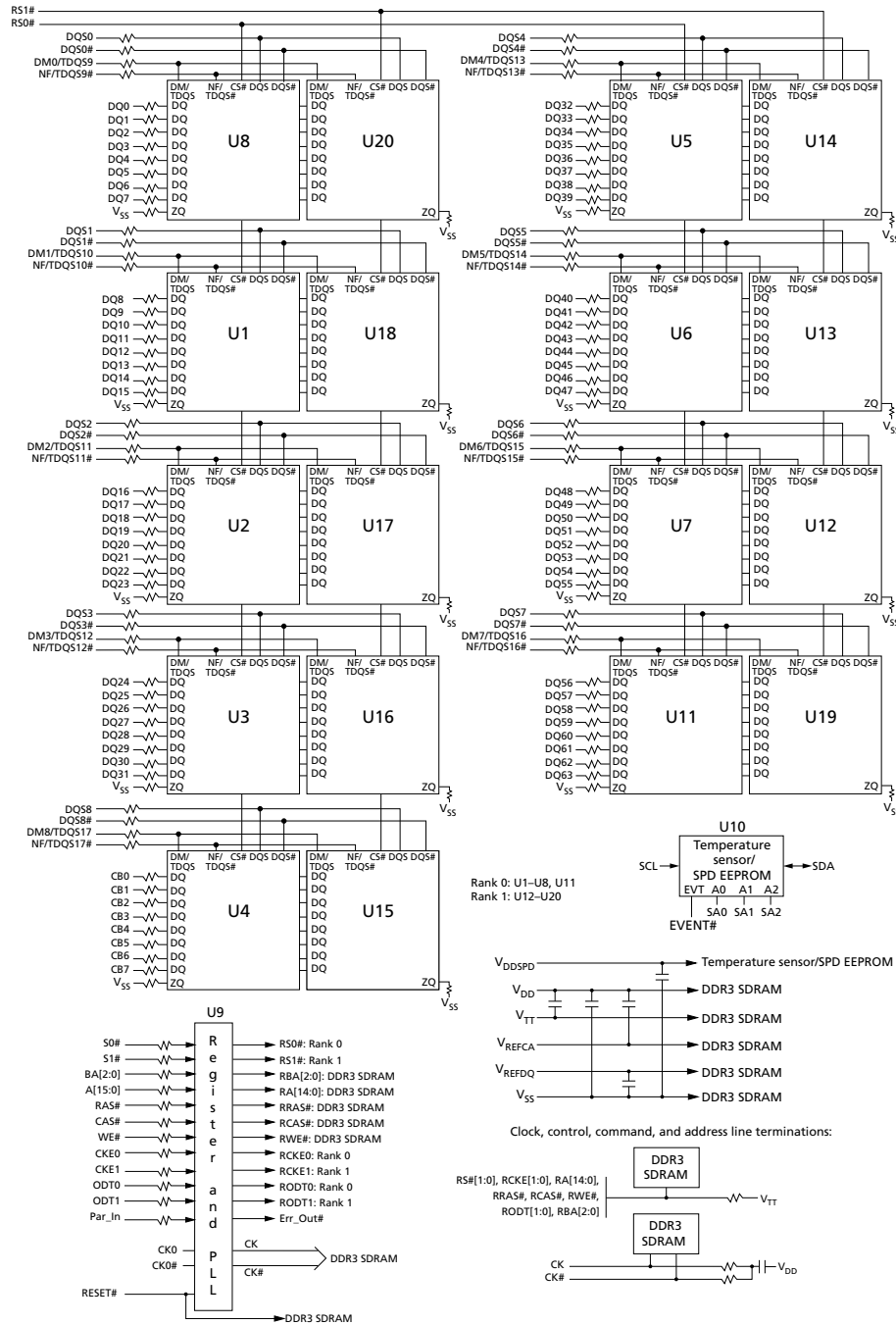
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U12	0	53	223	U13	0	45	214
	1	50	107		1	42	98
	2	48	101		2	40	92
	3	55	229		3	47	220
	4	49	102		4	41	93
	5	51	108		5	43	99
	6	52	222		6	44	213
	7	54	228		7	46	219
U14	0	37	205	U15	0	CB5	162
	1	34	89		1	CB2	46
	2	32	83		2	CB0	40
	3	39	211		3	CB7	168
	4	33	84		4	CB1	41
	5	35	90		5	CB3	47
	6	36	204		6	CB4	161
	7	38	210		7	CB6	167

Table 7: Component-to-Module DQ Map, Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U16	0	29	153	U17	0	21	144
	1	26	37		1	18	28
	2	24	31		2	16	22
	3	31	159		3	23	150
	4	25	32		4	17	23
	5	27	38		5	19	29
	6	28	152		6	20	143
	7	30	158		7	22	149
U18	0	13	135	U19	0	61	232
	1	10	19		1	58	116
	2	8	13		2	56	110
	3	15	141		3	63	238
	4	9	14		4	57	111
	5	11	20		5	59	117
	6	12	134		6	60	231
	7	14	140		7	62	237
U20	0	5	126				
	1	2	10				
	2	0	4				
	3	7	132				
	4	1	5				
	5	3	11				
	6	4	125				
	7	6	131				

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC standard "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver includes an even parity function for checking parity. The memory controller accepts a parity bit at the Par_In input and compares it with the data received on A[15:0], BA[2:0], RAS#, CAS#, and WE#. Valid parity is defined as an even number of ones (1s) across the address and command inputs (A[15:0], BA[2:0], RAS#, CAS#, and WE#) combined with Par_In. Parity errors are flagged on Err_Out#.

Address and command parity is checked during all DRAM operations and during control word WRITE operations to the registering clock driver. For SDRAM operations, the address is still propagated to the SDRAM even when there is a parity error. When writing to the internal control words of the registering clock driver, the write will be ignored if parity is not valid. For this reason, systems must connect the Par_In pins on the DIMM and provide correct parity when writing to the registering clock driver control word configuration registers.

Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I²C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.975	V

Table 9: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes	
V_{DD}	V_{DD} supply voltage	1.425	1.5	1.575	V		
I_{VT}	Termination reference current from V_{TT}	-600	-	+600	mA		
V_{TT}	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	1	
I_i	Input leakage current; Any input $0\text{V} \leq V_{IN} \leq V_{DD}$; V_{REF} input $0\text{V} \leq V_{IN} \leq 0.95\text{V}$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	TBD	TBD	TBD	μA	
		DM	-4	0	+4		
I_{OZ}	Output leakage current; $0\text{V} \leq V_{OUT} \leq V_{DD}$; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	-10	0	+10	μA	
I_{VREF}	V_{REF} supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		-18	0	+18	μA	
T_A	Module ambient operating temperature	Commercial	0	-	+70	$^{\circ}\text{C}$	2, 3
		Industrial	-40	-	+85		
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	-	+95	$^{\circ}\text{C}$	2, 3, 4
		Industrial	-40	-	+95		

- Notes:
- V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
 - T_A and T_C are simultaneous requirements.
 - For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
 - The refresh rate is required to double when $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 11: DDR3 I_{DD} Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet, Die Rev D

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I _{DD0} ¹	963	873	783	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I _{DD1} ¹	1053	1008	963	mA
Precharge power-down current: Slow exit	I _{DD2P0} ²	216	216	216	mA
Precharge power-down current: Fast exit	I _{DD2P1} ²	630	540	450	mA
Precharge quiet standby current	I _{DD2Q} ²	720	630	540	mA
Precharge standby current	I _{DD2N} ²	756	666	576	mA
Precharge standby ODT current	I _{DD2NT} ¹	558	513	468	mA
Active power-down current	I _{DD3P} ²	720	630	540	mA
Active standby current	I _{DD3N} ²	810	720	630	mA
Burst read operating current	I _{DD4R} ¹	1728	1548	1368	mA
Burst write operating current	I _{DD4W} ¹	1773	1593	1413	mA
Refresh current	I _{DD5B} ²	2043	1908	1816	mA
Self refresh temperature current: MAX T _C = 85°C	I _{DD6} ²	216	216	216	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	I _{DD6ET} ²	270	270	270	mA
All banks interleaved read current	I _{DD7} ¹	4023	3573	3123	mA
RESET low current	I _{DD8} ²	252	252	252	mA

- Notes: 1. One module rank in the active I_{DD}, the other rank in I_{DD2P0} (slow exit).
2. All ranks in this I_{DD} condition.

Registering Clock Driver Specifications

Table 12: Registering Clock Driver Electrical Characteristics

SSTE32882 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	V_{DD}	–	1.425	1.5	1.575	V
DC reference voltage	V_{REF}	–	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V
DC termination voltage	V_{TT}	–	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	$V_{REF} + 175\text{mV}$	–	$V_{DD} + 400\text{mV}$	V
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	–0.4	–	$V_{REF} - 175\text{mV}$	V
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	$V_{REF} + 100\text{mV}$	–	$V_{DD} + 0.4$	V
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	–0.4	–	$V_{REF} - 100\text{mV}$	V
High-level input voltage	$V_{IH(CMOS)}$	RESET#, MIRROR	$0.65 \times V_{DD}$	–	V_{DD}	V
Low-level input voltage	$V_{IL(CMOS)}$	RESET#, MIRROR	0	–	$0.35 \times V_{DD}$	V
Differential input crosspoint voltage range	$V_{IX(AC)}$	CK, CK#, FBIN, FBIN#	$0.5 \times V_{DD} - 175\text{mV}$	$0.5 \times V_{DD}$	$0.5 \times V_{DD} + 175\text{mV}$	V
Differential input voltage	$V_{ID(AC)}$	CK, CK#	350	–	$V_{DD} + \text{TBD}$	mV
High-level output current	I_{OH}	Err_Out#	–	–	TBD	mA
Low-level output current	I_{OL}	Err_Out#	TBD	–	TBD	mA

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I²C bus shared with the SPD EEPROM.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 13: Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V _{DDSPD}	3.0	3.6	V
Supply current: V _{DD} = 3.3V	I _{DD}	–	2.0	mA
Input high voltage: Logic 1; SCL, SDA	V _{IH}	1.45	V _{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V _{IL}	–	0.55	V
Output low voltage: I _{OUT} = 2.1mA	V _{OL}	–	0.4	V
Input current	I _{IN}	–5.0	5.0	μA
Temperature sensing range	–	–40	125	°C
Temperature sensor accuracy (class B)	–	–1.0	1.0	°C

Table 14: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t _{BUF}	4.7	–	μs
SDA fall time	t _F	20	300	ns
SDA rise time	t _R	–	1000	ns
Data hold time	t _{HD:DAT}	200	900	ns
Start condition hold time	t _{H:STA}	4.0	–	μs
Clock HIGH period	t _{HIGH}	4.0	50	μs
Clock LOW period	t _{LOW}	4.7	–	μs
SCL clock frequency	t _{SCL}	10	100	kHz
Data setup time	t _{SU:DAT}	250	–	ns
Start condition setup time	t _{SU:STA}	4.7	–	μs
Stop condition setup time	t _{SU:STO}	4.0	–	μs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

