2GB DDR2 – SDRAM registered So-RDIMM

200 Pin So-RDIMM

SEG02G72B1BH2MT-xxR

2GByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  - DDR2 667 MT/s CL5 — -30
  - DDR2 533 MT/s CL4 — -37
- Module densities
  2GB with 18 dies and 2 rank
- Standard Grade (T_A) 0°C to 70°C; (T_C) 0°C to 85°C
- Grade W (T_A) -40°C to 85°C; (T_C) -40°C to 95°C*

* The refresh rate has to be doubled when 85°C>T_C>95°C

Features:

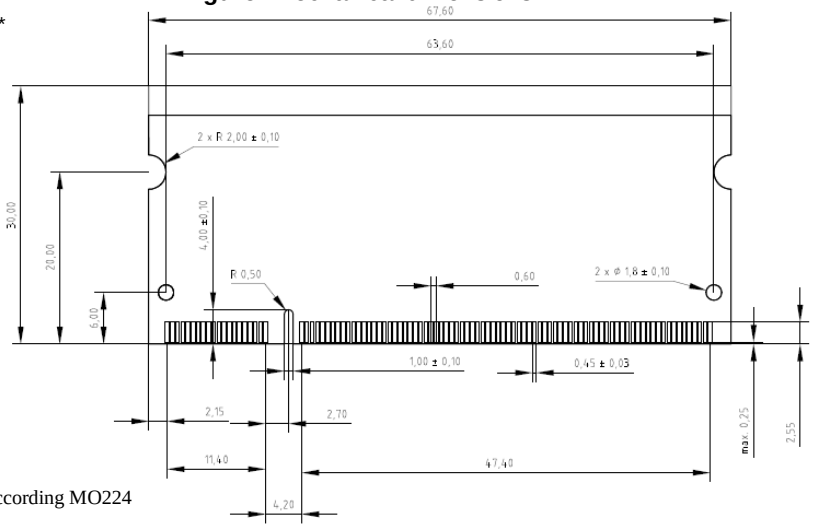
- 200-pin 72-bit Small Outline Registered Dual-In-Line Double Data Rate Synchronous DRAM Module
- Module organization: dual rank 256Mx72
- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- 1.8V I/O (SSTL_18 compatible)
- Serial Presence Detect with EEPROM
- Phase-lock loop (PLL) clock driver to reduce loading
- Supports ECC error detection and correction
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC2-5300 spec. and JEDEC- Standard MO 224. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR2 - SDRAM component base Micron MT47H128M8 DIE Rev. H**
- 128Mx8 DDR2 SDRAM in FBGA-60 package
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)

Environmental Requirements:

- Operating temperature (T_C)
  - Standard Grade 0°C to 85°C
  - Grade W -40°C to 95°C*
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Figure: mechanical dimensions



[1]the reference according MO224

This Swissbit module is an industry standard 200-pin 8-byte DDR2 SDRAM Small Outline Registered Dual-In-line Memory Module (So-RDIMM) which is organized as x72 high speed CMOS memory arrays. A Register component and a PLL chip reduce loading on the clock and command/address bus. The module uses DDR2 SDRAM devices with eight internal banks. The module uses double data rate to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.
The DDR2 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
256M x 72bit	18 x 128M x 8bit (1024Mbit)	14	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
67.6 (long) x 30.0(high) x 3.80 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEG02G72B1BH2MT-30[W]R	2 GB	5.3 GB/s	3.0ns/667MT/s	5-5-5
SEG02G72B1BH2MT-37[W]R	2 GB	4.2 GB/s	3.75ns/533MT/s	4-4-4

Pin Name

A0 - A13	Address Inputs
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM8	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 / CKE1	Clock Enable
CK0	Clock Input, positive line
CK0#	Clock Input, negative line
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0# / S1#	Chip Select
Reset#	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z.
CB0 – CB7	Check Bits

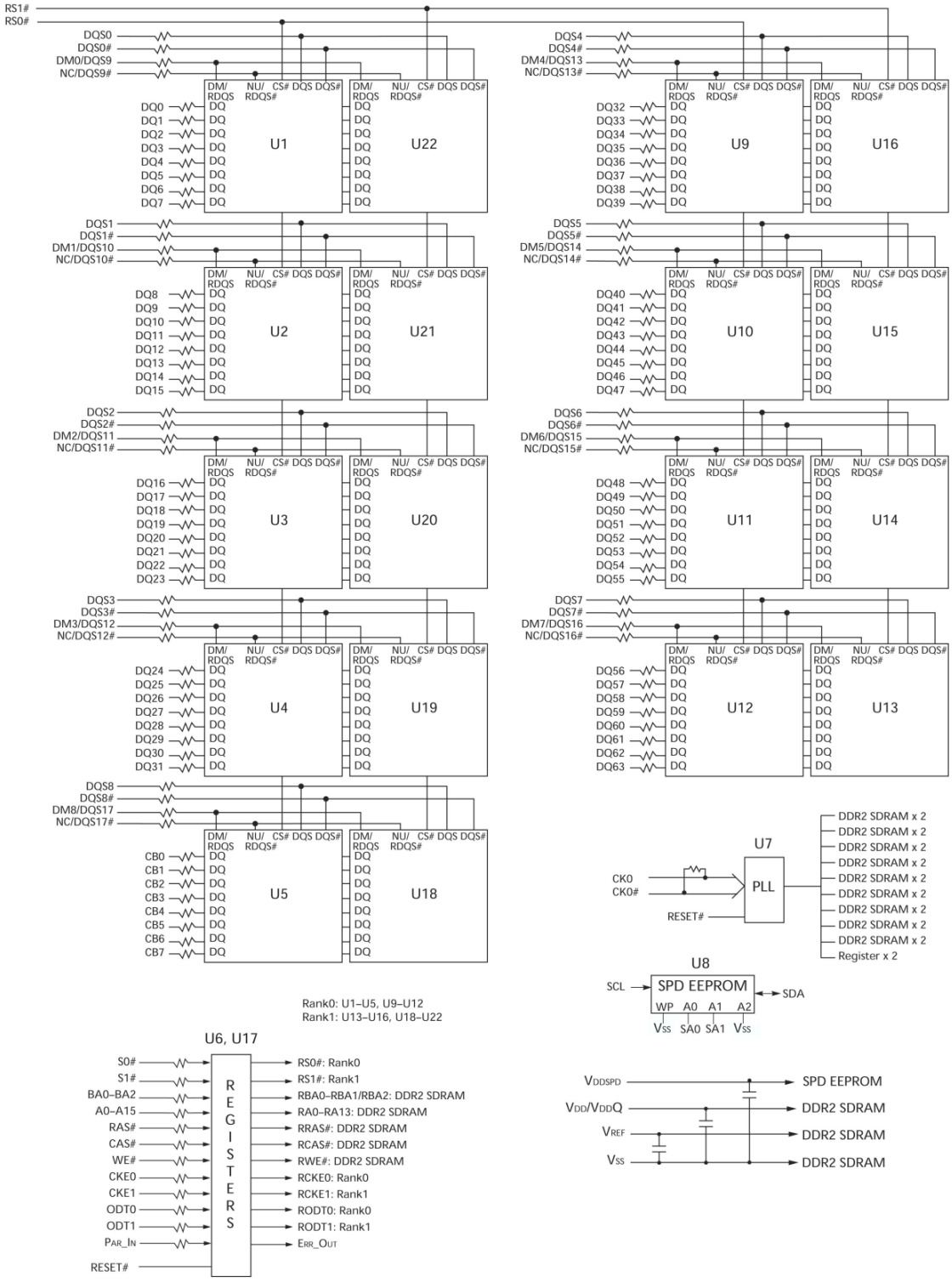
V_{DD}	Supply Voltage (1.8V± 0.1V)
V_{REF}	Input / Output Reference
V_{SS}	Ground
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0 / ODT1	On-Die Termination
NC	No Connection

Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	2	VSS	101	VDD	102	A6
3	DQ0	4	DQ4	103	A5	104	A4
5	VSS	6	DQ5	105	A3	106	VDD
7	DQ1	8	VSS	107	A2	108	A1
9	DQS0#	10	DM0	109	VDD	110	A0
11	DQS0	12	VSS	111	A10 | AP	112	BA1
13	VSS	14	DQ6	113	BA0	114	VDD
15	DQ2	16	DQ7	115	RAS#	116	WE#
17	DQ3	18	VSS	117	VDD	118	S0#
19	VSS	20	DQ12	119	CAS#	120	ODT0
21	DQ8	22	DQ13	121	S1#	122	A13
23	DQ9	24	VSS	123	VDD	124	VDD
25	VSS	26	DM1	125	ODT1	126	CK0
27	DQS1#	28	VSS	127	NC (S3#)	128	CK0#
29	DQS1	30	DQ14	129	DQ32	130	VSS
31	VSS	32	DQ15	131	VSS	132	DQ36
33	DQ10	34	VSS	133	DQ33	134	DQ37
35	DQ11	36	DQ20	135	DQS4#	136	VSS
37	VSS	38	DQ21	137	DQS4	138	DM4
39	DQ16	40	VSS	139	VSS	140	VSS
41	DQ17	42	Reset#	141	DQ34	142	DQ38
43	VSS	44	DM2	143	DQ35	144	DQ39
45	DQS2#	46	VSS	145	VSS	146	VSS
47	DQS2	48	DQ22	147	DQ40	148	DQ44
49	VSS	50	DQ23	149	DQ41	150	DQ45
51	DQ18	52	VSS	151	VSS	152	VSS
53	DQ19	54	DQ28	153	DQS5#	154	DM5
55	VSS	56	DQ29	155	DQS5	156	VSS
57	DQ24	58	VSS	157	VSS	158	DQ46
59	DQ25	60	DM3	159	DQ42	160	DQ47
61	VSS	62	VSS	161	DQ43	162	VSS
63	DQS3#	64	DQ30	163	VSS	164	DQ52

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
65	DQS3	66	DQ31	165	DQ48	166	DQ53
67	Vss	68	Vss	167	DQ49	168	Vss
69	DQ26	70	CB4	169	Vss	170	DM6
71	DQ27	72	CB5	171	DQS6#	172	Vss
73	Vss	74	Vss	173	DQS6	174	DQ54
75	CB0	76	DM8	175	Vss	176	DQ55
77	CB1	78	Vss	177	DQ50	178	Vss
79	Vss	80	CB6	179	DQ51	180	DQ60
81	DQS8#	82	CB7	181	Vss	182	DQ61
83	DQS8	84	Vss	183	DQ56	184	Vss
85	Vss	86	CB2	185	DQ57	186	DM7
87	CKE0	88	CB3	187	Vss	188	DQ62
89	CKE1	90	Vss	189	DQS7#	190	Vss
91	NC (S2#)	92	BA2	191	DQS7	192	DQ63
93	VDD	94	NC	193	DQ58	194	SDA
95	A12	96	A11	195	Vss	196	SCL
97	A9	98	VDD	197	DQ59	198	SA1
99	A7	100	A8	199	VDDSPD	200	SA0

FUNCTIONAL BLOCK DIAGRAMM 2GB DDR2 ECC Registered SoDIMM, 2 RANKS AND 18 COMPONENTS



MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	-1.0	2.3	V
I/O Supply Voltage		V_{DDQ}	-0.5	2.3	V
V_{DDL} Supply Voltage		V_{DDL}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)		I_I			µA
	Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
	CK, CK#		-20	20	
	DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	-5	5	µA
	DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level		I_{VREF}	-16	16	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V
V_{DDL} Supply Voltage	V_{DDL}	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.125		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.125	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.25	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.25	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition		Symbol	max. 4200-444	max. 5300-555	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	693	828	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	918	963	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2P}	126	126	mA
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	720	720	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	720	720	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast PDN Exit MR[12] = 0	I_{DD3P}	540	540	mA
	Slow PDN Exit MR[12] = 1		180	180	
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	900	990	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	1188	1278	mA

Parameter & Test Condition	Symbol	max. 4200-444	max. 5300-555	Unit
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	1188	1278	mA
BURST REFRESH CURRENT: $t_{CK} = t_{CK}$ (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	3870	3870	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	126	126	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RRD} = t_{RRD}$ (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	2493	2583	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

	I_{DD} MEASUREMENT CONDITIONS		
SYMBOL	**4200-444**	**5300-555**	**Unit**
CL (I_{DD})	4	5	t_{CK}
t_{RCD} (I_{DD})	15	15	ns
t_{RC} (I_{DD})	60	60	ns
t_{RRD} (I_{DD})	7.5	7.5	ns
t_{CK} (I_{DD})	3.75	3.0	ns
t_{RAS} MIN (I_{DD})	45	45	ns
t_{RAS} MAX (I_{DD})	70'000	70'000	ns
t_{RP} (I_{DD})	15	15	ns
t_{RFC} (I_{DD})	105	105	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS			4200-444		5300-555		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
Clock cycle time	CL = 5	t_{CK} (5)			3.0	8.0	ns
	CL = 4	t_{CK} (4)	3.75	8.0	3.75	8.0	ns
	CL = 3	t_{CK} (3)	5.0	8.0	5.0	8.0	ns
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Half clock period		t_{HP}	min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		ps
Access window (output) of DQ_S from CK/CK#		t_{AC}	-0.50	+0.50	-0.45	+0.45	ns
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.50 (=t_{AC} max)		+0.45 (=t_{AC} max)	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.50 (=t_{AC} min)	+0.50 (=t_{AC} max)	-0.45 (=t_{AC} min)	+0.45 (=t_{AC} max)	ns
DQ and DM input setup time relative to DQS		t_{DS}	0.10		0.10		ns
DQ and DM input hold time relative to DQS		t_{DH}	0.35		0.30		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		t_{CK}
Data hold skew factor		t_{QHS}		0.4		0.34	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data valid output window		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.3		0.24	ns
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
DQS write preamble		t_{WPRE}	0.25		0.35		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		0		ns
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Write command to first DQS latching transition			WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	0.6		0.6		t_{CK}
Address and control input setup time		t_{IS}	0.5		0.4		ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		4200-444		5300-555		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
Address and control input hold time	t_{IH}	0.5		0.4		ns
CAS# to CAS# command delay	t_{CCD}	2		2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	55		55		ns
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	7.5		7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		ns
Four bank Activate period	t_{FAW}	37.5		37.5		ns
ACTIVE to PRECHARGE command	t_{RAS}	40	70’000	40	70’000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		ns
Write recovery time	t_{WR}	15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		ns
PRECHARGE command period	t_{RP}	15		15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
LOAD MODE command cycle time	t_{MRD}	2		2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	105	70’000	105	70’000	ns
Average periodic refresh interval (0°C<= T_{CASE} <= 85 °C)	t_{REFI}		7.8		7.8	µs
(85°C<= T_{CASE} <= 95 °C)	$t_{REFI\ (IT)}$		3.9		3.9	
Exit SELF REFRESH to non-READ command	t_{XSNR}	t_{RFC}(min) + 10		t_{RFC}(min) + 10		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		t_{IS}		ps
ODT turn-on delay	t_{AOND}	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	ps
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT to power-down entry latency	t_{ANPD}	3		3		t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		4200-444		5300-555		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
ODT power-down exit latency	t_{AXPD}	8		8		t_{CK}
ODT enable from MRS command	T_{MOD}	12		12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2		2		t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	6 – AL		7 – AL		t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2		2		t_{CK}
CKE minimum high/low time	t_{CKE}	3		3		t_{CK}

Register Specifications

Parameter	Symbol	Pins	Conditions	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 125	$V_{DD}Q$ + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	-	V
Output low voltage	V_{OL}	Parity output	LVCMOS	-	0.5	V
Input current	I_I	All pins	V_I = $V_{DD}Q$ or $V_{SS}Q$	-5	+5	µA
Static standby	I_{DD}	All pins	RESET# = $V_{SS}Q$ (I_O = 0)	-	100	µA
Static operating	I_{DD}	All pins	RESET# = $V_{SS}Q$; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	-	40	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	-	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at $t_{CK/2}$, 50% duty cycle	-	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	Data	V_I = V_{REF} ±250mV; $V_{DD}Q$ = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	V_I = $V_{DD}Q$ or $V_{SS}Q$	-	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

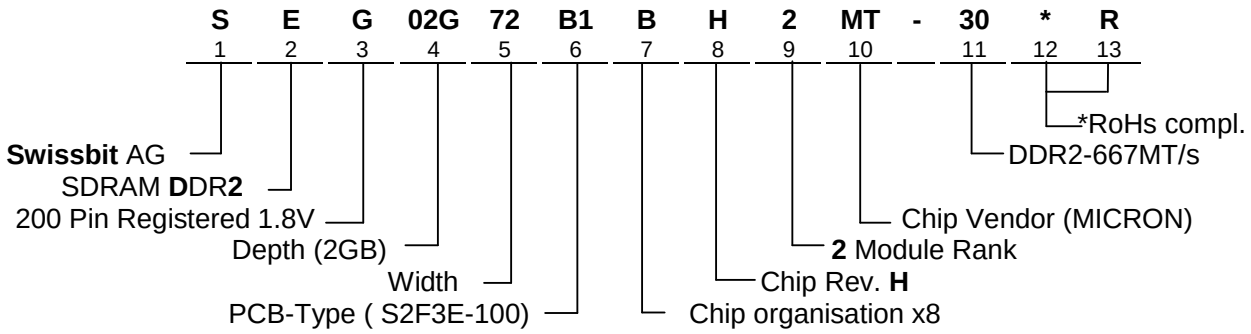
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	4200-444	5300-555
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x08	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0E	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A	
5	DIMM HIGHT AND MODULE RANKS	0x61	
6	MODULE DATA WIDTH	0x48	
7	RESERVED	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	0x05	
9	SDRAM CYCLE TIME, (t_{CK}) [max CL] CAS LATENCY = 5 (5300), CL = 4 (4200)	0x3D	0x30
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL] CAS LATENCY = 5 (5300); CL = 4 (4200)	0x50	0x45
11	MODULE CONFIGURATION TYPE	0x02	
12	REFRESH RATE / TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x08	
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00	
16	BURST LENGTHS SUPPORTED	0x0C	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08	
18	CAS LATENCIES SUPPORTED	0x18	0x38
19	MODULE THICKNESS	0x01	
20	DDR2 DIMM TYPE	0x07	
21	SDRAM MODULE ATTRIBUTES	0x04	
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03	
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x50	0x3D
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x50	0x45
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x50
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x45
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C	
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x1E	
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C	
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D	
31	MODULE BANK DENSITY	0x01	

SERIAL PRESENCE-DTECT MATRIX (continued)

BYTE	DESCRIPTION	4200-444	5300-555
32	ADDRESS AND COMMAND SETUP TIME, (t_{ISb})	0x25	0x20
33	ADDRESS AND COMMAND HOLD TIME, (t_{IHb})	0x37	0x27
34	DATA / DATA MASK INPUT SETUP TIME, (t_{DSb})	0x10	
35	DATA / DATA MASK INPUT HOLD TIME, (t_{DHb})	0x22	0x17
36	WRITE RECOVERY TIME, (t_{WR})	0x3C	
37	WRITE to READ Command Delay, (t_{WTR})	0x1E	
38	READ to PRECHARGE Command Delay, (t_{RTP})	0x1E	
39	Mem Analysis Probe	0x00	
40	Extension for Bytes 41 and 42	0x06	
41	MIN ACTIVE AUTO REFRESH TIME, (t_{RC})	0x3C	
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x7F	
43	SDRAM DEVICE MAX CYCLE TIME, (t_{CKMAX})	0x80	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t_{DQSQ})	0x1E	0x18
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t_{QHS})	0x28	0x22
46	PLL Relock Time	0x0F	
47-61	Optional Features, not supported	0x00	
62	SPD REVISION	0x13	
63	CHECKSUM FOR BYTES 0-62	0xB6	0x18
64-66	MANUFACTURER`S JEDEC ID CODE	0x7F	
67	MANUFACTURER`S JEDEC ID CODE (continued)	0xDA	
68-71	MANUFACTURER`S JEDEC ID CODE (continued)	0x00	
72	MANUFACTURING LOCATION	0x01 Switzerland | 0x02 Germany | 0x03 USA	
73-90	MODULE PART NUMBER (ASCII)	“SEG02G72B1BH2MT-30”	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00	
128-255	Open for customer use	0xFF	

Part Number Code



* optional / additional information

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