AOZ1110

4A Synchronous EZBuck Regulator

General Description

The AOZ1110QI is a high efficiency, easy to use, 4A synchronous buck regulator optimized for portable electronic devices. The AOZ1110QI works from a 2.7V to 5.5V input voltage range, and provides up to 4A of continuous output current with an output voltage adjustable down to 0.8V. With a 1% output accuracy rating, the AOZ1110 is designed for low tolerance applications, such as DSPs and FPGAs.

The AOZ1110QI is available in a 24-pin 4X4 QFN package and is rated over a -40°C to +85°C ambient temperature range.

Features

- 2.7V to 5.5V input voltage range
- 30mΩ high-side and 20mΩ low-side MOSFET
- Efficiency up to 95%
- Adjustable soft start
- Output voltage adjustable down to 0.8V
- 4A continuous output current
- Selectable 500kHz & 1MHz PWM operation
- Cycle-by-cycle current limit
- Over-voltage protection
- Short-circuit protection
- Thermal shutdown
- Power good indicator
- Small size 4x4 QFN-24 package

Applications

- Point of load DC/DC conversion for DSPs, FPGAs, ASICs and microprocessors
- DVD and HDD
- Notebook PCs
- Telecom/Networking/Datacom equipment

Green Product

Typical Application

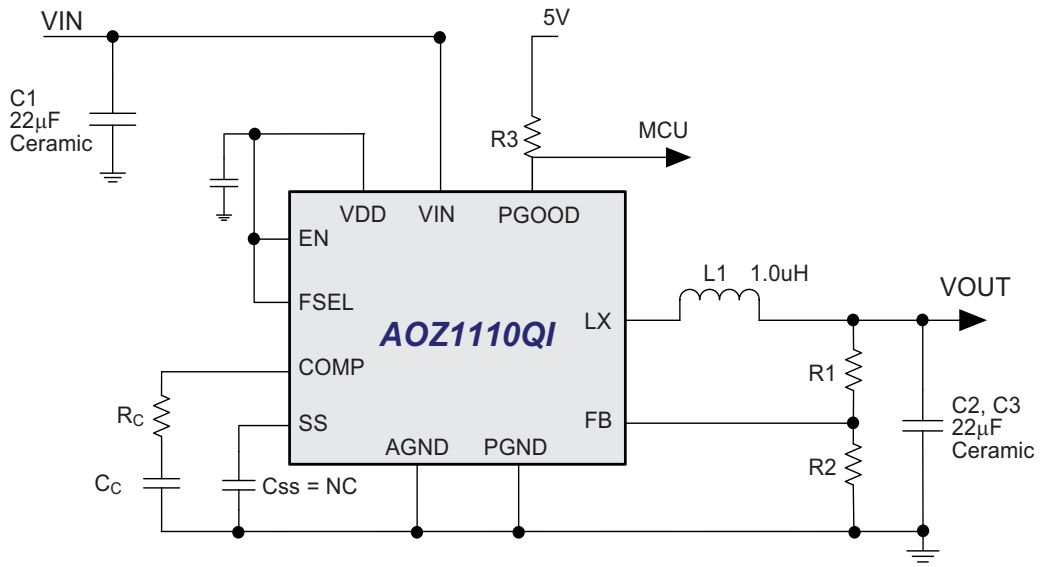


Figure 1. Typical Application

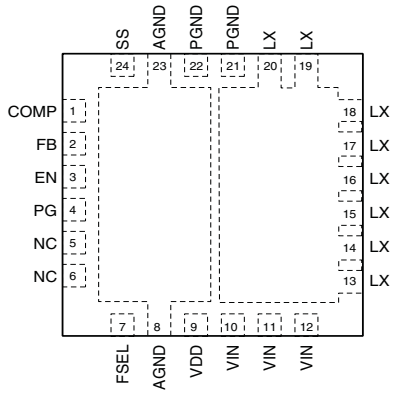
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1110QI	-40°C to +85°C	24-pin 4mm x 4mm QFN	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

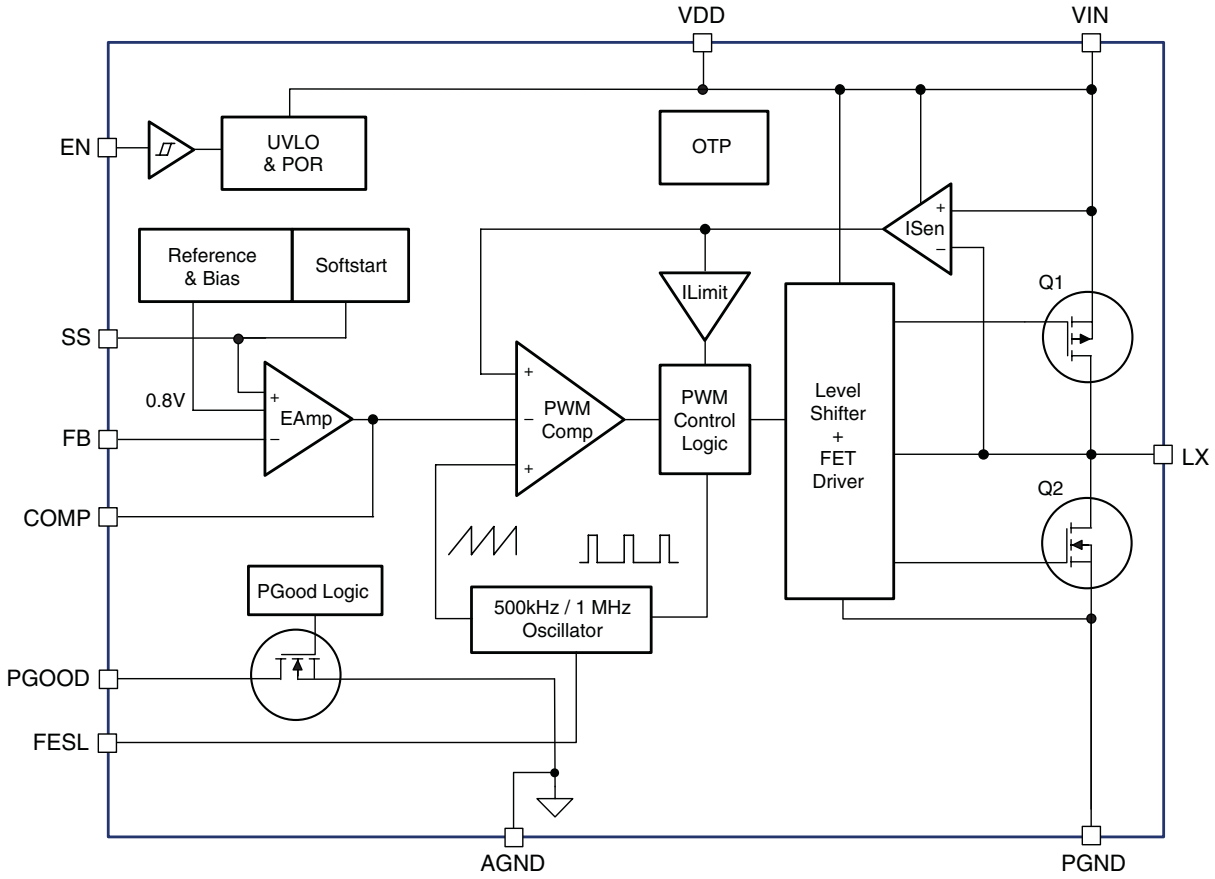


24-Pin 4mm x 4mm QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	COMP	External loop compensation pin.
2	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
3	EN	Device enable pin, active high.
4	PGOOD	Power good signal output pin. It is an open drain logic output used to indicate the status of output voltages. Connect a pull up resistor to VIN.
5,6	NC	No connect.
7	FSEL	Frequency Selection Pin. Tie this pin to ground, to set the switching frequency to 500kHz; tie this pin to VDD, to set the switching frequency to 1MHz.
8, 23	AGND	Reference connection for controller circuit. All AGND pins are connected internally. Electrically needs to be connected to PGND. Also used as thermal connection for controller circuit.
9	VDD	Supply voltage to control circuit and gate drivers. Connect a 10Ω resistor between VIN and VDD and a 0.1μF capacitor from VDD to AGND to decouple noise voltage.
10, 11, 12	VIN	Supply voltage input. All VIN pins must be connected together externally. When VIN voltage rises above the UVLO threshold the device starts up.
13, 14, 15, 16, 17, 18, 19, 20	LX	PWM output connection to inductor. All LX pins must be connected together externally. Also used as thermal connection for internal MOSFET.
21, 22	PGND	Power ground. All PGND pins must be connected together. Electrically needs to be connected to AGND.
24	SS	Soft start pin. Connect a capacitor externally to control soft start period. Leave it open for internal set soft-start time.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	6V
Supply Voltage (V_{DD})	6V
LX to GND	-0.7V to 6V
EN to GND	-0.3V to 6V
FB to GND	-0.3V to 6V
COMP to GND	-0.3V to 6V
SS to GND	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV
PGOOD	-0.3V to 6V
FSEL	-0.3V to 6V
NC	-0.3V to 6V

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	2.7V to 5.5V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance (2) 4x4 QFN-24 (Θ_{JA})	45°C/W

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

2. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 3.3V, unless otherwise specified(3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**2.7**		**5.5**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} rising V_{IN} falling	 **2.20**	**2.50** **2.30**	**2.60**	V V
I_{IN}	Supply Current (Quiescent)	V_{FB} = 1.0V, L disconnected		**1.5**	**3**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V, Active PGood = 100kΩ Excluding PG current			**1**	µA
V_{FB}	Feedback Voltage	T_A = 25°C T_A = -40°C to 85°C	0.792 0.784	0.800 0.800	0.808 0.816	V
	Load Regulation	0A < Iload < 3A, V_{IN} = 3.3V, V_{OUT} =1 .5V		0.2		%
	Line Regulation	2.7V < V_{IN} < 5.5V, V_{OUT} = 1.5V Iload = 100mA		0.2		%
I_{FB}	FB Input Current				200	nA
ENABLE						
V_{EN}	EN Input Threshold	Off threshold On threshold	 **1.2**		**0.4**	V V
V_{HYS}	EN Input Hysteresis			**200**		mV
OSCILLATOR						
f_O	Frequency	F_{SEL} = VDD	0.85	1.0	1.15	MHz
		F_{SEL} = GND	425	500	575	kHz
D_{MAX}	Maximum Duty Cycle(4)		100			%
t_{ON_MIN}	Minimum Controllable on time(4)				200	ns
ERROR AMPLIFIER						
G_{VEA}	Error Amplifier Open Loop Voltage gain(4)			60		dB
G_{EA}	Error Amplifier Transconductance(4)			200		µA / V
OVER CURRENT, OVER VOLTAGE AND OVER TEMPERATURE						
I_{LIM}	Current Limit	V_{IN} = 3.3V	5	6	7	A
	Current Limit Response Time(4)			200		ns
T_{LO}	Short Circuit Latch off Time	V_{FB} = 0V		2		ms
OVP	Over Voltage Protection			115		%
	OVP Hyteresis			3		%
	Over-Temperature shutdown limit	T_J rising T_J falling		150 100		°C °C
OSCILLATOR						
I_{SS_OUT}	Soft Start Pin Source Current	SS = 0V, C_{SS} = 0.001µF to 0.1µF	1.5	2.0	3.0	µA
I_{SS_IN}	Soft Start Pin Sink Current	V_{IN} = 2.7V, C_{SS} = 0.001µF to 0.1µF	1.5	3.0	5.0	mA
t_{SS}	Internal Soft Time	C_{SS} = open		500		µs

Electrical Characteristics *(Continued)*

T_A = 25°C, V_{IN} = V_{EN} = 3.3V, unless otherwise specified(3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
PWM OUTPUT STAGE						
$R_{DS(ON)}$	High-Side PFET On-Resistance	V_{IN} = 5V		33	64	mΩ
	High-Side PFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 5V		19	30	mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
POWER GOOD						
V_{OLPG}	PG LOW Voltage	$I_{(sink)}$ = 1.0mA			**0.3**	V
	PG Leakage Current	V = 5.5V			**±1**	µA
	PG Upper Threshold Voltage	Fraction of set point	**110**	**115**	**120**	%
	PG Lower Threshold Voltage	Fraction of set point	**80**	**85**	**90**	%
	PG Hysteresis Voltage			**3**		%
t_{PG}	PG Falling Edge Deglitch Time			**120**		µs

Notes:

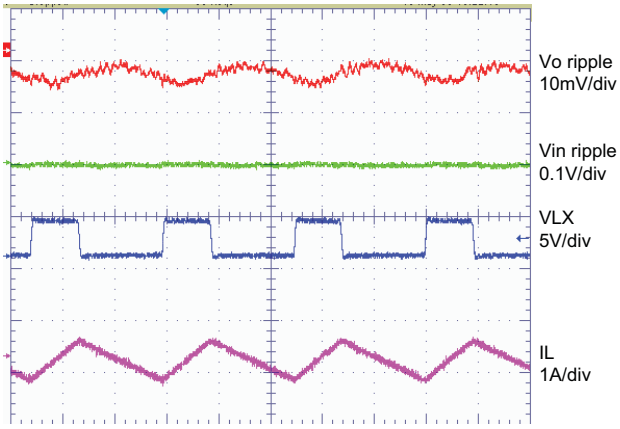
3. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

4. Guaranteed by design.

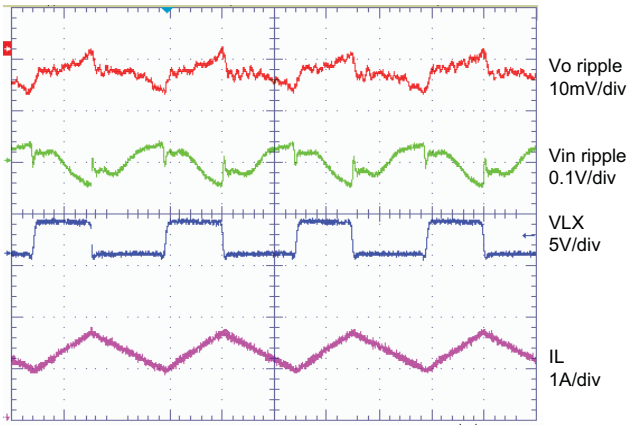
Typical Performance Characteristics

Circuit of Figure 1 with internal soft-start. T_A = 25°C, V_{IN} = V_{EN} = 3.3V, V_{OUT} = 1.2V unless otherwise specified.

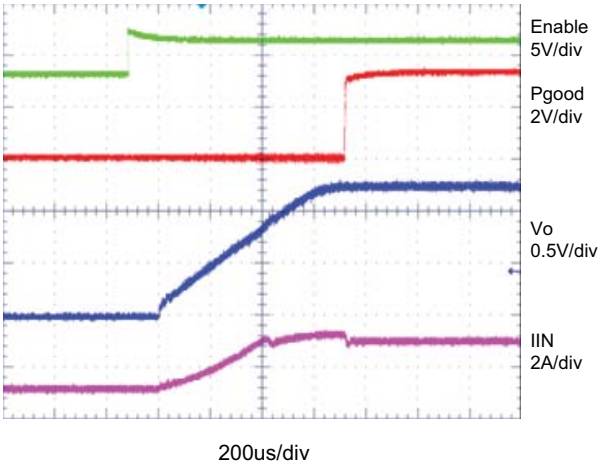
Switching Waveforms at Light Load



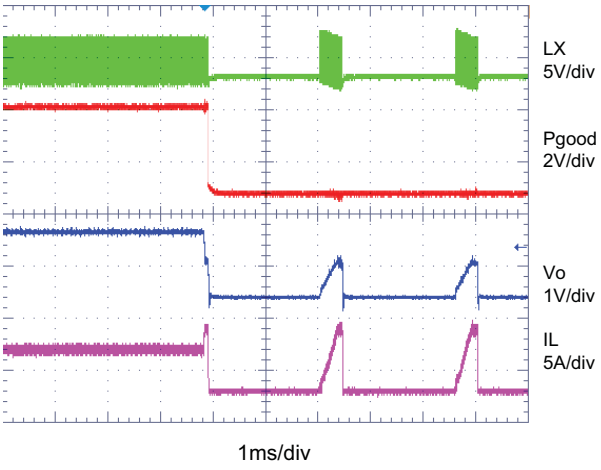
Switching Waveforms at Heavy Load



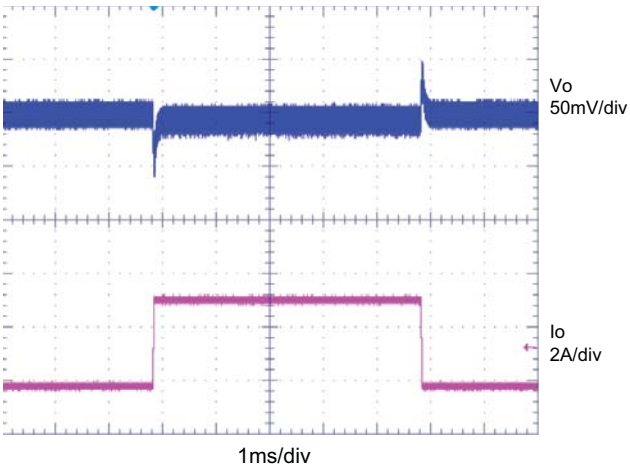
Start Up Waveforms



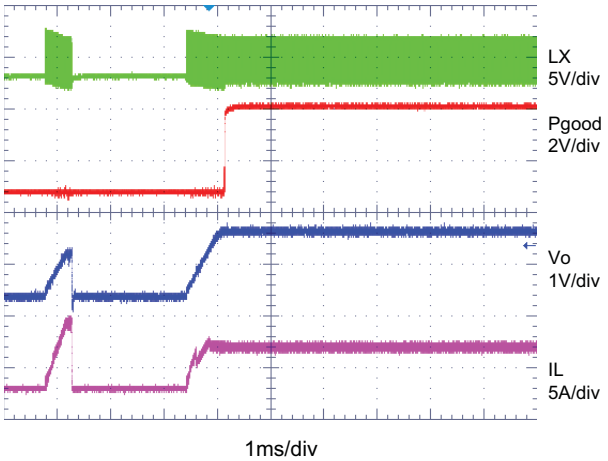
Short-Circuit Protection Waveforms



Load Transient Waveforms

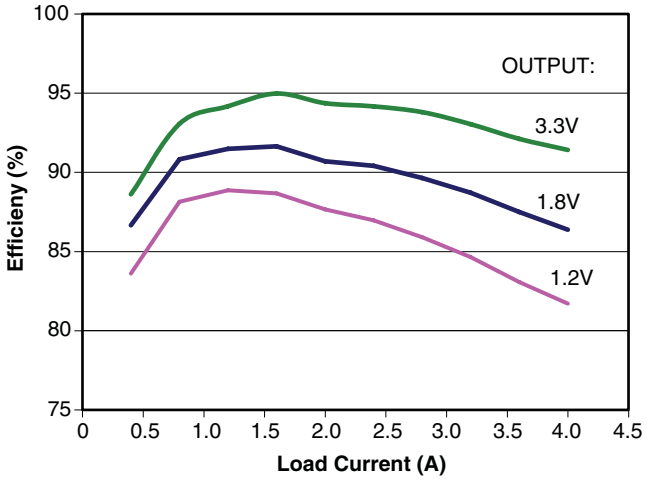


Short-Circuit Recovery Waveforms

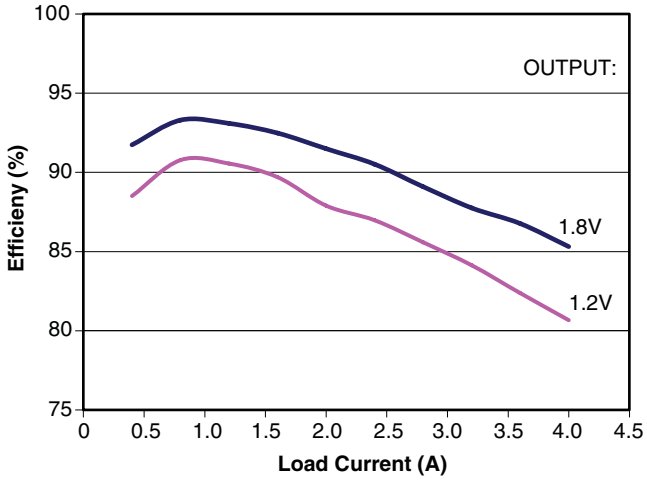


Efficiency

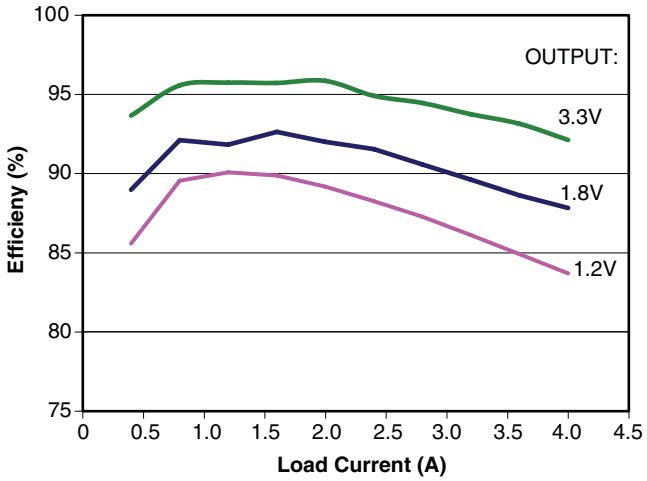
Efficiency (f_{SW} = 1MHz, V_{IN} = 5V) vs. Load Current



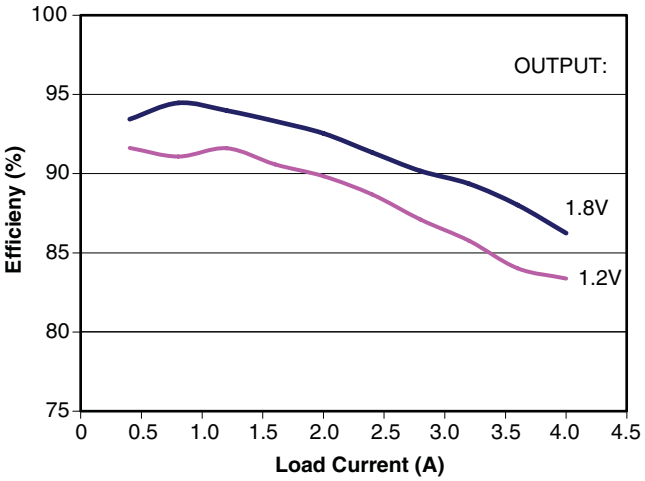
Efficiency (f_{SW} = 1MHz, V_{IN} = 3.3V) vs. Load Current



Efficiency (f_{SW} = 500kHz, V_{IN} = 5V) vs. Load Current



Efficiency (f_{SW} = 500kHz, V_{IN} = 3.3V) vs. Load Current



Detailed Description

The AOZ1110QI is a current-mode synchronous step down regulator with complimentary MOSFET switches. The operating input voltage range is 2.7V to 5.5V. The output range can be adjusted to a minimum of 0.8V and supplies up to 4A of continuous current. Features include cycle-by-cycle current limiting, short circuit protection, adjustable soft start and a power good output signal.

Enable and Soft Start

The AOZ1110QI has both internal and external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 2.5V and voltage on EN pin is HIGH. In the soft start, a 2μA internal current source charges the external capacitor at SS. As the SS capacitor is charged, the voltage at SS rises. The SS voltage clamps the reference voltage of the error amplifier, therefore output voltage rising time follows the SS pin voltage. With the slow ramping up output voltage, the inrush current can be prevented. If there is no external capacitor connected to the SS pin, the internal soft start will operate at 500μs.

Power Good

The output of power good is an open drain N-MOSFET, which supplies an active high power good stage. A pull-up resistor (R3) should connect this pin to a DC power trail with maximum voltage no higher than 6V. The AOZ1110QI monitors the FB voltage: when the FB pin voltage is lower than 85% of the target voltage or higher than 115% of the target voltage, N-MOSFET turns on and the power good pin is pulled low, which indicates the power is abnormal.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1110QI integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal low-side N-MOSFET switch to output. The internal adaptive FET driver guarantees no turn on overlap of both high-side and low-side switch.

Comparing with regulators using freewheeling Schottky diodes, the AOZ1110QI uses freewheeling N-MOSFET to realize synchronous rectification. It greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ1110QI uses a P-MOSFET as the high-side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an N-MOSFET switch.

Switching Frequency

The AOZ1110QI switching frequency can be selected by FSEL pin. When the FSEL logic is tied to VDD, the switching frequency will be 1.0 MHz. When the FSEL logic is tied to GND, the switching frequency will be 0.5 MHz.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin by using a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R1 with equation below.

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1, R_2 and most used output voltage values are listed in Table 1.

Table 1.

Vo (V)	R_1 (kΩ)	R_s (kΩ)
0.8	1.0	open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.1	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop on upper P-MOSFET and inductor.

Protection Features

The AOZ1110QI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1110QI employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0V and 2.2V internally. The peak inductor current is automatically limited cycle by cycle.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 2.5V, the converter starts operation. When input voltage falls below 2.3V, the converter will be shut down.

Output Over Voltage Protection (OVP)

The AOZ1110QI monitors the feedback voltage: when the feedback voltage is higher than 15% of set value, it immediately turns off P-MOSFET cycle by cycle to protect the output voltage overshoot at fault condition.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down both high side P-MOSFET and low side N-MOSFET if the junction temperature exceeds 150ºC. The regulator will restart automatically under the control of soft start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1110QI application circuit is show in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the V_{IN} pin and PGND pin of AOZ1110QI to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

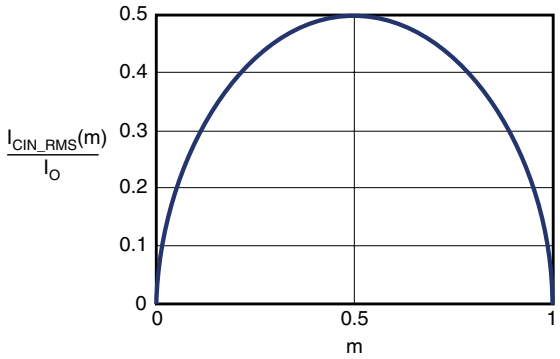


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where;

C_O is output capacitor value,

and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \left(\frac{1}{8 \times f \times C_O}\right)$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ1110QI employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value,

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for the AOZ1110QI. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1110QI, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200×10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V,

and, C_C is the compensation capacitor in Figure1.

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency. The strategy for choosing R_c and Cc is to set the cross over frequency with Rc and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

f_C is desired crossover frequency. For best performance, f_C is set to be about 1/10 of switching frequency,

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200×10^{-6} A/V;

G_{CS} is the current sense circuit transconductance, which is 10 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected cross-over frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{p1}}$$

The equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ1110QI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low-side N-MOSFET. Current flows in the second loop when the low side N-MOSFET is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1110QI.

In the AOZ1110QI buck regulator circuit, the major power dissipating components are the AOZ1110QI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power:

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor:

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1012D and thermal impedance from junction to ambient:

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

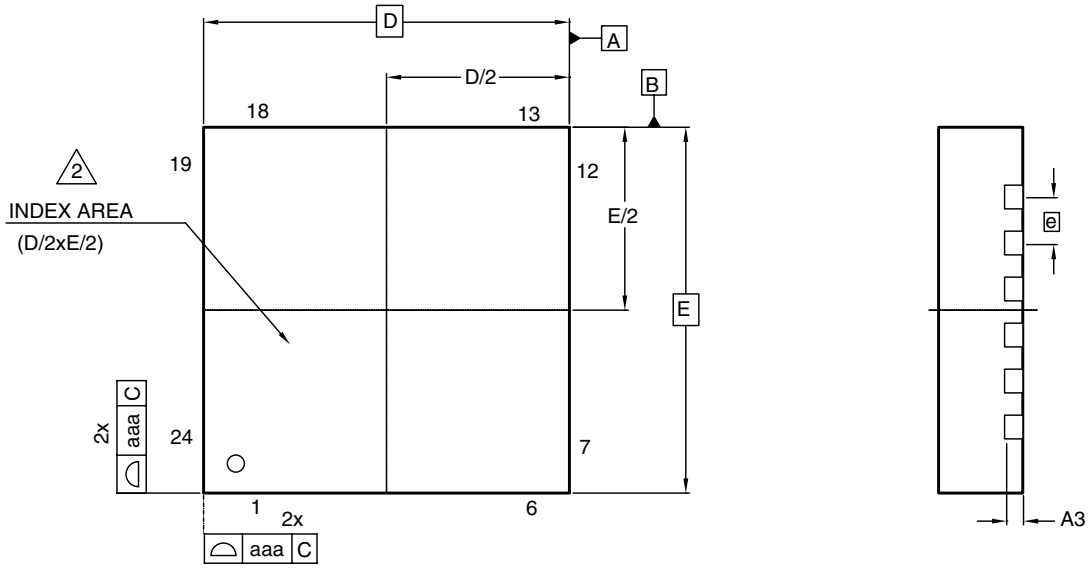
The maximum junction temperature of AOZ1110QI is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ1110QI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

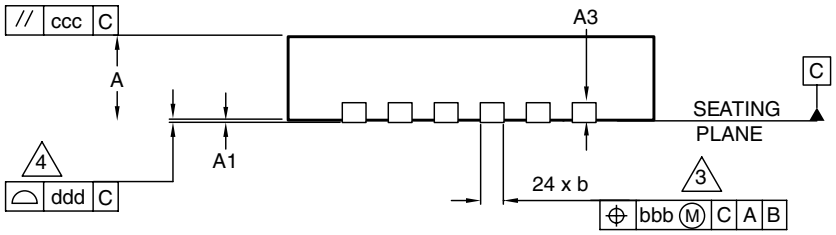
Several layout tips are listed below for the best electric and thermal performance.

1. The LX pins are connected to internal P-MOSFET and N-MOSFET drains. They are low resistance thermal conduction path and most noisy switching node. Connect a large copper plane to LX pin to help thermal dissipation. For full load (4A) application, also connect the LX pads to the bottom layer by thermal vias to enhance the thermal dissipation.
2. Do not use thermal relief connection to the VIN and the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.
3. Input capacitor should be connected to the VIN pin and the PGND pin as close as possible.
4. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
5. Make the current trace from LX pins to L to Co to the PGND as short as possible.
6. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
7. Keep sensitive signal trace far away form the LX pins.

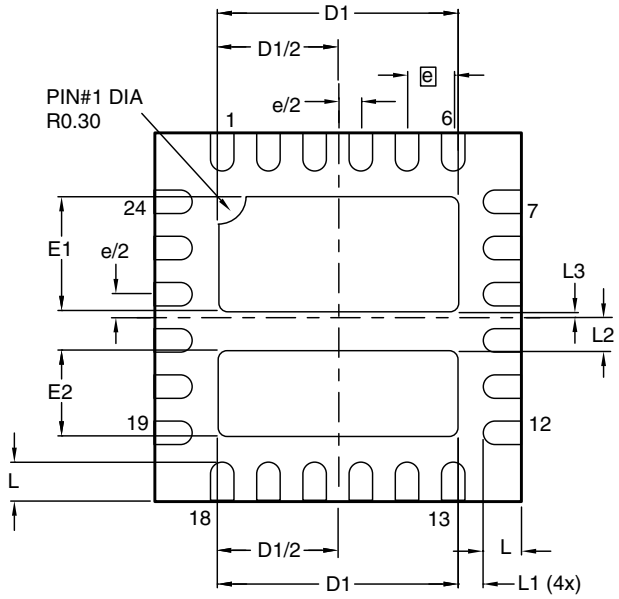
Package Dimensions, QFN 4x4-24L



TOP VIEW



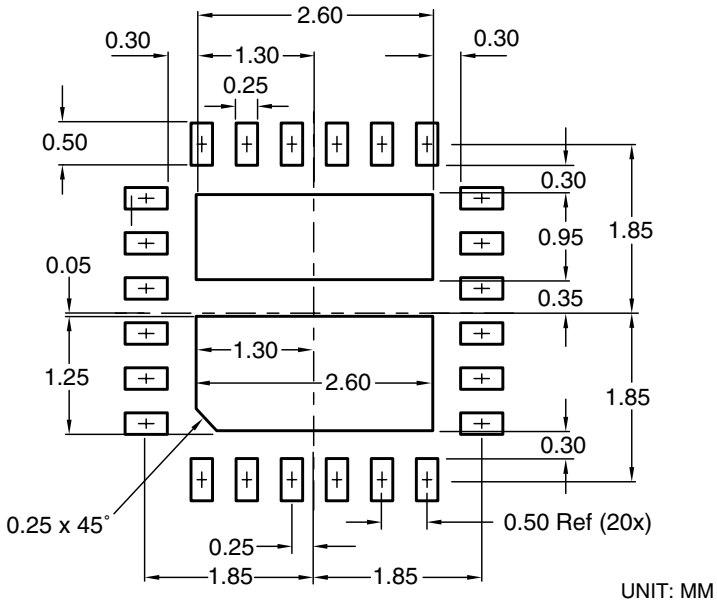
SIDE VIEW



BOTTOM VIEW

Package Dimensions, QFN 4x4-24L *(Continued)*

RECOMMENDED LAND PATTERN



UNIT: MM

Dimensions in millimeters

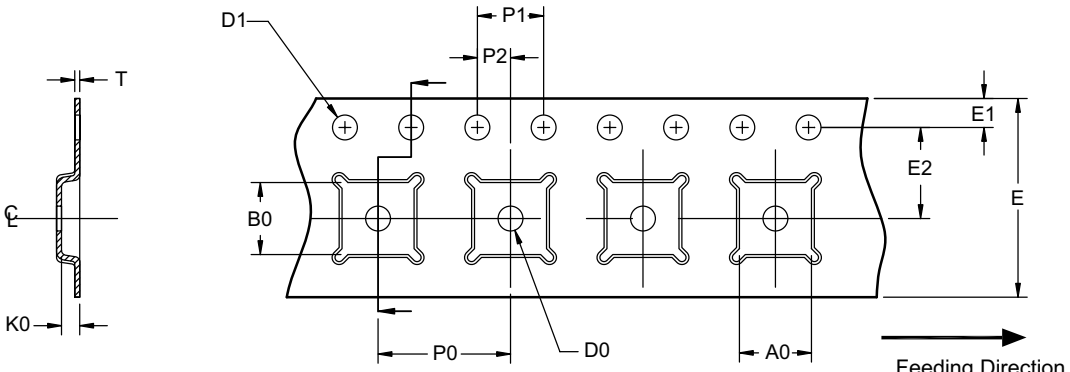
Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D1	2.50	2.60	2.70
E		4.00 BSC	
E1	1.15	1.25	1.35
E2	0.85	0.95	1.05
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.20	0.30	0.40
L2	0.25	0.35	0.45
L3	---	0.05	0.15
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF.	
b	0.008	0.010	0.012
D		0.157 BSC	
D1	0.098	0.102	0.106
E		0.157 BSC	
E1	0.045	0.049	0.053
E2	0.033	0.037	0.041
e		0.020 BSC	
L	0.014	0.016	0.018
L1	0.008	0.012	0.016
L2	0.010	0.014	0.018
L3	---	0.002	0.006
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Tape and Reel Dimensions, QFN 4x4-24L

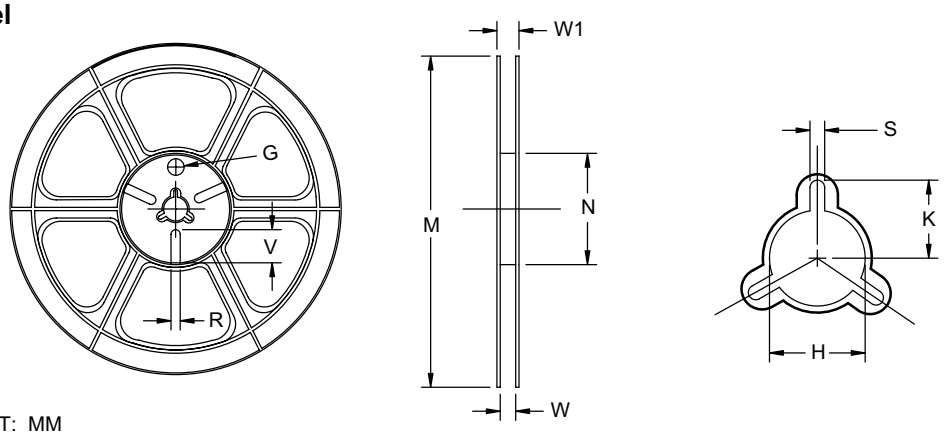
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN 4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.1/-0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

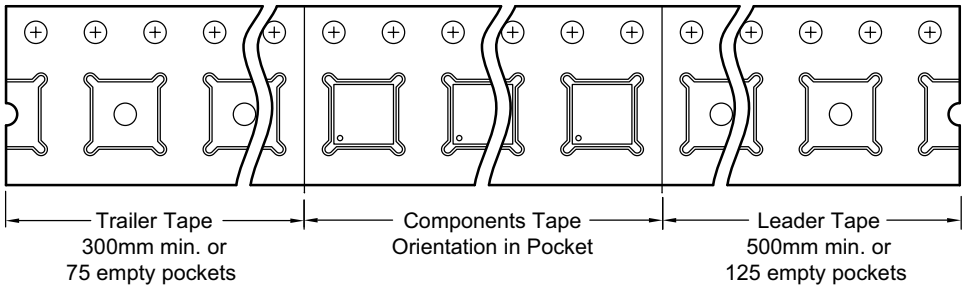
Reel



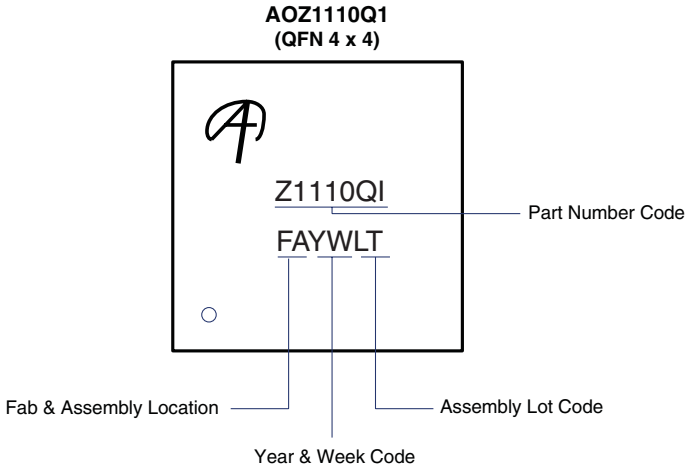
UNIT: MM

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation



Part Marking



This datasheet contains preliminary data; supplementary data may be published at a later date.
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.