1-chip High-current System with High Withstand Voltage

STEP DOWN CONVERTER Power Supply IC

BD9322EFJ, BD9323EFJ, BD9324EFJ

Pb Free
ROHM Electronic Components

DESIGN INFORMATION

●Description

The BD9322EFJ, BD9323EFJ and BD9324EFJ are step-down regulators that integrate a low resistance high side N-channel MOSFET.
It achieves 2A / 3A / 4A continuous output current over a wide input supply range.
Current mode operation provides fast transient response and easy phase compensation.

●Features

1) Wide operating INPUT Range **4.75V～18V**
2) Selectable **2A / 3A / 4A** Output Current
3) Selectable **0.1Ω / 0.15Ω** Internal MOSFET Switch
4) Low ESR Output Ceramic Capacitors are Available
5) Low Stanby Current during Shutdown Mode
6) **380kHz** Operating Frequency
7) Feedback voltage 0.9V **±1.5%** Accuracy
8) Protection circuit: Undervoltage lockout protection circuit
   Thermal shutdown circuit
   Overcurrent protection circuit
9) HTSOP-J8 Package (with Exposed thermal PAD)

●Applications

Distributed Power System
Pre-Regulator for Linear Regulator

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	20	V
Switch Voltage	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd	3760*	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃
BST Voltage	V_{BST}	V_{SW}+7	V
All other pins	V_{OTH}	7	V

* Derating in done 30.08 mW/℃ for operating above Ta≧25℃(Mount on 4-layer 70.0mm×70.0mm×1.6mm board)

● Operation Range(Ta= -40～85℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	4.75	12	18	V
Output current for BD9322EFJ	I_{SW2}	—	—	2**	A
Output current for BD9323EFJ	I_{SW3}	—	—	3**	A
Output current for BD9324EFJ	I_{SW4}	—	—	4**	A

** Pd, ASO should not be exceeded

● Electrical characteristics (unless otherwise specified VIN=12V Ta=25℃)

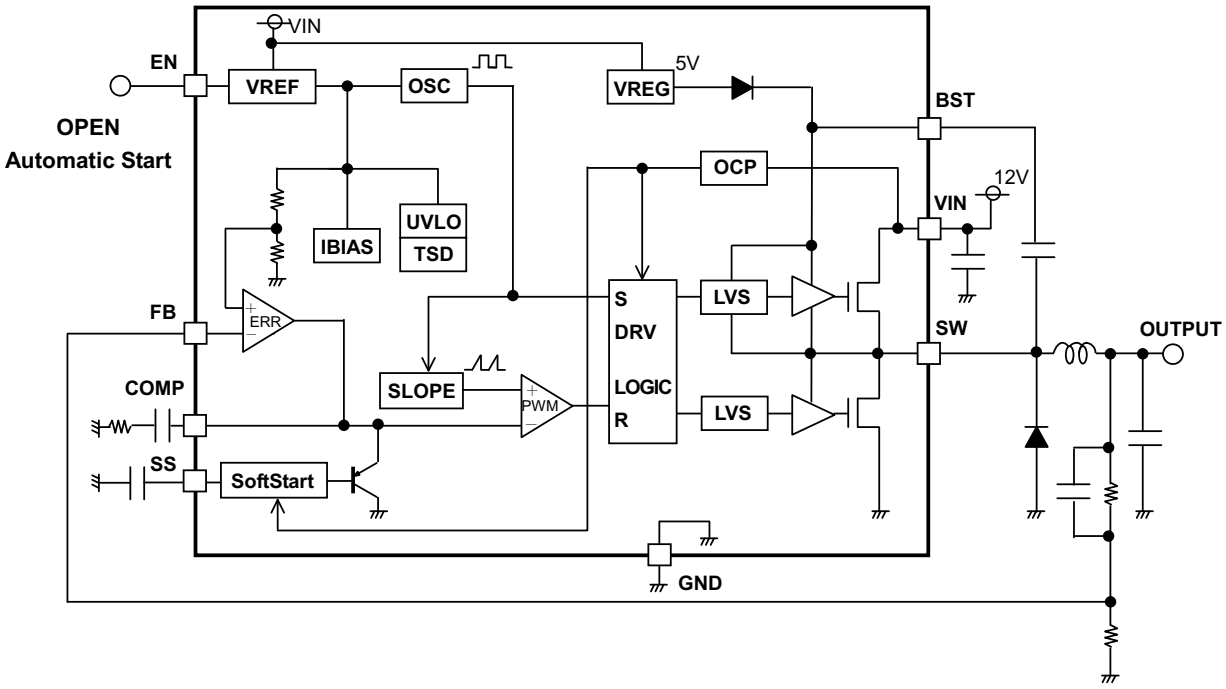
Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.1	2	μA	
Feedback voltage	V_{FB}	0.886	0.900	0.914	V	Voltage follower
SW block – SW						
Hi-side FET On-resistance for BD9322EFJ	R_{ON2}	-	0.15	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9323EFJ	R_{ON3}	-	0.10	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9324EFJ	R_{ON4}	-	0.10	-	Ω	I_{SW}= -0.8A ***
Lo-side FET On-resistance	R_{ONL}	-	10	-	Ω	I_{SW}= 0.1A
Leak current N-channel	I_{LEAKN}	-	0	10	μA	V_{IN}= 18V , V_{SW} = 0V
Switch Current Limit for BD9322EFJ	I_{LIMIT2}	2.5	-	-	A	***
Switch Current Limit for BD9323EFJ	I_{LIMIT3}	3.5	-	-	A	***
Switch Current Limit for BD9324EFJ	I_{LIMIT4}	4.5	-	-	A	***
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Pull-up current	I_{EN}	12	23	34	μA	V_{EN}= 0V
Enable Threshold voltage	V_{EN}	0.6	0.63	0.66	V	
Under Voltage Lockout threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	uA	V_{SS}= 0.1 V
Soft Start Time	T_{SS}	-	1.6	-	ms	C_{SS}= 0.1 uF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= OPEN
Quiescent Current	I_{QUI}	-	100	190	μA	V_{EN}= 0V

*** See the series line-up table below.

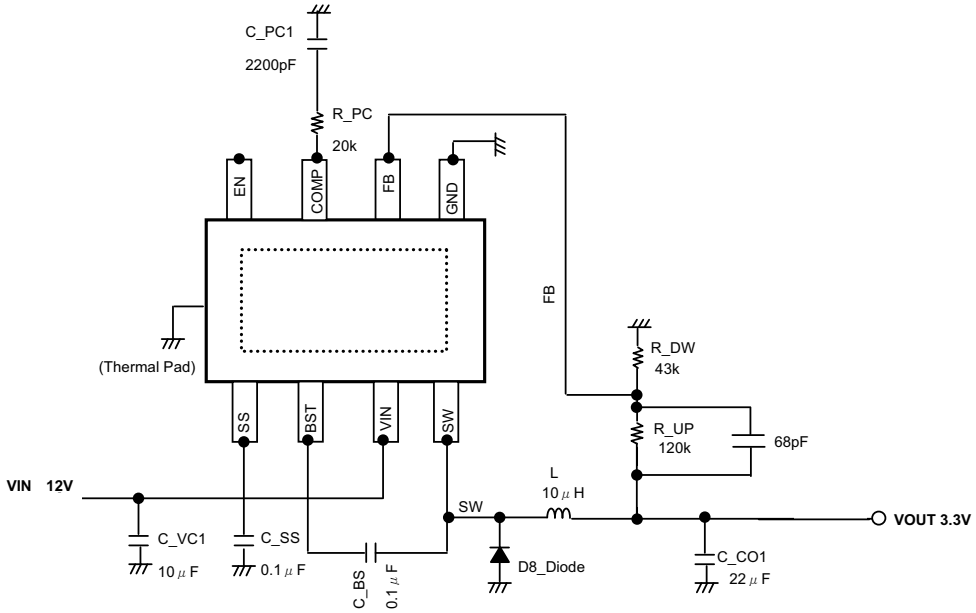
● Series Line-up Table

LINE-UP	BD9322EFJ	BD9323EFJ	BD9324EFJ
FET ON-RESISTANCE	0.15 Ω	0.10 Ω	0.10 Ω
OUTPUT CURRENT	2.0 A	3.0A	4.0 A

● Block Diagram



● Typical Application Circuit



● Block Operation

•VREG

A block to generate constant-voltage for DC/DC boosting.

•VREF

A block that generates internal reference voltage of 2.9 V (Typ.).

•TSD/UVLO

TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175℃ (Typ.)
The UVLO circuit shuts down the IC when the Vcc is Low Voltage.

•Error amp block (ERR)

This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

•Oscillator block (OSC)

This block generates the oscillating frequency.

•SLOPE block

This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

•PWM block

The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

•DRV block

A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

•Soft start circuit

Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

● Physical Dimension (TBD)

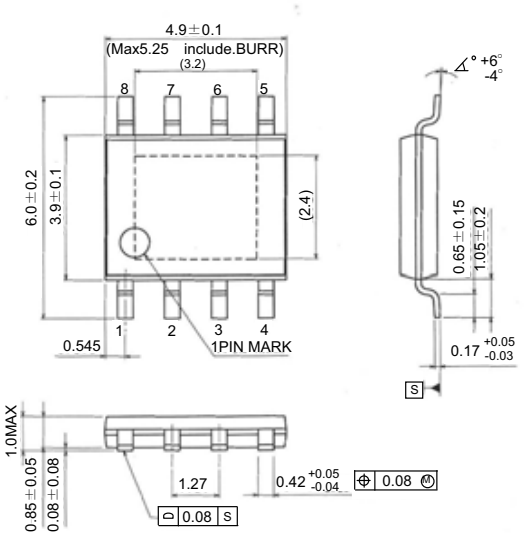


Fig HTSOP-J8 Package (TBD)
(Unit:mm)

● Pin Assignment and Pin Function

Pin No.	Pin name	Function
1	SS	Soft Start Control Input
2	BST	High-Side Gate Drive Boost Input
3	VIN	Power Input
4	SW	Power Switching Output
5	GND	Ground
6	FB	Feed Back Input
7	COMP	Compensation Node
8	EN	Enable Input

● Typical Performance Characteristics (Unless otherwise specified, VIN= 12V Ta = 25℃)

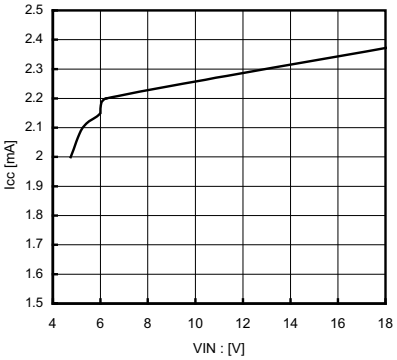


Fig. Circuit Current
(No switching)

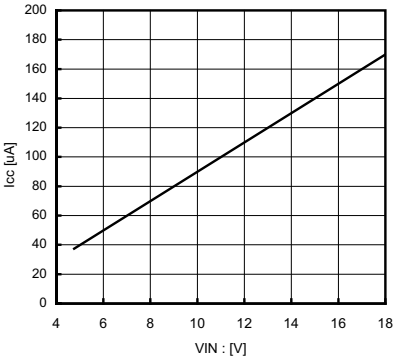


Fig. Quiescent Current
(IC not active)

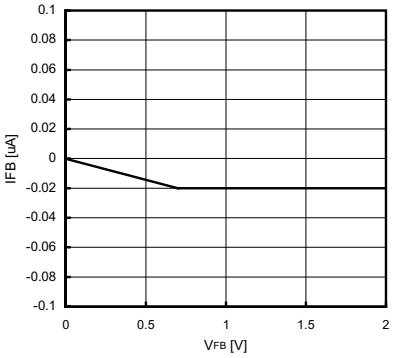


Fig. Input Bias Current

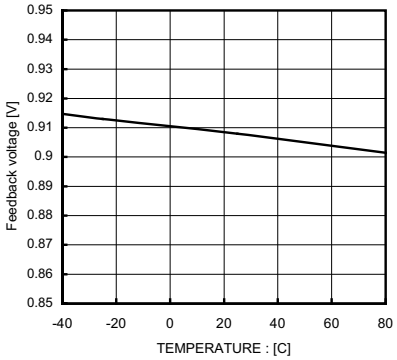


Fig. Feedback voltage

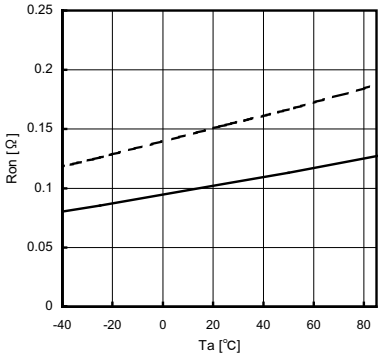


Fig. Hi-Side On-resistance

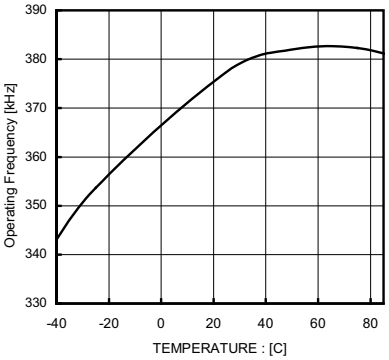


Fig. Operating Frequency

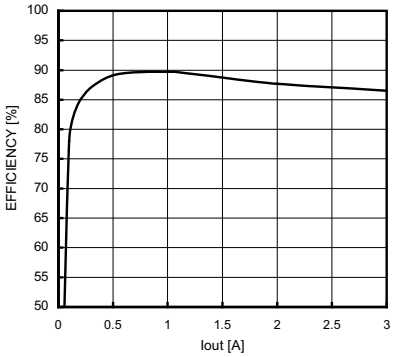


Fig. STEP Down Efficiency
(VIN= 12V VOUT= 3.3V L= 22uH)

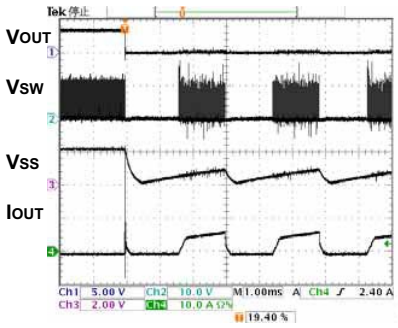


Fig. OverCurrent Protection
(VOUT is shorted to GND)

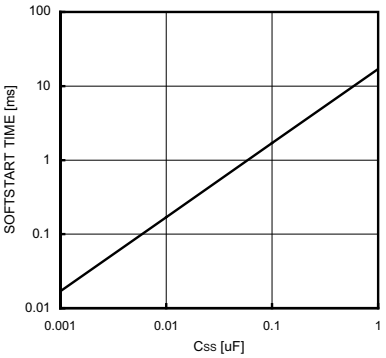


Fig. Soft Start Time

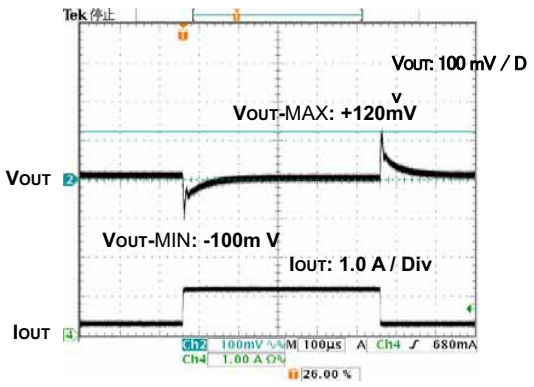


Fig. Transient Response
(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF Iout= 0.2-1.0A)

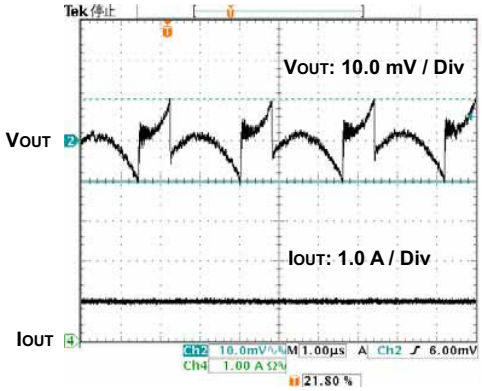


Fig. Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF I out= 1.0A)

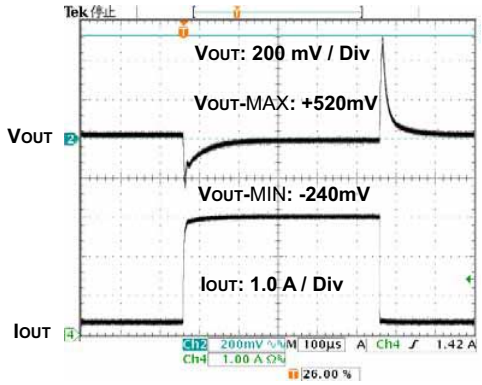


Fig. Transient Response
(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF Iout= 0.2-3.0A)

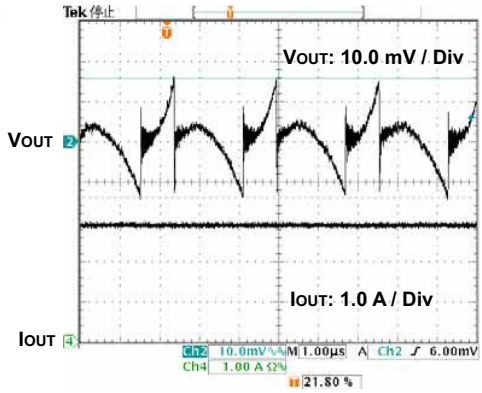


Fig. Output Ripple Voltage
(VIN= 12V VOUT= 3.

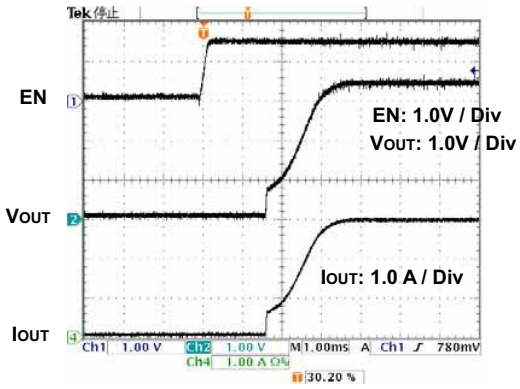


Fig. Start Up waveform
(VIN= 12V VOUT= 3.3V L= 10uH CSS= 0.1uF)

● Selecting Application Components

(1) Output LC constant (Buck Converter)

The inductance L to use for output is decided by the rated current I_{LR} and input current maximum value I_{OMAX} of the inductance.

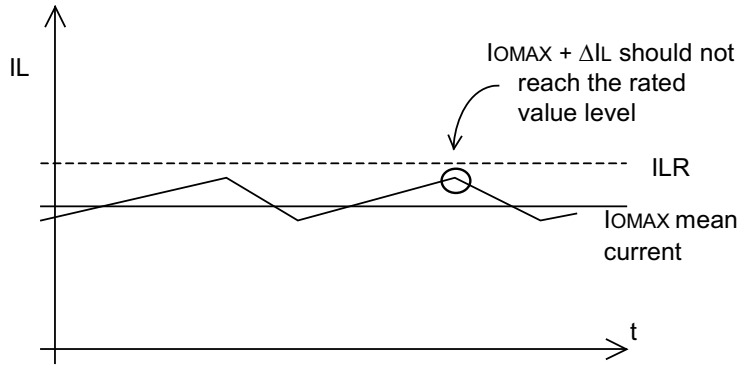


Fig.

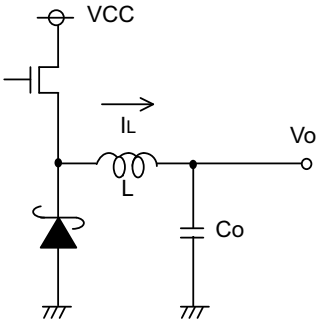


Fig.

Adjust so that $I_{OMAX} + \Delta I_L$ does not reach the rated current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (Vcc - Vo) \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage V_{DR} during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\ us \quad [V]$$

However, 10μs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2) Phase compensation

Phase Setting Method

The following conditions are required in order to ensure the stability of the negative feedback circuit.

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).

Because DC/DC converter applications are sampled using the switching frequency, the overall GBW should be set to 1/10 the switching frequency or lower. The target application characteristics can be summarized as follows:

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
- The GBW at that time (i.e., the frequency of a 0-dB gain) is 1/10 of the switching frequency or below.

In other words, because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies to raise response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting a phase advances).
The GBW (i.e., the frequency with the gain set to 1) is determined by the phase compensation capacitance connected to the error amp. Increase the capacitance if a GBW reduction is required.

(a) Standard integrator (low-pass filter)

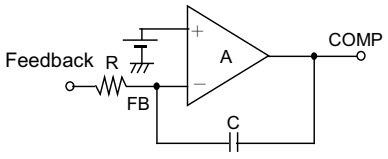


Fig.

(b) Open loop characteristics of integrator

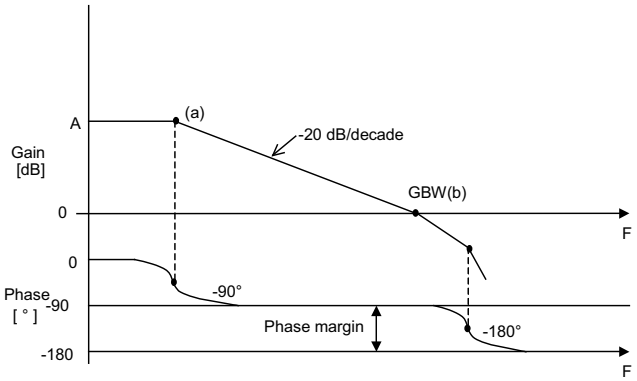


Fig.

Point (a) $fa = \frac{1}{2\pi RCA}$ [Hz]

Point (b) $fb = GBW = \frac{1}{2\pi RC}$ [Hz]

The error amp performs phase compensation of types (a) and (b), making it act as a low-pass filter.

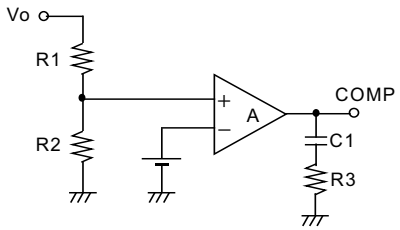


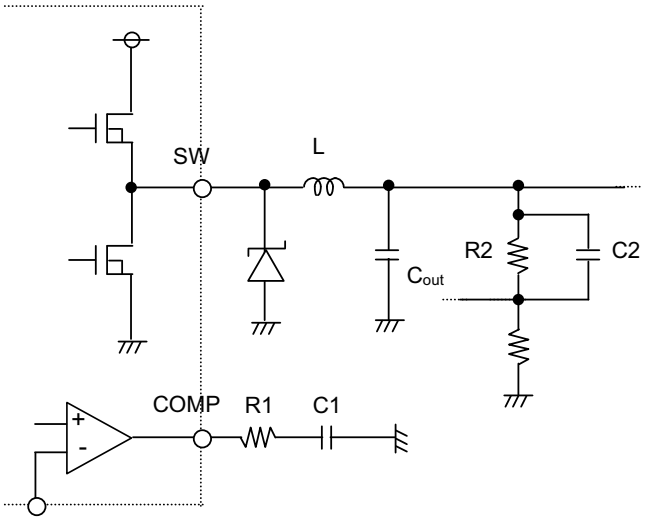
Fig.

LC resonant frequency $fp = \frac{1}{2\pi\sqrt{LC}}$ [Hz]

Phase advance $fz = \frac{1}{2\pi C_1 R_3}$ [Hz]

Set a phase advancing frequency close to the LC resonant frequency for the purpose of canceling the LC resonance.

● Selecting the Feedforward Capacitor



For a stable converter loop and the best transient response, the bypass capacitors for phase compensation are needed.

The regulator loop can be compensated by adjusting the external components connected to COMP pin. C1 is decided by the following formula.

$$C1 = \frac{1}{2\pi \cdot F_{z1} \cdot R1} \quad [F]$$

$$F_{z1} = 1/3 \cdot F_{LC} \quad [Hz]$$

$$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{out}}} \quad [Hz]$$

Across the upper resistor R2, a bypass capacitor is needed to have a better transient response.
C2 will set a zero in the loop together with R2.

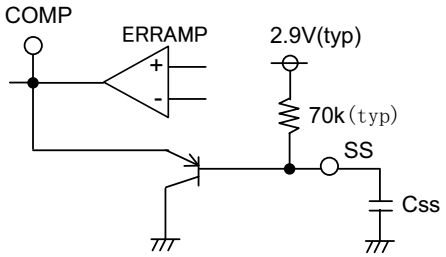
$$C2 = \frac{1}{2\pi \cdot F_{z2} \cdot R2} \quad [F]$$

$$F_{z2} = 3 \cdot F_{LC} \quad [Hz]$$

$$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{out}}} \quad [Hz]$$

※Depending on the PCB patterns or conditions,
the further adjustment beyond the calcurated value above might be needed.

● Soft Start Function



The buck converter has an adjustable SoftStart function to prevent high inrush current during start up.

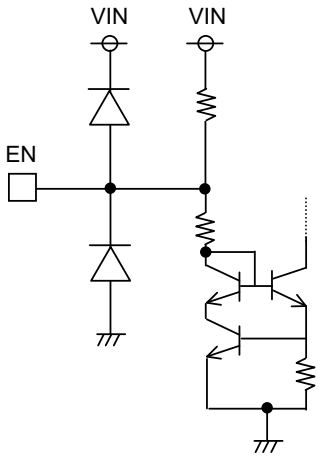
The soft-start time is set by the external capacitor connected to SS pin.

The soft start time is given by;

$$Tss\ [ms] = 16.2 \cdot Css\ [uF]$$

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.

● EN Function



The equivalent internal circuit.

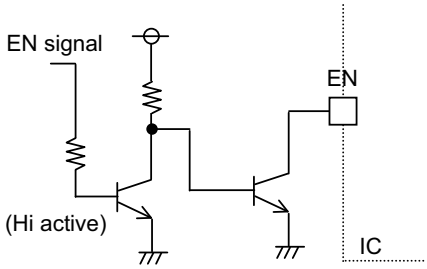
The EN terminal controls IC's shut down.

Leaving EN terminal open, makes IC start up automatically.

To shut down the IC, the external component has to pull the current from EN terminal and make the EN voltage low.

The EN threshold voltage is 0.63V (typ.).

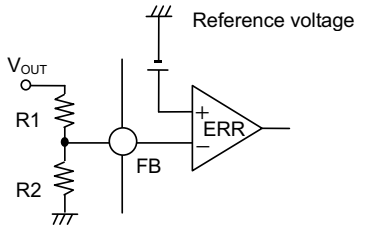
ex)



The example of EN driving circuit.

(3) Design of Feedback Resistance constant

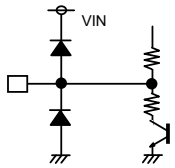
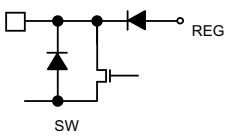
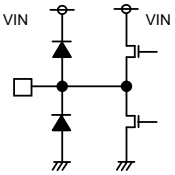
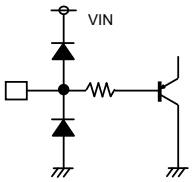
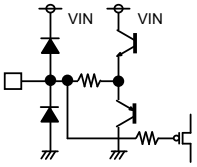
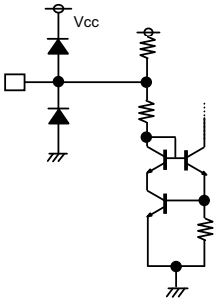
Set the feedback resistance as shown below.



$$V_{OUT} = \frac{R1 + R2}{R2} \times \text{Reference Voltage} \quad [V]$$

Fig.

● I/O Equivalent Circuit Diagram Fig.

1.SS	2.BST	4.SW
		
6.FB	**7.COMP**	**8.EN**
		

● Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Fig. , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

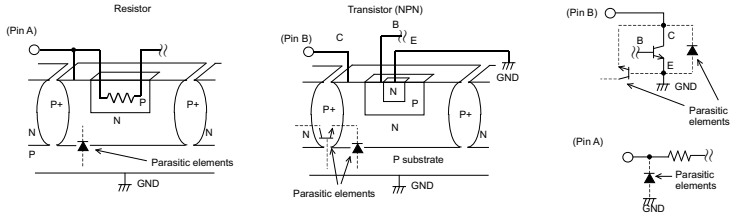


Fig. Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

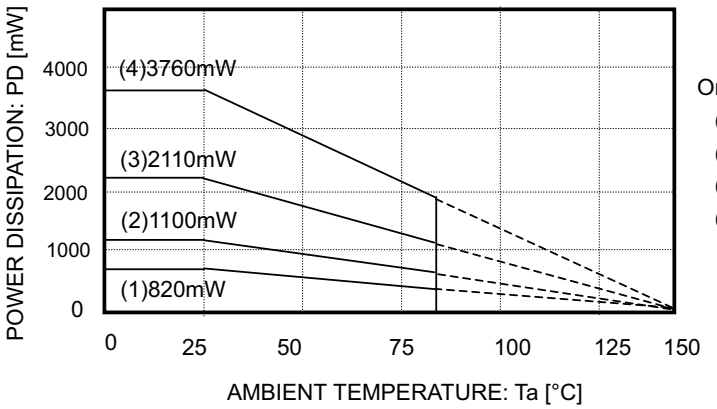
10) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards

At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

● Power Dissipation



On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

Excellence in Electronics

ROHM CO., LTD.
21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto
615-8585, Japan
TEL: (075)311-2121 FAX: (075)315-0172
URL http: // www. rohm. com

Published by
Application Engineering Group

Contact us for further information about the products.

Atlanta U.S.A. / ROHM ELECTRONICS ATLANTA SALES OFFICE (DIVISION OF ROHM ELE. U.S.A .,LLC)
TEL: +1(770)754-5972 FAX: +1(770)754-0691
Dallas U.S.A. / ROHM ELECTRONICS DALLAS SALES OFFICE (DIVISION OF ROHM ELE. U.S.A .,LLC)
TEL: +1(972)312-8818 FAX: +1(972)312-0330
San Diego U.S.A. / ROHM ELECTRONICS SAN DIEGO SALES OFFICE (DIVISION OF ROHM ELE. U.S.A .,LLC)
TEL: +1(858)625-3630 FAX: +1(858)625-3670
Germany / ROHM ELECTRONICS GMBH (GERMANY)
TEL: +49(2154)9210 FAX: +49(2154)921400
United Kingdom / ROHM ELECTRONICS GMBH (UK)
TEL: +44(0)1908-306700 FAX: +44(0)1908-235788
France / ROHM ELECTRONICS GMBH (FRANCE)
TEL: +33(0)1 56 97 30 60 FAX: +33(0)1 56 97 30 80
Hong Kong China / ROHM ELECTRONICS (H.K.) CO., LTD.
TEL: +852(2)7406262 FAX: +852(2)375-8971
Shanghai China / ROHM ELECTRONICS (SHANGHAI) CO., LTD.
TEL: +86(21)6279-2727 FAX: +86(21)6247-2066
Dalian China / ROHM ELECTRONICS TRADING (DALIAN) CO., LTD.
TEL:+86(411)8230-8549 FAX:+86(411)8230-8537
Beijing China / BEIJING REPRESENTATIVE OFFICE
TEL: +86(10)8525-2483 FAX: +86(10)8525-2489
Taiwan / ROHM ELECTRONICS TAIWAN CO., LTD.
TEL: +886(2)2500-6956 FAX: +886(2)2503-2869
Korea / ROHM ELECTRONICS KOREA CORPORATION
TEL: +82(2)8182-700 FAX: +82(2)8182-715
Singapore / ROHM ELECTRONICS ASIA PTE. LTD. (RES / REI)
TEL: +65-6332-2322 FAX: +65-6332-5662
Malaysia / ROHM ELECTRONICS (MALAYSIA) SDN. BHD.
TEL: +60(3)7958-8355 FAX: +60(3)7958-8377
Philippines / ROHM ELECTRONICS (PHILIPPINES) SALES CORPORATION
TEL: +63(2)807-6872 FAX: +63(2)809-1422
Thailand / ROHM ELECTRONICS (THAILAND) CO., LTD.
TEL: +66(2)254-4890 FAX: +66(2)256-6334