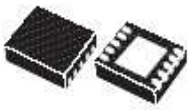
STEF05

Electronic fuse for 5V line

Features

- Continuous Current Typ: 3.6A
- NChannel On Resistance Typ:40mΩ
- Enable/Fault Functions
- Output Clamp Voltage Typ:6.65V
- Under Voltage Lockout
- Short Circuit Limit
- Overload Current Limit
- Controlled Output Voltage Ramp
- Thermal Latch Typ: 165℃
- Uses Tiny Capacitors
- Operative Junction Temp. -40℃ to 125℃
- Available in DFN 3x3 10L.



DFN 3x3 - 10L

Description

The STEF05 is an integrated electronic fuse optimized for monitoring the output current and the input voltage. Connected in series to the 5V rail, it is able to protect the electronic circuitry on its output from over current and over voltage. The STEF05 has a controlled delay and turn-on time. When an over load condition occurs the device limits the output current to a predefined safe value. If the anomalous overload condition persists it goes to the open state, disconnecting the load from the power supply. If a continuous short circuit is present on the board, when the power is re-applied, the E-fuse initially limits the output current to a safe value and then again goes to the open state.

The device is equipped with a thermal protection circuit. The intervention of the thermal protection is signalled to the board monitoring circuits through an appropriate signal on the Fault pin.

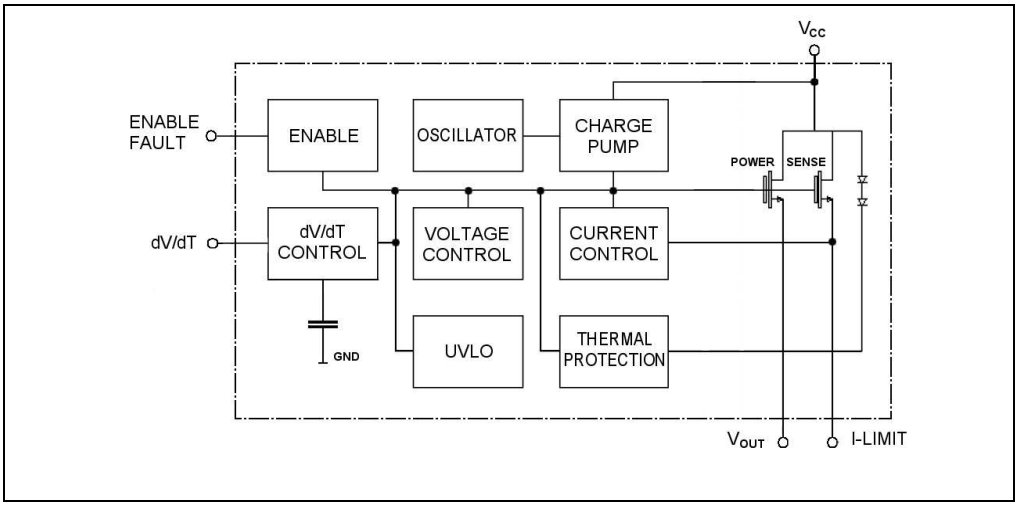
Unlike the mechanical fuses, that must be physically replaced after a single event, the E-fuse does not degrade in its performances after short circuit/thermal protection interventions and it is resetted either by re-cycling the supply voltage or using the appropriate Enable pin.

The companion chip for the 12V power rails is also available under the STEF12 code.

Applications

- Hard disk drives
- Solid State Drives (SSD)
- Hard Disk and SSD arrays
- Set top boxes
- DVDs and Blu-Ray disc drivers

Device block diagram



1 Pin Configuration

Figure 1. Pin Configuration (Top View)

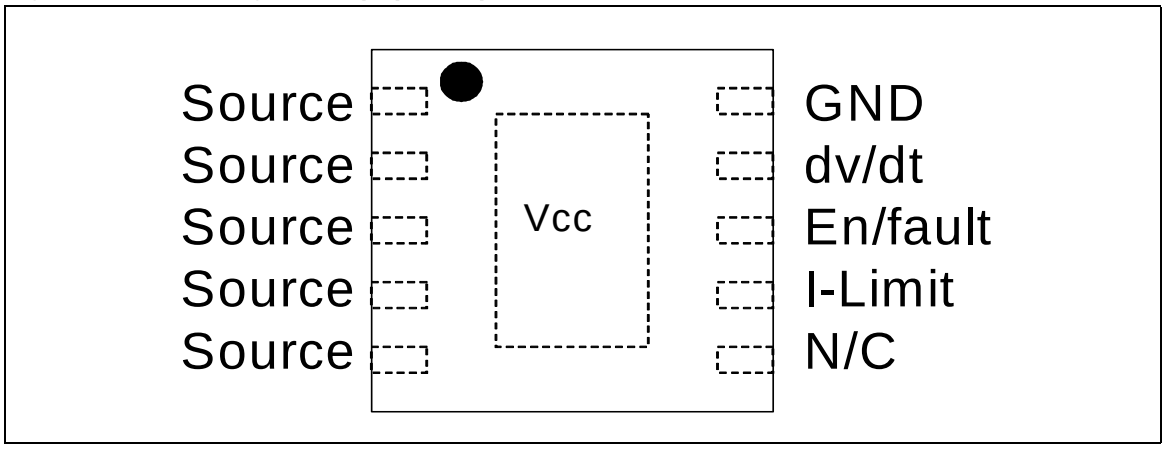


Table 1. Pin Description

PIN N°	SYMBOL	NOTE
1 to 5	Vout/Source	Connected to the Source of the internal power MOSFET and to the output terminal of the fuse
6	NC	Not connected
7	I-Limit	A resistor between this pin and the Source pin sets the overload and short circuit current limit levels.
8	En/Fault	The enable/fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to Ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
10	GND	Ground Pin
11	Vcc	Exposed pad. Positive input voltage must be connected to Vcc.

Table 2. Order Codes

Type	Tape & Reel	Package
STEF05	STEF05PUR	DFN 3x3 10L.

2 Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive Power Supply Voltage (steady state)	-0.3 to 10	V
	Positive Power Supply Voltage (max 100ms)	-0.3 to 15	
Vout/source	(max 100ms)	-0.3 to Vcc+0.3	V
I-Limit	(max 100ms)	-0.3 to 15	V
En/Fault		-0.3 to 7	V
dv/dt		-0.3 to 7	V
T_J	Max Junction Temperature(1)	-40 to 125	℃
T_{STG}	Storage Temperature Range	-65 to 150	℃
T_{LEAD}	Lead Temperature (Soldering) 10 sec	260	℃

1. The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional Operation under these conditions is not implied.

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction-Ambient	52.7	℃/W
R_{thJC}	Thermal Resistance Junction-Case	17.4	℃/W

3 Electrical Characteristics

Table 5. Electrical Characteristics for STEF05

V_{CC} =5V, V_{EN}=3.3V, C_I=10µF, C_O =47µF, T_J =25℃ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Under/Over Voltage Protection						
V_{Clamp}	Output Clamping Voltage	V_{CC}=10V	5.95	6.65	7.35	V
V_{UVLO}	Under voltage Lockout	Turn On, voltage going up	3.2	3.6	4	V
V_{Hyst}	UVLO Hysteresis			0.40		V
Power MOSFET						
t_{dly}	Delay Time	Enabling of chip to I_D=100mA with a 1A resistive load		500		µs
R_{DSon}	ON Resistance	Note1	20	40	60	mΩ
		Note2, -40℃<T_J<125℃			70	
V_{OFF}	Off State output Voltage	Vcc=10V, V_{GS}=0, R_L=infinite		35	100	mV
I_D	Continuous Current	0.5in^2 pad, Note2, T_A=25℃		3.6		A
		minimum copper,T_A=80℃		1.7		
Current Limit						
I_{Short}	Short Circuit Current Limit	R_{Limit}=22Ohm	1.9	2.9	3.9	A
I_{Lim}	Overload Current Limit	R_{Limit}=22Ohm		2.9		A
dv/dt Circuit						
dv/dt	Output Voltage Ramp Time	Enable to Vout=4.7V, No $C_{dv/dt}$	0.7	1.2	2.5	ms
$V_{dv/dt}$	dv/dt voltage end ramp	Vout=4.7V		1.8		V
$I_{dv/dt}$	dv/dt source pin current			170		nA
Enable/Fault						
V_{IL}	Low Level Input Voltage	Output Disabled	0.35	0.58	0.81	V
$V_{I(INT)}$	Intermediate Level Input Voltage	Thermal Fault, Output Disabled	0.82	1.4	1.95	V
V_{IH}	high Level Input Voltage	Output Enabled	1.96	2.64	3.3	V
$V_{I(MAX)}$	High State Maximum Voltage		3.4	4.3	5.2	V
I_{IL}	Low Level Input Current (Sink)	V_{Enable}=0V		-10	-30	µA
I_I	High Level Leakage Current for External Switch	V_{Enable}=3.3V			1	µA
	Maximum Fan-out for Fault Signal	Total numbers of chips that can be connected to this pin for simultaneous shutdown			3	Units
Total Device						
I_{Bias}	Bias Current	Device operational		0.5	2	mA
		Thermal Shutdown		1		
V_{min}	Minimum Operating Voltage				3.1	V
Thermal Latch						
TSD	Shutdown Temperature	Note2		165		℃

Note: 1 Pulse test: Pulse width=300µs, Duty cycle=2%

2 Guaranteed by design, but not tested in production

4 Typical Application

Figure 2. Application circuit

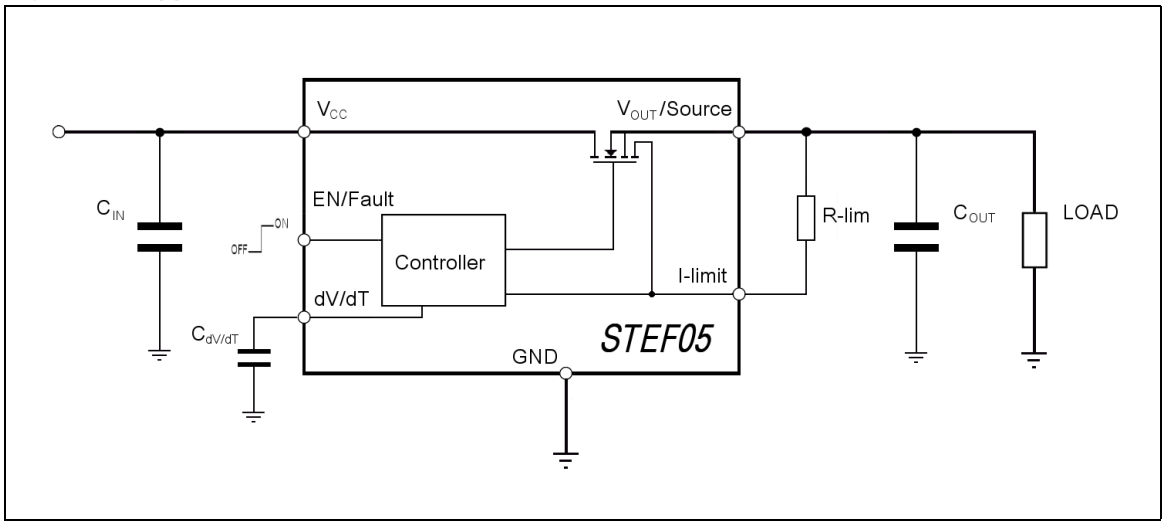
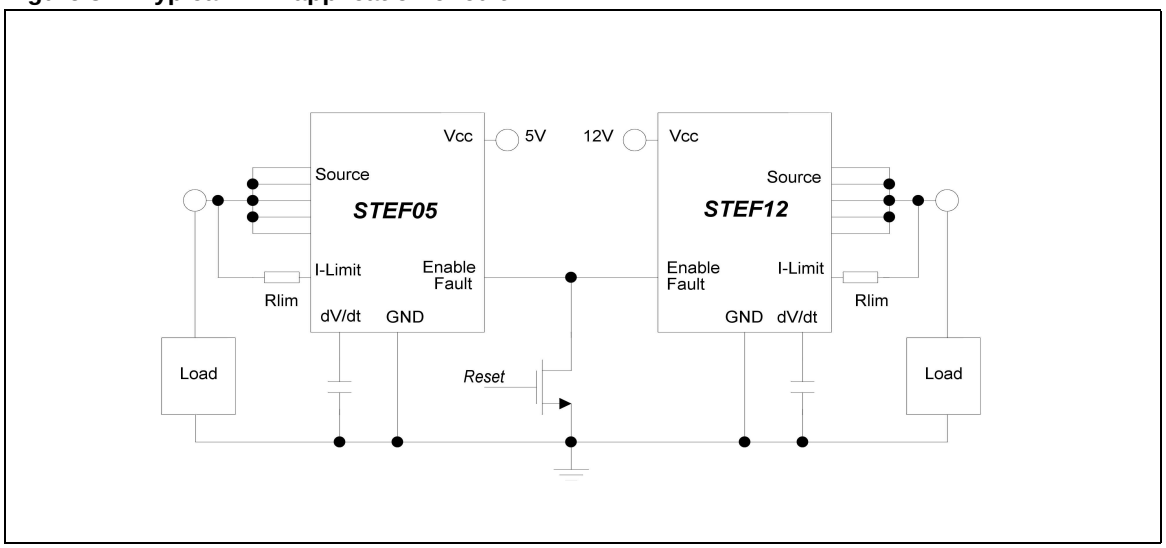


Figure 3. Typical HDD application circuit



4.1 Operating modes

4.1.1 Turn-on.

When the input voltage is applied, the Enable/Fault pin goes up to the high state, enabling the internal control circuitry.

After an initial delay time of typically 500µs, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 1ms (refer to *Figures 4, 14*).

4.1.2 Normal operating condition.

The STEF05 E-fuse behaves like a mechanical fuse, buffering the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the N-channel MOSFET RDSOn.

4.1.3 Output voltage clamp.

This internal protection circuit clamps the output voltage to a maximum safe value, typically 6.65V, if the input voltage exceeds this threshold.

4.1.4 Current Limiting.

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value selected externally by means of the limiting resistor R_{Limit} (*Figure 2*).

4.1.5 Thermal Shutdown.

If the device temperature exceeds the thermal latch threshold, typically 165°C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The EN/Fault pin of the device will be automatically set at an intermediate voltage, in order to signal the overtemperature event. In this condition the E-fuse can be resetted either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

4.2 R limit calculation

As shown in *Figure 2*, the device uses an internal N-channel Sense Fet with a fixed ratio, to monitor the output current and limit it at the level set by the user.

The R_{Limit} value for achieving the requested current limitation can be extimated by using the following theoretical formula, together with the *"**Current limit vs R_{Limit}**"* graph in *Figure 10*.

$$R_{Limit} = \frac{65}{I_{Short}}$$

4.3 $C_{dv/dt}$ calculation

Connecting a capacitor between the $C_{dv/dt}$ pin and Gnd will allow the modification of the output voltage ramp up time.

Given the desired time interval Δt during which the output voltage goes from zero to his maximum value, the capacitance to be added on $C_{dv/dt}$ pin can be calculated using the following theoretical formula:

$$C_{dvdt} = 50 \times 10^{-9} \Delta t - 30 \times 10^{-12}$$

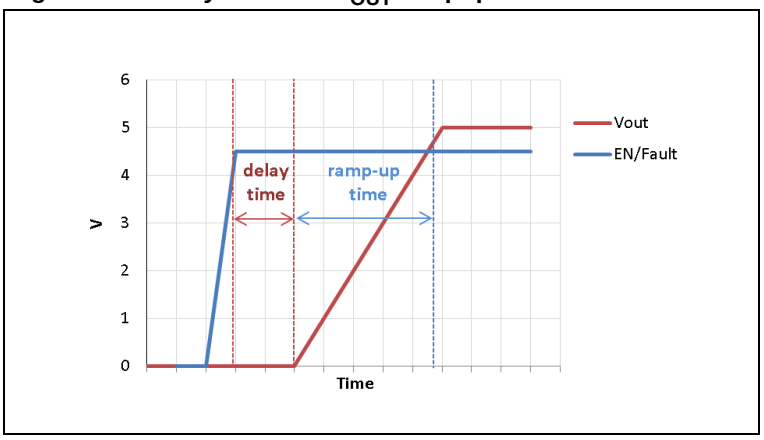
Where $C_{dv/dt}$ is expressed in Farad and the time in seconds.

The addition of an external $C_{dv/dt}$ influences also the initial delay time, defined as the time between the Enable signal going high and the start of the V_{OUT} slope *(Figure 4)*.

The contribution of the external capacitor to this time interval can be extimated by using the following theoretical formula:

$$\text{delay time} = 500 \times 10^{-6} + 13.6 \times 10^{6} \times C_{dvdt}$$

Figure 4. Delay time and V_{OUT} rampup time



4.4 Enable-fault pin

The Enable/Fault pin has the dual function of controlling the output of the device and, at the same time , of providing information about the device status to the application.

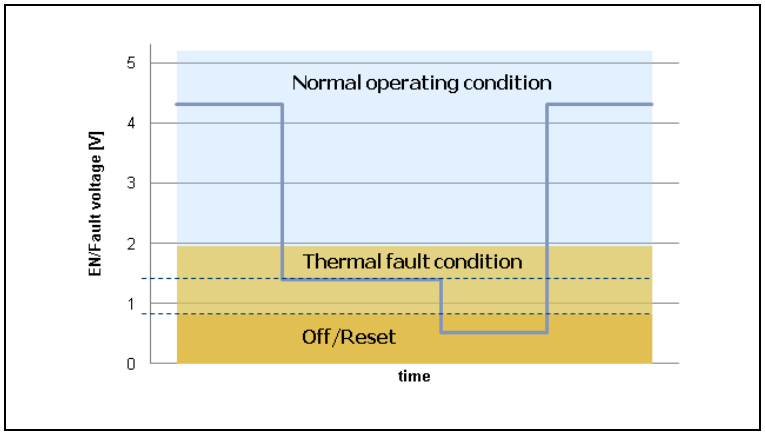
When it is used as a standard Enable pin, it should be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it will turn the output of the E-Fuse off.

If this pin is left floating, since it has an internal pull-up circuitry, the output of the E-Fuse will be kept ON, in normal operating condition.

In case of thermal fault the pin is pulled to an intermediate state *(Figure 5)*. This signal can be provided to a monitor circuit, informing that a thermal shutdown has occurred, or it can be directly connected to the Enable/Fault pins of other STEFxx devices on the same application, in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be resetted either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

Figure 5. Enable/Fault pin status



5 Typical Performance Characteristics

(The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25℃)

Figure 6. Clamping voltage vs temperature

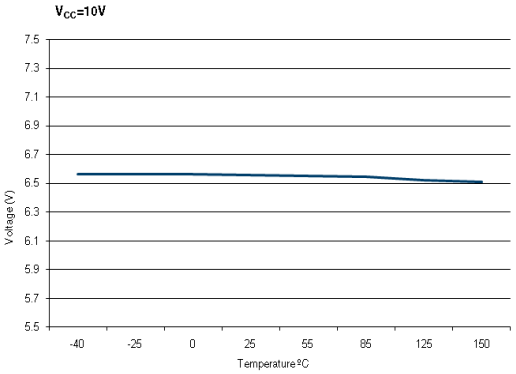


Figure 7. UVLO voltage vs temperature

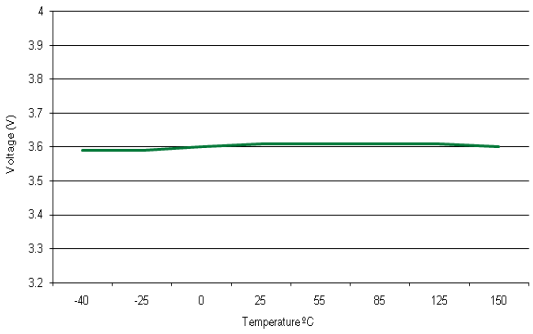


Figure 8. UVLO hysteresis vs temperature

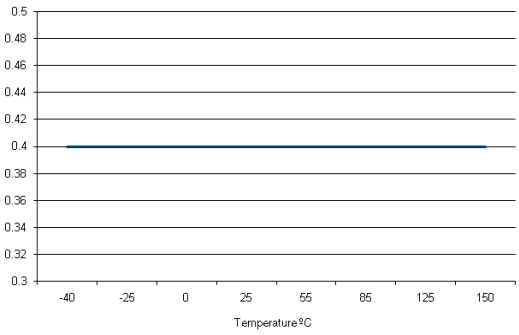


Figure 9. Off-state voltage vs temperature

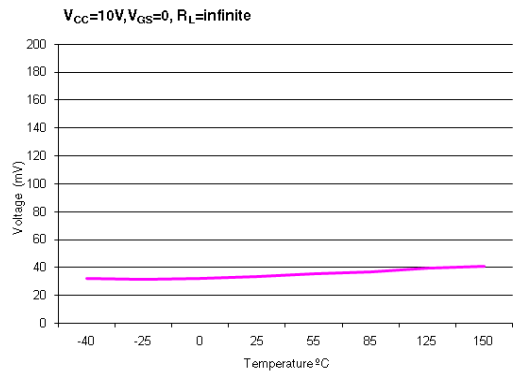


Figure 10. Bias current (device operational)

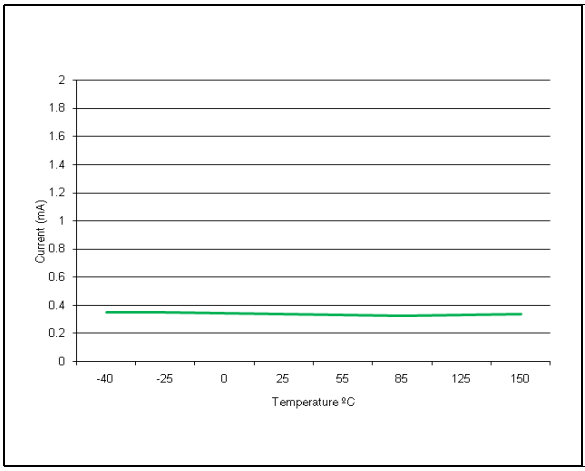


Figure 11. ON resistance vs temperature

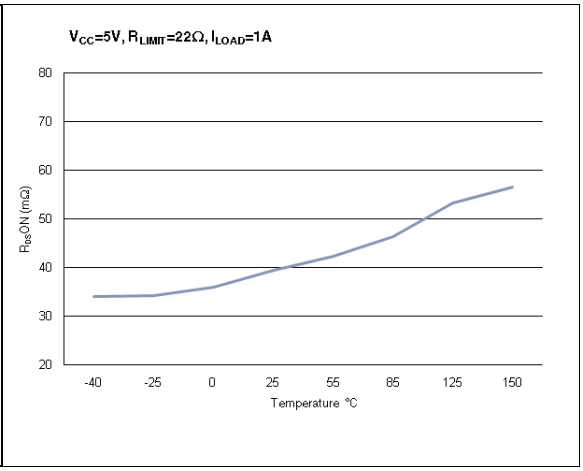


Figure 12. Current limit vs R_{Limit}

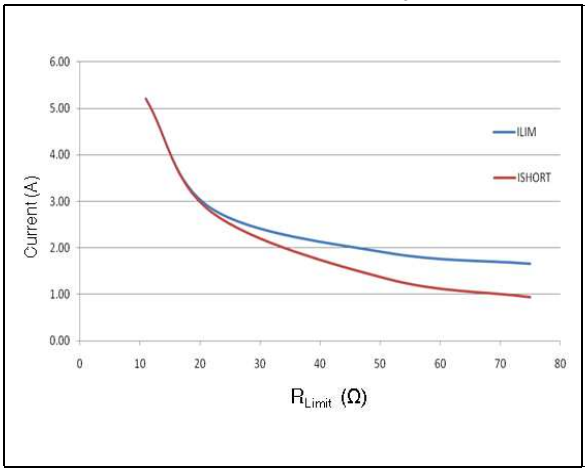


Figure 13. Thermal latch delay vs power

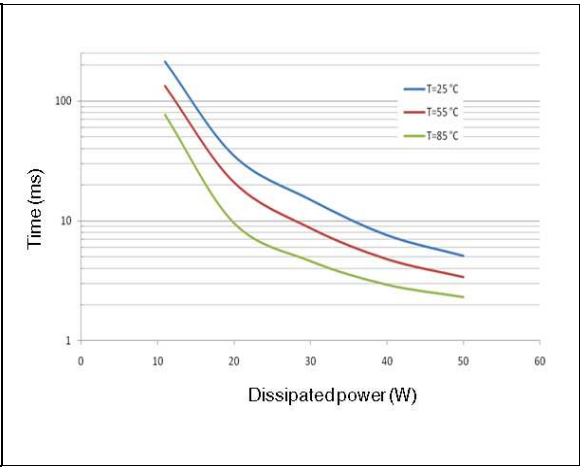


Figure 14. V_{OUT} ramp-up vs Enable

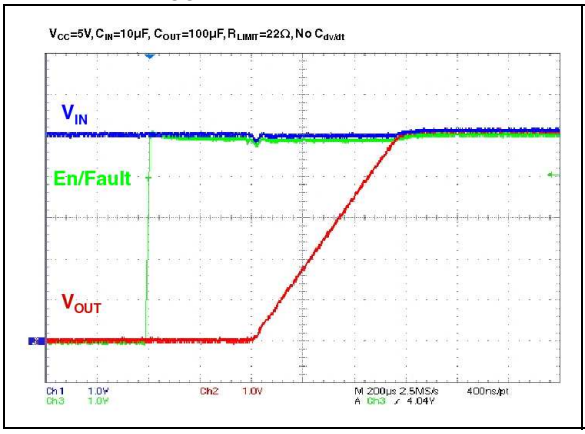


Figure 15. V_{OUT} clamping

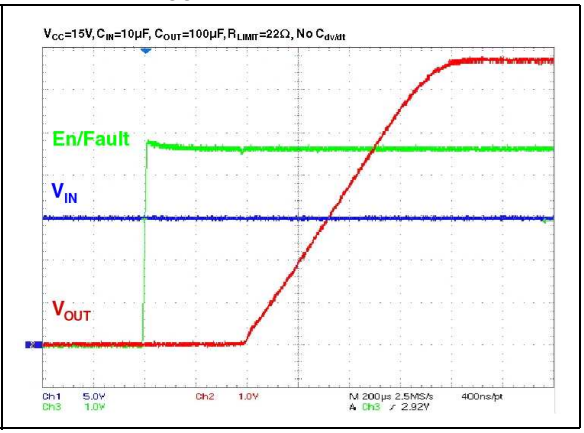


Figure 16. Line transient

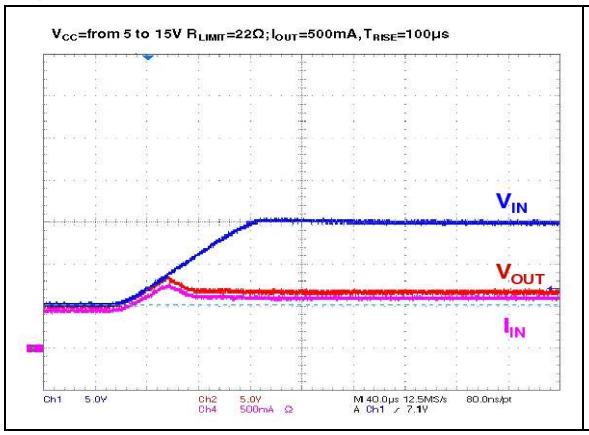


Figure 17. Startup into output short circuit

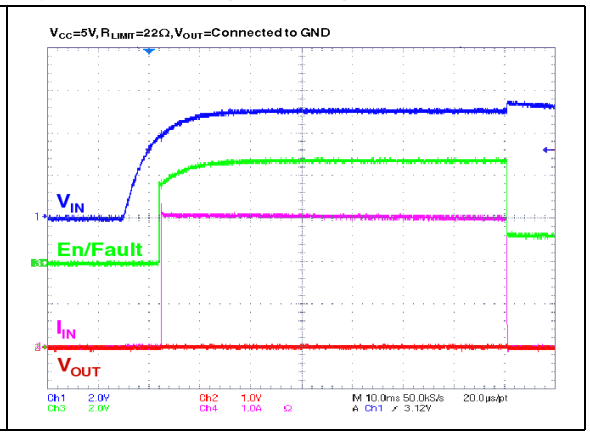


Figure 18. Thermal latch from 2A load to short circuit

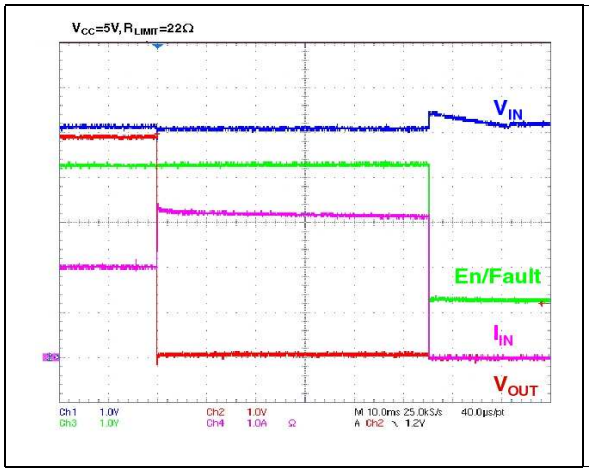
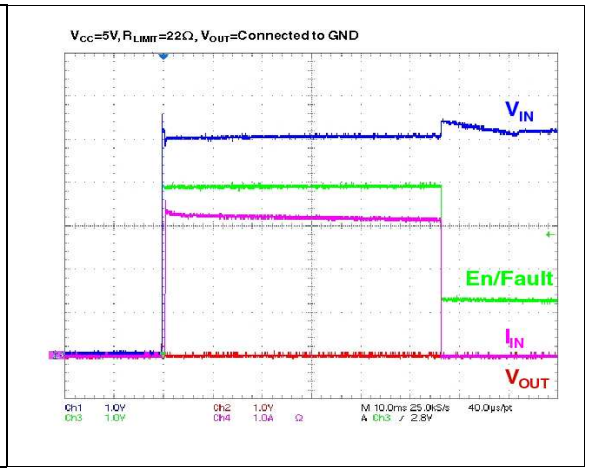
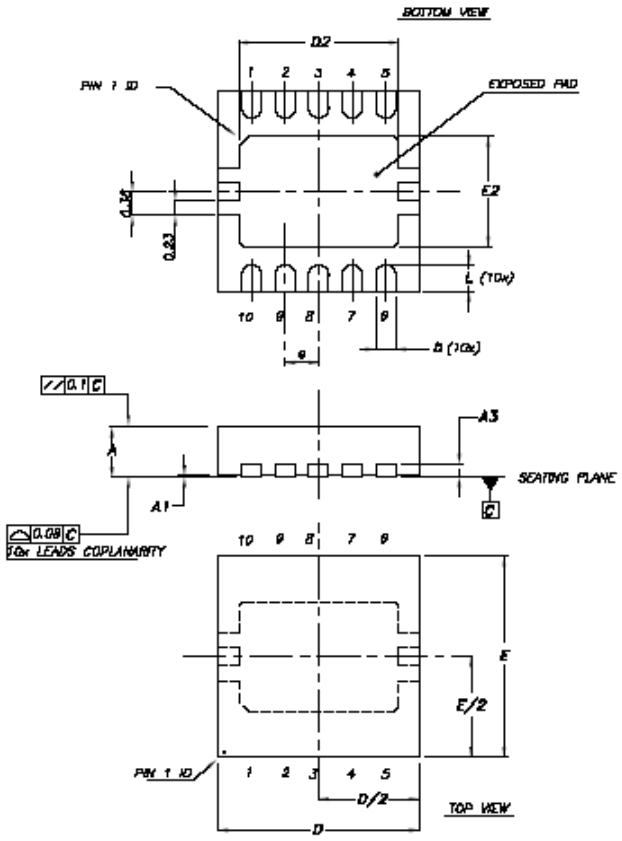


Figure 19. Startup into output short circuit (fast rise)



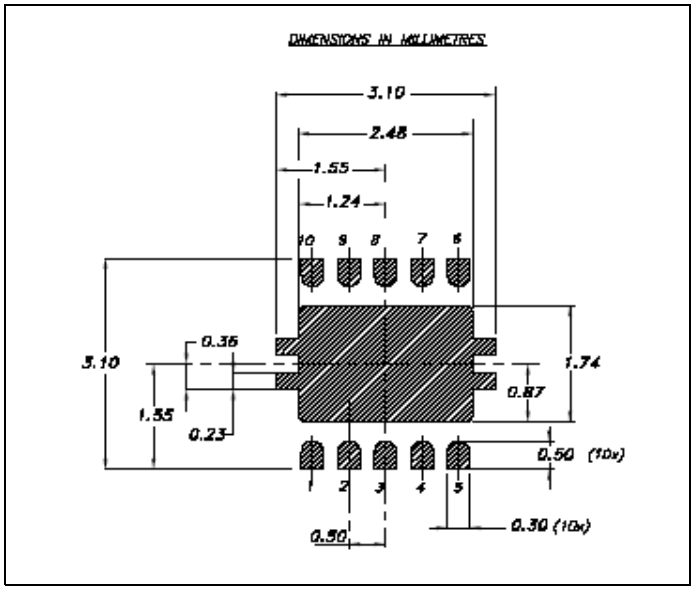
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.



Dim.	mm.			Inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3	3.10	0.114	0.118	0.122
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50			0.020	
L	0.30	0.40	0.50	0.012	0.016	0.020

7 Footprint Recommended Data



8 Revision History

Date	Revision	Description of Change
13 May 11	07	General review.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com