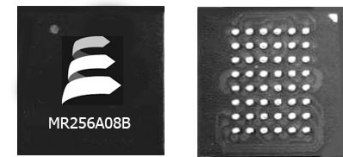


### Features

- Fast 35 ns Read/Write Cycle
- SRAM Compatible Timing Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to eliminate battery assembly, reliability, and liability issues
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, and Automotive Temperatures
- RoHS-Compliant SRAM-compatible TSOPII Package
- RoHS-Compliant SRAM-compatible BGA Package Shrinks Board Area By Three Times



48-BGA



### Introduction

The MR256A08B is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 8 bits. The MR256A08B offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR256A08B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The MR256A08B is available in small footprint 400-mil, 44-lead plastic small-outline TSOP type-II package or 8 mm x 8 mm, 48-pin ball grid array (BGA) package with 0.75 mm ball centers. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The MR256A08B provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), and automotive temperature (-40 to +125 °C) range options.

# Device Pin Assignment

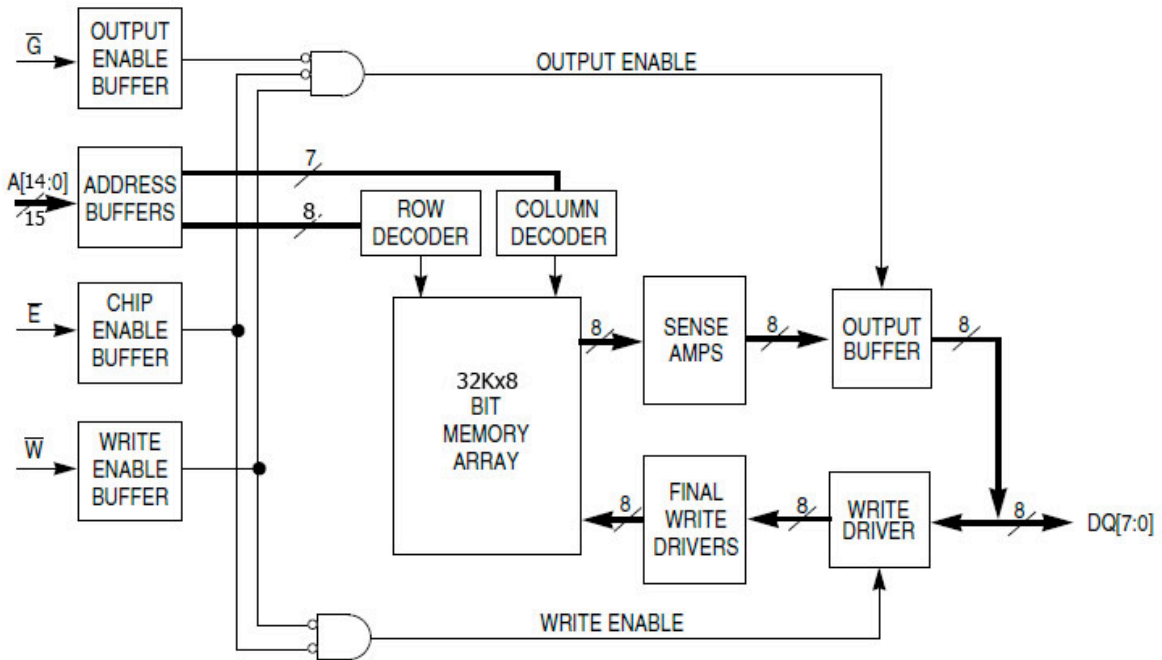
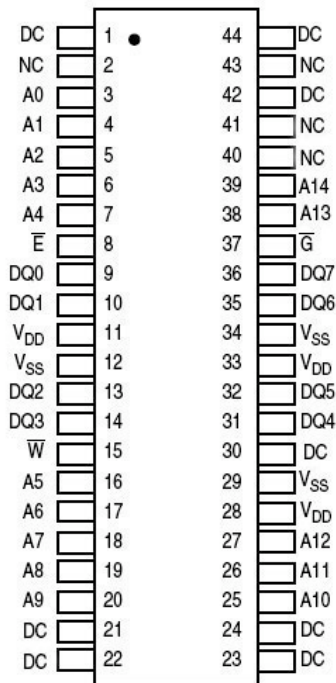


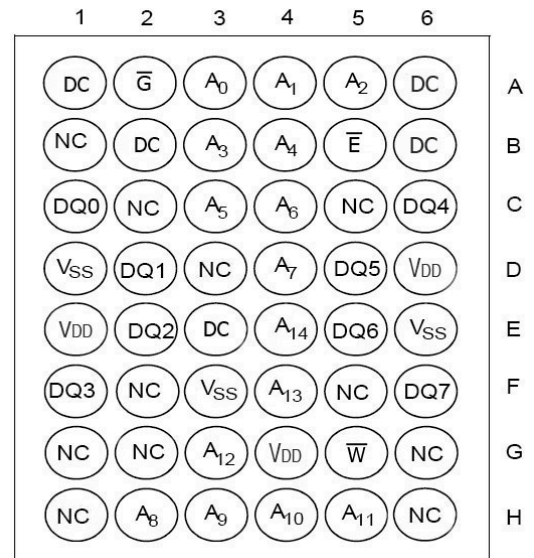
Figure 1. Block Diagram



44-Pin TSOP Type II

**Table 1. Pin Functions**

Signal Name	Function
A	Address input
$\bar{E}$	Chip enable
$\bar{W}$	Write enable
$\bar{G}$	Output enable
DQ	Data I/O
$V_{DD}$	Power supply
$V_{SS}$	Ground
DC	Do not connect this pin
NC	No connect - connection is optional



48-Pin BGA

**Table 2. Operating Modes**

$\overline{E}^1$	$\overline{G}^1$	$\overline{W}^1$	Mode	$V_{DD}$ Current	DQ[7:0] <sup>2</sup>
H	X	X	Not selected	$I_{SB1}, I_{SB2}$	Hi-Z
L	H	H	Output disabled	$I_{DDR}$	Hi-Z
L	L	H	Byte read	$I_{DDR}$	$D_{Out}$
L	X	L	Byte write	$I_{DDW}$	$D_{In}$

NOTES:

<sup>1</sup> H = high, L = low, X = don't care

<sup>2</sup> Hi-Z = high impedance

## Electrical Specifications

### Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

**Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Value	Unit
Supply voltage <sup>2</sup>	$V_{DD}$	-0.5 to 4.0	V
Voltage on any pin <sup>2</sup>	$V_{In}$	-0.5 to $V_{DD} + 0.5$	V
Output current per pin	$I_{Out}$	$\pm 20$	mA
Package power dissipation <sup>3</sup>	$P_D$	0.600	W
Temperature under bias MR256A08B (Commercial)	$T_{Bias}$	-10 to 85	°C
Storage temperature	$T_{stg}$	-55 to 150	°C
Lead temperature during solder (3 minute max)	$T_{Lead}$	260	°C
Maximum magnetic field during write MR256A08B (All Temperatures)	$H_{max\_write}$	2000	A/m
Maximum magnetic field during read or standby	$H_{max\_read}$	8000	A/m

NOTES:

<sup>1</sup> Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

<sup>2</sup> All voltages are referenced to  $V_{SS}$ .

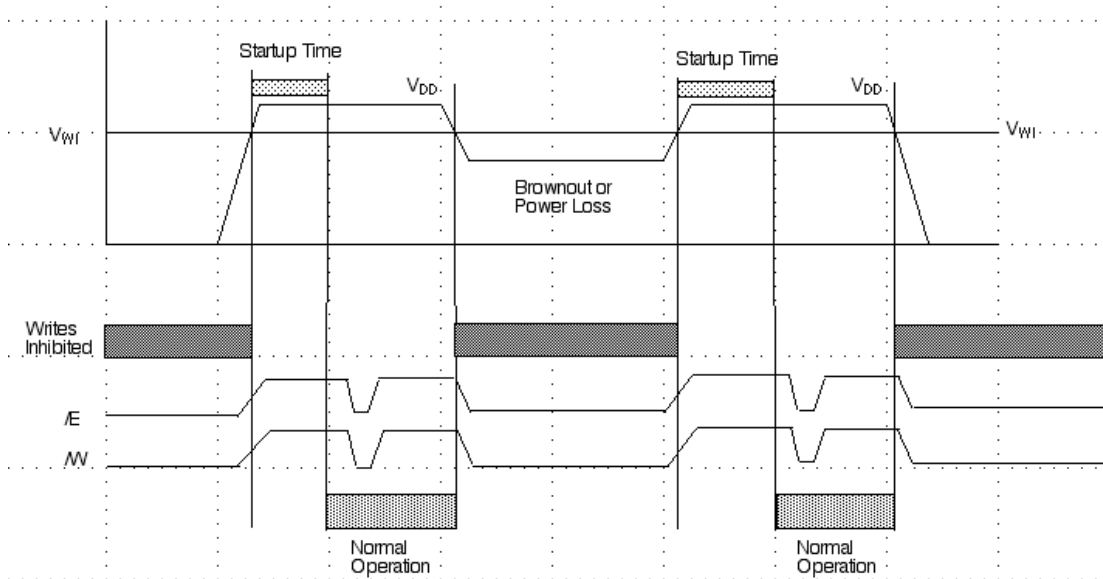
<sup>3</sup> Power dissipation capability depends on package characteristics and use environment.

**Table 4. Operating Conditions**  
Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	$V_{DD}$	3.0 <sup>1</sup>	3.3	3.6	V
Write inhibit voltage	$V_{WI}$	2.5	2.7	3.0 <sup>1</sup>	V
Input high voltage	$V_{IH}$	2.2	—	$V_{DD} + 0.3$ <sup>2</sup>	V
Input low voltage	$V_{IL}$	-0.5 <sup>3</sup>	—	0.8	V
Operating temperature MR256A08B (Commercial) MR256A08BC (Industrial) MR256A08BM (Automotive) <sup>4</sup>	$T_A$	0 -40 -40		70 85 125	°C

NOTES:

- 1 There is a 2 ms startup time once  $V_{DD}$  exceeds  $V_{DDmin}$ . See Power up and Powerdown Sequencing section below
- 2  $V_{IH} (max) = V_{DD} + 0.3 V_{dc}$ ;  $V_{IH} (max) = V_{DD} + 2.0 V_{ac}$  (pulse width  $\leq 10$  ns) for  $I \leq 20.0$  mA.
- 3  $V_{IL} (min) = -0.5 V_{dc}$ ;  $V_{IL} (min) = -2.0 V_{ac}$  (pulse width  $\leq 10$  ns) for  $I \leq 20.0$  mA.
- 4 Automotive temperature profile assumes 10% Duty Cycle at Maximum Temperature (2-years out of 20-year Life)



**Power Up and Power Down Sequencing**

MRAM is protected from write operations whenever  $V_{DD}$  is less than  $V_{WI}$ . As soon as  $V_{DD}$  exceeds  $V_{DDmin}$ , there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The  $/E$  and  $/W$  control signals should track  $V_{DD}$  on power up to  $V_{DD}-0.2V$  or  $V_{IH}$  (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives  $/E$  and  $/W$  should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where  $V_{DD}$  goes below  $V_{WI}$ , writes are protected and a startup time must be observed when power returns above  $V_{DDmin}$ .

### dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{lkg(I)}$	—	—	$\pm 1$	$\mu A$
Output leakage current	$I_{lkg(O)}$	—	—	$\pm 1$	$\mu A$
Output low voltage ( $I_{OL} = +4 \text{ mA}$ ) ( $I_{OL} = +100 \mu A$ )	$V_{OL}$	—	—	0.4 $V_{SS} + 0.2$	V
Output high voltage ( $I_{OH} = -4 \text{ mA}$ ) ( $I_{OH} = -100 \mu A$ )	$V_{OH}$	2.4 $V_{DD} - 0.2$	—	—	V

### Power Supply Characteristics

Parameter	Symbol	Typ	Max	Unit
ac active supply current — read modes <sup>1</sup> ( $I_{Out} = 0 \text{ mA}$ , $V_{DD} = \text{max}$ )	$I_{DDR}$	30	TBD	mA
ac active supply current — write modes <sup>1</sup> ( $V_{DD} = \text{max}$ ) MR256A08B (Commercial) MR256A08BC (Industrial) MR256A08BM (Automotive)	$I_{DDW}$	65 65 65	TBD	mA
ac standby current ( $V_{DD} = \text{max}$ , $\bar{E} = V_{IH}$ ) (no other restrictions on other inputs)	$I_{SB1}$	TBD	TBD	mA
CMOS standby current ( $\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$ ) ( $V_{DD} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	5	TBD	mA

**NOTES:**

<sup>1</sup> All active current measurements are measured with one address transition per cycle and at minimum cycle time.

## Timing Specifications

**Table 7. Capacitance<sup>1</sup>**

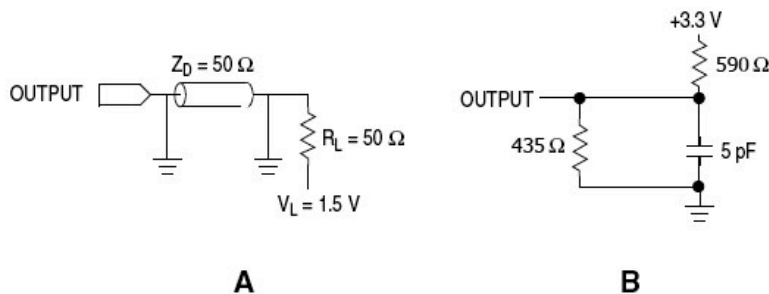
Parameter	Symbol	Typ	Max	Unit
Address input capacitance	$C_{In}$	—	6	pF
Control input capacitance	$C_{In}$	—	6	pF
Input/output capacitance	$C_{I/O}$	—	8	pF

NOTES:

<sup>1</sup>  $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , periodically sampled rather than 100% tested.

**Table 8. ac Measurement Conditions**

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B



**Figure 3. Output Load for ac Test**

# Timing Specifications

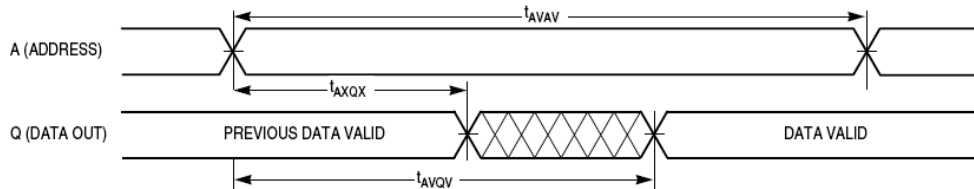
## Read Mode

Table 9. Read Cycle Timing<sup>1,2</sup>

Parameter	Symbol	Min	Max	Unit
Read cycle time	$t_{AVAV}$	35	—	ns
Address access time	$t_{AVQV}$	—	35	ns
Enable access time <sup>3</sup>	$t_{ELQV}$	—	35	ns
Output enable access time	$t_{GLQV}$	—	15	ns
Byte enable access time	$t_{BLQV}$	—	15	ns
Output hold from address change	$t_{AXQX}$	3	—	ns
Enable low to output active <sup>4,5</sup>	$t_{ELQX}$	3	—	ns
Output enable low to output active <sup>4,5</sup>	$t_{GLQX}$	0	—	ns
Byte enable low to output active <sup>4,5</sup>	$t_{BLQX}$	0	—	ns
Enable high to output Hi-Z <sup>4,5</sup>	$t_{EHQZ}$	0	15	ns
Output enable high to output Hi-Z <sup>4,5</sup>	$t_{GHQZ}$	0	10	ns
Byte high to output Hi-Z <sup>4,5</sup>	$t_{BHQZ}$	0	10	ns

NOTES:

- 1  $\bar{W}$  is high for read cycle.
- 2 Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
- 3 Addresses valid before or at the same time  $\bar{E}$  goes low.
- 4 This parameter is sampled and not 100% tested.
- 5 Transition is measured  $\pm 200$  mV from steady-state voltage.



NOTES:

Device is continuously selected ( $\bar{E} \leq V_{IL}$ ,  $\bar{G} \leq V_{IL}$ ).

Figure 5. Read Cycle 1

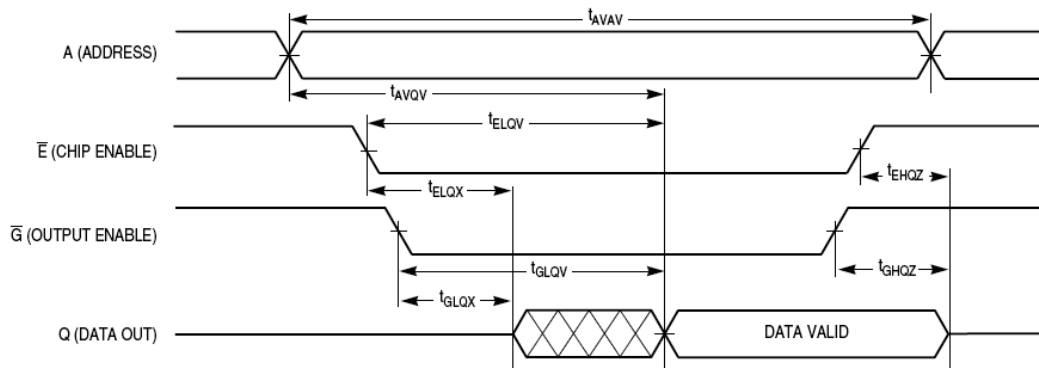


Figure 6. Read Cycle 2

# Timing Specifications

## Write Mode

Table 10. Write Cycle Timing 1 ( $\overline{W}$  Controlled)<sup>1, 2, 3, 4, 5</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>6</sup>	$t_{AVAV}$	35	—	ns
Address set-up time	$t_{AVWL}$	0	—	ns
Address valid to end of write ( $\overline{G}$ high)	$t_{AVWH}$	18	—	ns
Address valid to end of write ( $\overline{G}$ low)	$t_{AVWH}$	20	—	ns
Write pulse width ( $\overline{G}$ high)	$t_{WLWH}$ $t_{WLEH}$	15	—	ns
Write pulse width ( $\overline{G}$ low)	$t_{WLWH}$ $t_{WLEH}$	15	—	ns
Data valid to end of write	$t_{DVWH}$	10	—	ns
Data hold time	$t_{WHDX}$	0	—	ns
Write low to data Hi-Z <sup>7, 8, 9</sup>	$t_{WLQZ}$	0	12	ns
Write high to output active <sup>7, 8, 9</sup>	$t_{WHQX}$	3	—	ns
Write recovery time	$t_{WHAX}$	12	—	ns

NOTES:

- 1 A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- 2 Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles
- 3 If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- 4 After  $\overline{W}$ ,  $\overline{E}$ , or  $\overline{UB}/\overline{LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- 5 The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- 6 All write cycle timings are referenced from the last valid address to the first transition address.
- 7 This parameter is sampled and not 100% tested.
- 8 Transition is measured  $\pm 200$  mV from steady-state voltage.
- 9 At any given voltage or temperature,  $t_{WLQZ}$  max <  $t_{WHQX}$  min.

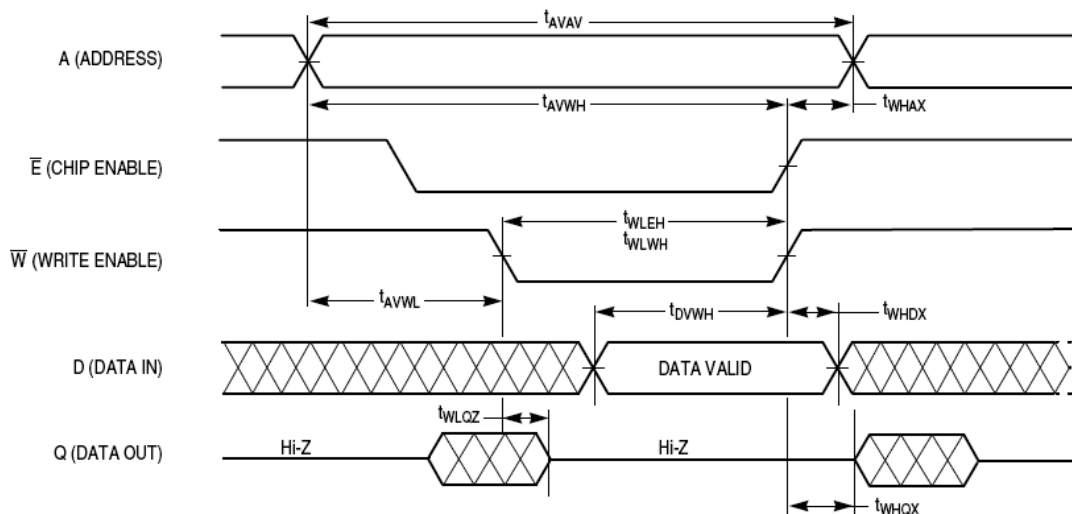


Figure 7. Write Cycle 1 ( $\overline{W}$  Controlled)



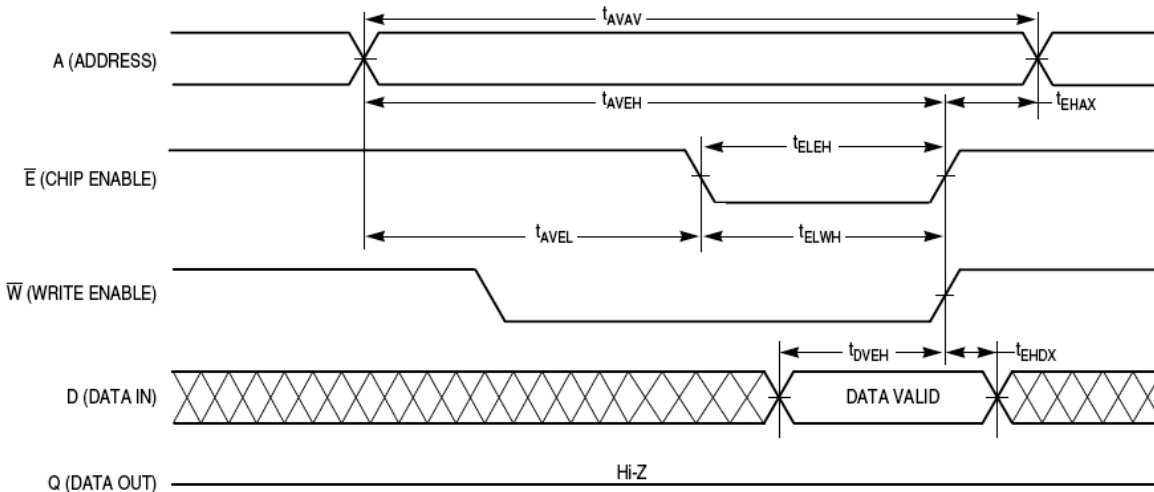
# Timing Specifications

**Table 11. Write Cycle Timing 2 ( $\overline{E}$  Controlled)<sup>1, 2, 3, 4, 5</sup>**

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>6</sup>	$t_{AVAV}$	35	—	ns
Address set-up time	$t_{AVEL}$	0	—	ns
Address valid to end of write ( $\overline{G}$ high)	$t_{AVEH}$	18	—	ns
Address valid to end of write ( $\overline{G}$ low)	$t_{AVEH}$	20	—	ns
Enable to end of write ( $\overline{G}$ high)	$t_{ELEH}$ $t_{ELWH}$	15	—	ns
Enable to end of write ( $\overline{G}$ low) <sup>7, 8</sup>	$t_{ELEH}$ $t_{ELWH}$	15	—	ns
Data valid to end of write	$t_{DVEH}$	10	—	ns
Data hold time	$t_{EHDX}$	0	—	ns
Write recovery time	$t_{EHAX}$	12	—	ns

**NOTES:**

- 1 A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- 2 Power supplies must be properly grounded and decoupled, and bus contention must be minimized or eliminated during read and write cycles.
- 3 If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- 4 After  $\overline{W}$ ,  $\overline{E}$ , or  $\overline{UB/LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- 5 The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- 6 All write cycle timings are referenced from the last valid address to the first transition address.
- 7 If  $\overline{E}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- 8 If  $\overline{E}$  goes high at the same time or before  $\overline{W}$  goes high, the output will remain in a high-impedance state.

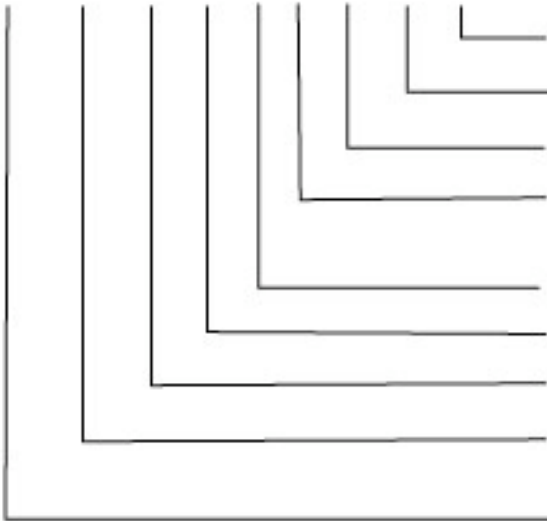


**Figure 8. Write Cycle 2 ( $\overline{E}$  Controlled)**

## Ordering Information

### Part Numbering System

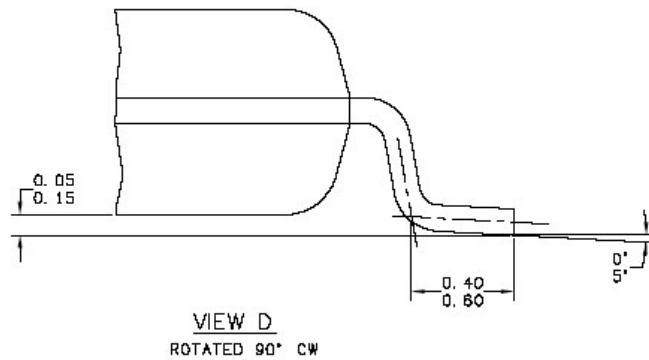
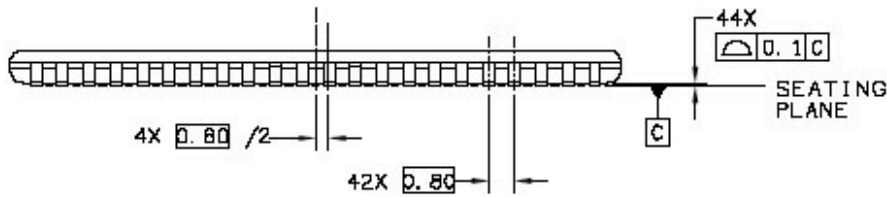
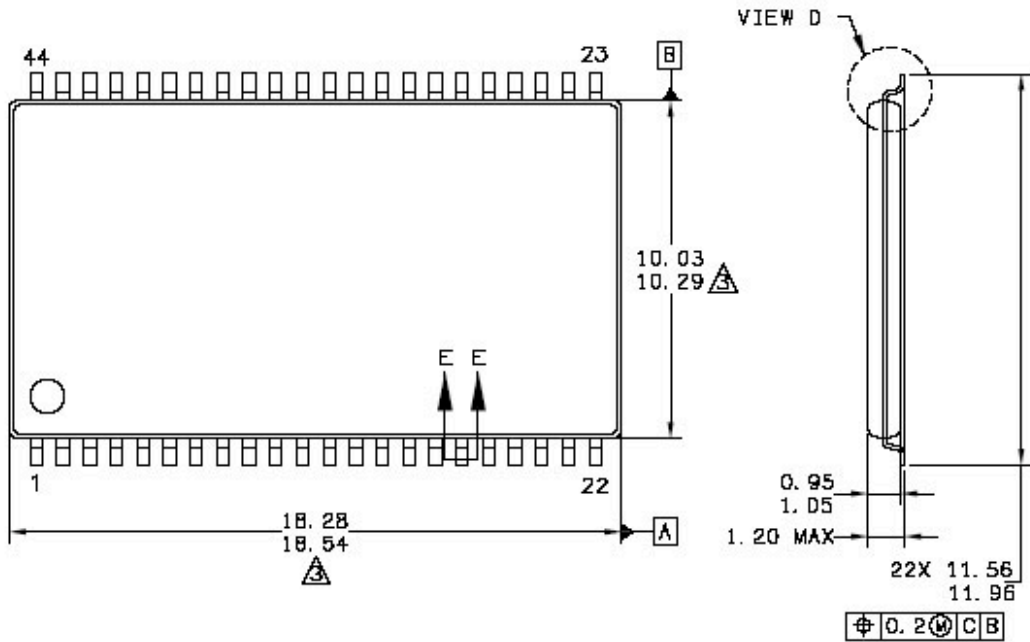
MR 256 A 08 B YS 35 R



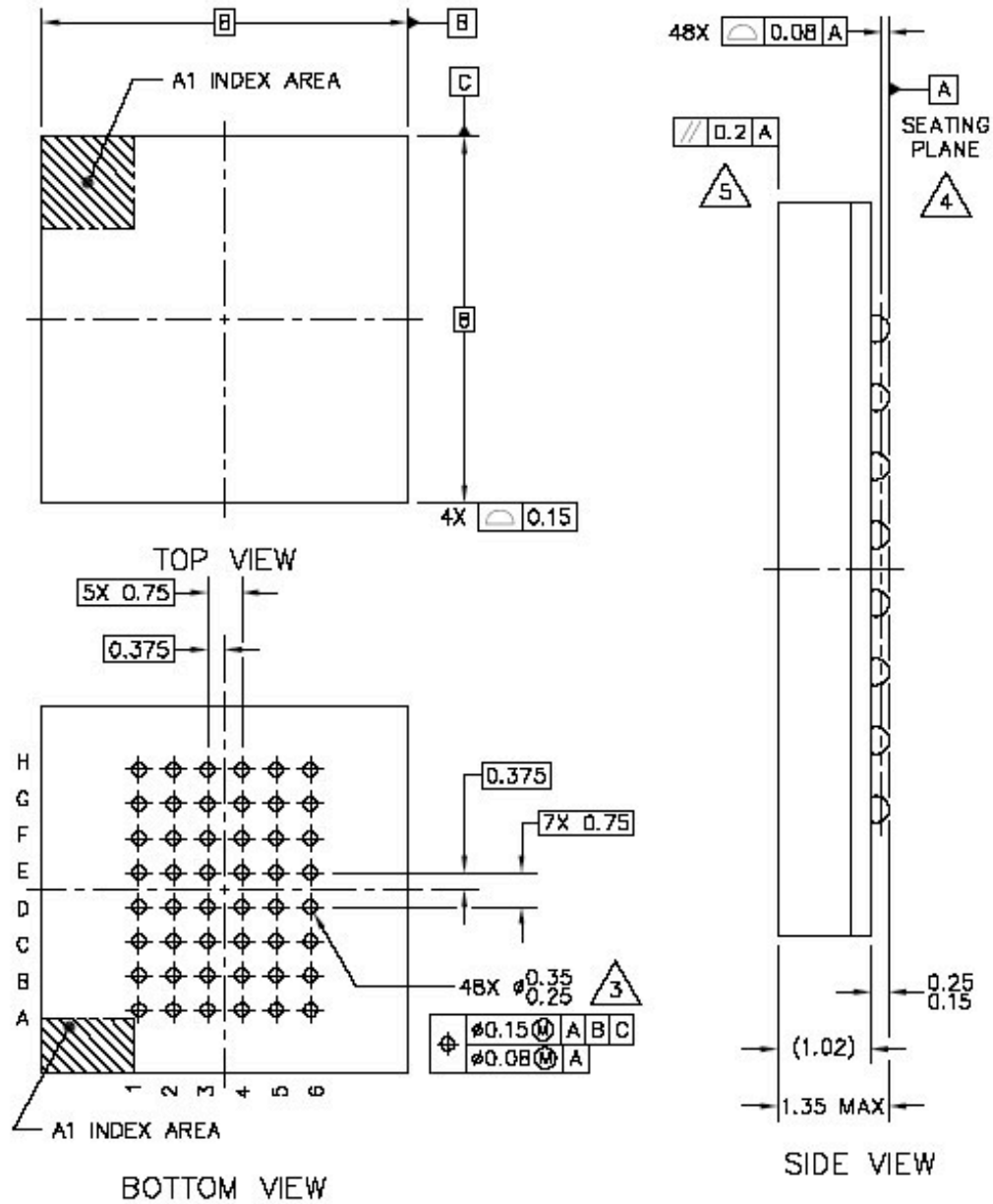
Carrier (Blank=Tray, R=Tape & Reel)  
 Speed (35 ns)  
 Package (YS=TSOPII, MA=BGA)  
 Temperature Range (Blank=0 to 70°C, C=-40 to +85°C, M=-40 to +125°C)  
 Revision (A=180 nm, B=130 nm)  
 Data Width (08=8-bit, 16=16-bit)  
 Type (A=Asynchronous, S=Synchronous)  
 Density (256=256Kb, 0=1Mb, 1=2Mb, 2=4Mb, 4=16Mb)  
 Magneto-resistive RAM (MR)

Part Number	Description	Temperature
MR256A08BYS35	3.3 V 32Kx8 MRAM 44-TSOP	Commercial
MR256A08BYS35R	3.3 V 32Kx8 MRAM 44-TSOP T&R	Commercial
MR256A08BMA35	3.3 V 32Kx8 MRAM 48-BGA	Commercial
MR256A08BCYS35	3.3 V 32Kx8 MRAM 44-TSOP	Industrial
MR256A08BCYS35R	3.3 V 32Kx8 MRAM 44-TSOP T&R	Industrial
MR256A08BCMA35	3.3 V 32Kx8 MRAM 48-BGA	Industrial
MR256A08BMYS35	3.3 V 32Kx8 MRAM 44-TSOP	Automotive
MR256A08BMYS35R	3.3 V 32Kx8 MRAM 44-TSOP T&R	Automotive
MR256A08BMMA35	3.3 V 32Kx8 MRAM 48-BGA	Automotive

# Mechanical Drawing (44-TSOP)



# Mechanical Drawing (48-BGA)



**NOTES:**

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

---

## Revision History

Revision	Date	Description of Change
0	Sep 12, 2008	Initial Advance Information Release
1	Mar 25, 2009	Add Industrial and Automotive Temperature Options

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document.

Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part.

Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.

©Everspin Technologies, Inc. 2009

### How to Reach Us:

EverSpin Technologies, Inc.  
1300 N. Alma School Road, CH-400  
Chandler, AZ 85224  
(480) 347-1111  
[www.Everspin.com](http://www.Everspin.com)