CY8CLEDAC02

AC-DC Controller for Dimmable LED Lighting

Features

- AC offline input range from 80 to 277 VAC
- Up to 25 W output power range
- Intelligent wall dimmer detection:
  - Leading edge (R, RL) dimmers
  - Trailing edge (RC, RLC) dimmers
  - No dimmer
- Wide dimming range from 2 to 100 percent
- Resonant control to achieve high efficiency (85 percent without dimmer)
- Meets harmonic requirement with high power factor (0.7 without dimmer)
- Primary-side sensing eliminates opto-isolators
- Tight LED current regulation (typically < ± 2.5 percent)
- Low startup current (typically 10 μA)
- Low startup time (typically 0.5 s with active startup)
- Multiple protection features:
  - Output overvoltage protection (OOVP)
  - Output short circuit protection (OSCP)
  - Overtemperature protection (OTP)
  - Current-sense resistor short protection (CSSP)
  - Peak current limit protection (PCLP)
  - Single-point fault protection
- Applications:
  - Dimmable offline LED driver
  - Dimmable LED replacement lamps
  - Dimmable LED luminaires

Description

The CY8CLEDAC02 is a high performance offline LED driver, designed to interface directly with most conventional phase cut based wall dimmers. The device uses proprietary digital control technology to provide automatic detection of dimmer type (leading or trailing edge). It automatically generates dimming signals for LED loads and has the ability to dim down to 2 percent. It modulates LED brightness using a linear dimming scheme and switches to a pulse width modulation (PWM) based dimming scheme for output current levels lower than 20 percent of the full load current. In PWM mode optimized dimming frequencies in the range of 900 Hz result in zero visible flicker.

At the heart of a CY8CLEDAC02 based system is the chopping circuit which provides the load necessary to enable correct wall dimmer operation. It also improves PF when there is no dimmer on the line.

The devices' proprietary primary side sensing enables tight LED current regulation and eliminates the need for secondary feedback circuitry. No opto-couplers are necessary to meet UL isolation requirements; enabling flyback conversion with automatic isolation.

The CY8CLEDAC02 operates in quasi-resonant mode to achieve high efficiency. This mode of operation helps minimize external component count and simplifies EMI design, lowering the total bill of material cost.

The device's cycle-by-cycle adaptive digital regulation uses critical discontinuous conduction mode (CDCM) when driving LED loads. The control algorithm for cycle-by-cycle regulation has internal compensation for guaranteed system phase and gain margins; requiring no external components for loop compensation.

The CY8CLEDAC02 has full featured circuit protection not normally available with other primary-side control solutions. The built-in protection includes output overvoltage protection, output short circuit protection, overtemperature protection, current-sense resistor short protection, and peak current limit protection. It also enables automatic LED brightness adjustment to compensate for temperature drift by simply connecting a NTC resistor to the V_T pin.

Logic Block Diagram

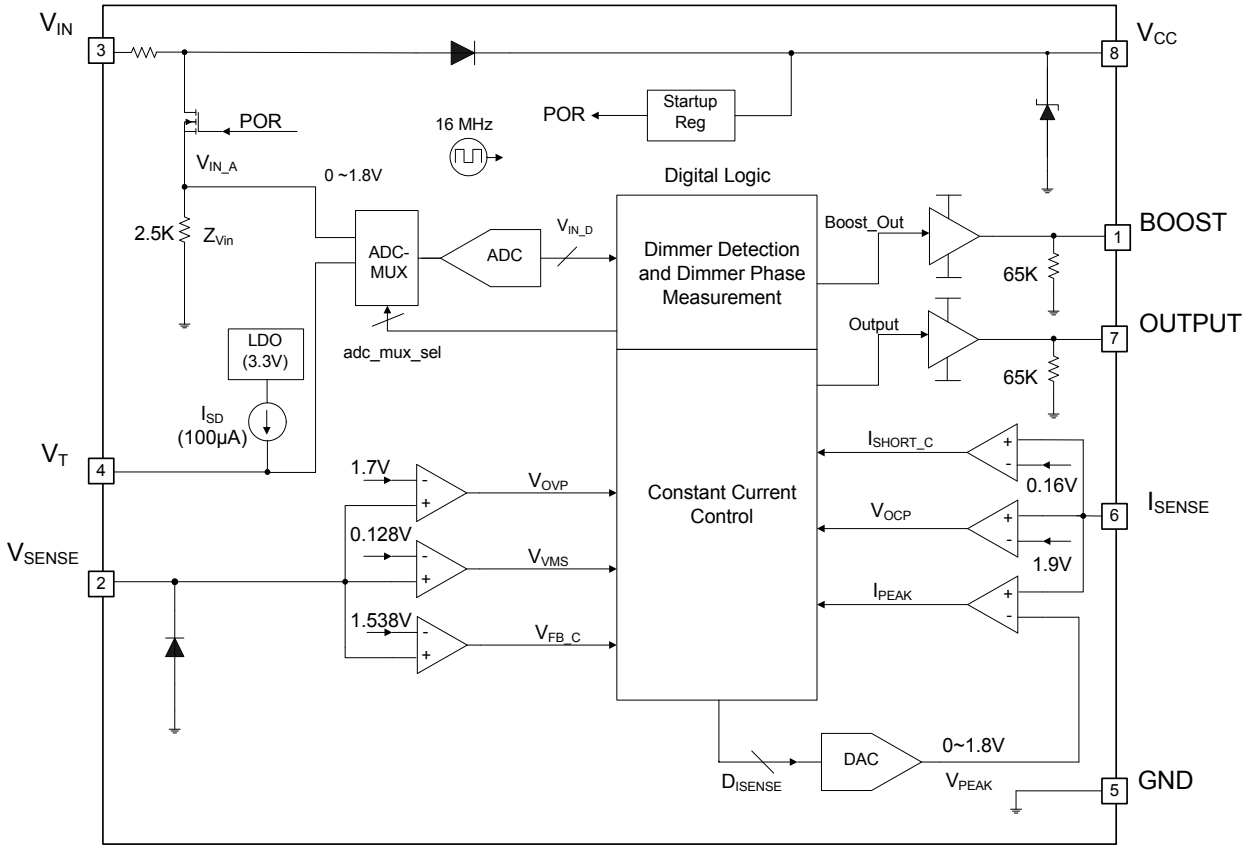

Figure 1. Simplified Application Diagram

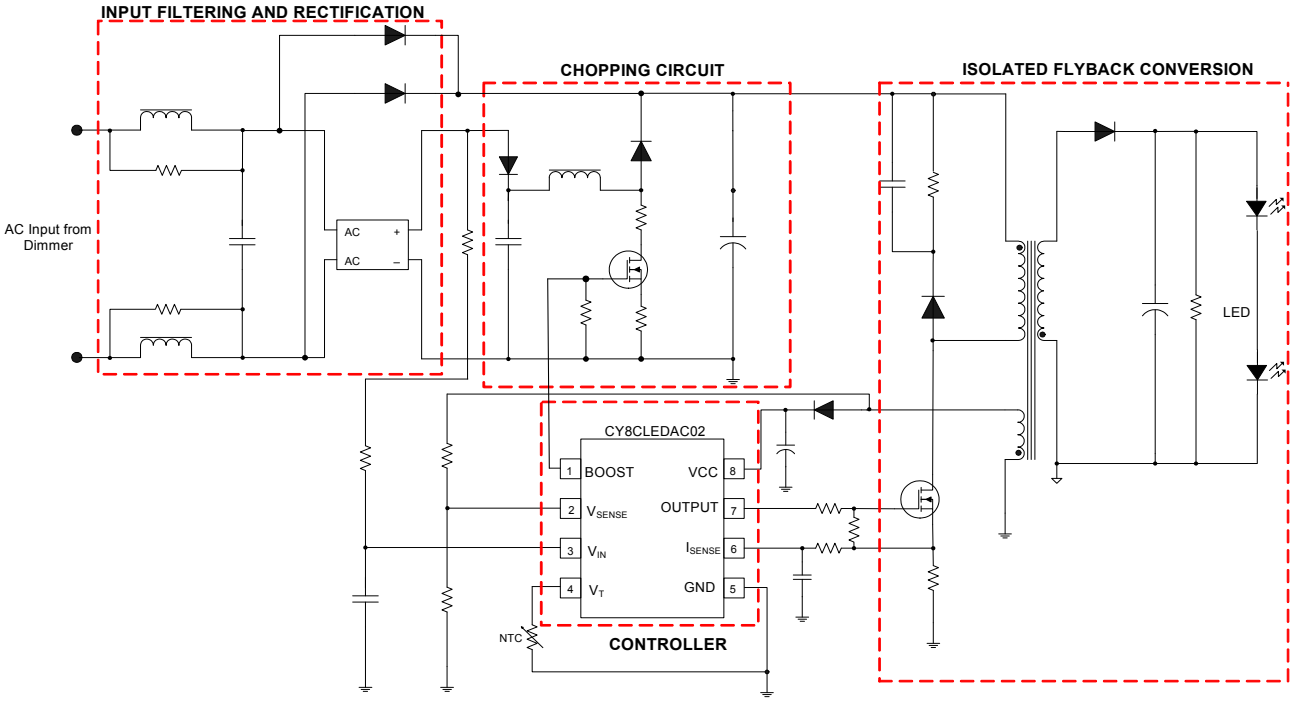

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Figure 2. Pin Diagram - 8-Pin SOIC CY8CLEDAC02

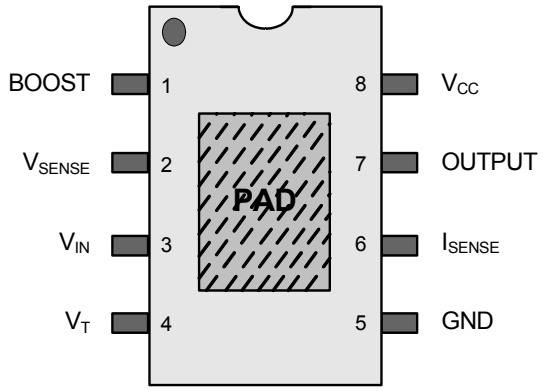


Table 1. Pin Description - 8-Pin SOIC CY8CLEDAC02

Pin No.	Name	Type	Pin Description
1	BOOST	Output	Gate driver for driving the MOSFET switch in the chopping circuit
2	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary regulation and zero voltage switching)
3	V_{IN}	Analog Input	Rectified AC line voltage sense, also used for device startup
4	V_T	Analog Input	Used for temperature compensation and overtemperature protection, also used as an external shut down pin
5	GND	Ground	Ground
6	I_{SENSE}	Analog Input	Primary current sense. Used for cycle-by-cycle peak-current control and limiting
7	OUTPUT	Output	Gate driver for main MOSFET switch
8	V_{CC}	Power Input	Power supply for control logic and voltage sense for power-on reset circuitry
–	PAD	Exposed Pad	Connect exposed pad electrically to GND

Functional Description

Overview

The digital logic block is the main control block. All the other blocks are either inputs or outputs for the digital logic block.

The digital logic block receives signals to determine the input voltage (V_{IN}), output voltage (V_{SENSE}), temperature (V_T), and output current (I_{SENSE}). It has three output controls; D_{ISENSE} (current control), Output (flyback MOSFET gate drive control), and Boost_Out (chopper MOSFET gate drive control).

The bias winding of the transformer provides voltage feedback to the controller for regulation and safety features. The external voltage sense resistors (not shown) determine the feedback signal to the V_{SENSE} pin of the controller. The V_{SENSE} pin connects to circuitry composed of three comparators: V_{OVP} (output overvoltage protection), V_{VMS} (voltage valley mode switch), and V_{FB_C} (voltage feedback from coil). When the V_{SENSE} voltage exceeds $V_{SENSE(MAX)}$ (1.7 V) the control block detects an overvoltage condition, it will enter a shutdown mode and wait for POR to re-initialize the system. V_{VMS} is monitored by the control block to determine when the power in the flyback MOSFET is at a minimum or in a 'valley'. When the V_{SENSE} voltage goes below the 0.128 V threshold the control block starts monitoring valleys and will start the next cycle at the 'valley' for maximum efficiency and minimum switching EMI. For normal operation, the V_{SENSE} voltage should be set below $V_{SENSE(NOM)}$ (1.538 V). When the V_{SENSE} voltage exceeds $V_{SENSE(NOM)}$ the controller senses an output overvoltage and tries to maintain a constant output voltage. This is an intermediate mode where the controller starts reacting to a problem with the output voltage. However, an OVP fault will only trigger if V_{SENSE} voltage exceeds $V_{SENSE(MAX)}$.

The I_{SENSE} pin connects to circuitry composed of three comparators: I_{PEAK}, V_{OCP}, and I_{SHORT_C}. These three blocks work together for soft start control and peak current detection, overcurrent protection, and sense resistor short protection respectively. The DAC V_{PEAK} controls soft start; minimizing stress associated with system startup. The I_{PEAK} comparator monitors the voltage at the I_{SENSE} pin. The voltage is generated by current flowing through a small external resistor (R_{ISENSE} - not shown). When the I_{SENSE} voltage reaches V_{REG-TH} (1.8 V), the I_{PEAK} comparator asserts a high to the control block. The control block will shut off the output and wait for V_{VMS} detection; then start the next cycle. The V_{OCP} comparator provides primary side overcurrent protection. When the voltage on I_{SENSE} reaches V_{PEAK} (1.9 V), the V_{OCP} signal gets asserted. When overcurrent is detected, the control block will enter a shutdown mode and reset the system. When the I_{SENSE} voltage reaches V_{RSNS} (0.16 V), a sense resistor short circuit fault is detected and the control block will enter a shutdown mode and reset all the digital logic.

The Output signal connects to the gate driver block for the OUTPUT pin that, in turn, connects to the flyback MOSFET gate pin (not shown). The OUTPUT pin is a digital control pin that switches between high level (approximately V_{CC}) and low level (approximately ground). The duration for high (t_{ON}) and low (t_{OFF}) of the Gate Driver is a function of the control block operating upon its inputs: V_{IN},t_{ON}, V_{FB}, V_{VMS}, V_T, I_{PEAK}, V_{OCP}, and V_{CC}.

The Boost_Out signal connects to the gate driver block for the BOOST pin that, in turn, connects to the chopper MOSFET gate pin (not shown). The BOOST pin is again a digital control pin that switches between high level (approximately V_{CC}) and low level (approximately ground). The BOOST pin timing is internally controlled and depends on the mode of operation for the IC (that is, no dimmer, trailing edge dimmer, or leading edge dimmer mode).

The V_T pin connects to a current source (I_{SD}), generated by an internal LDO, and an analog to digital converter. This pin can be used for OTP along with automatic LED brightness adjustment to compensate for temperature drift. This can be achieved by simply connecting the V_T pin to an external NTC component (not shown). The current source causes a voltage to develop at the V_T pin which is sampled once every AC half cycle by the ADC. If the voltage is between 0.5 to 2 V, the controller operates normally. For a voltage range 0.5 V to 0.3 V, the LED intensity is linearly dimmed. At 0.3 V the LEDs are dimmed to 10 percent. From 0.3 V to 0.1 V, the LED intensity stays at 10 percent and below 0.1 V (V_{SH-TH}), the controller will trigger a fault, enter shutdown mode, and reset all the digital logic.

Device Startup

Before startup, V_{IN} charges up the V_{CC} capacitor through the internal diode between V_{IN} and V_{CC} (see "Logic Block Diagram" on page 2). When the voltage at V_{CC} rises above the startup threshold V_{CCST}, the control logic is enabled.

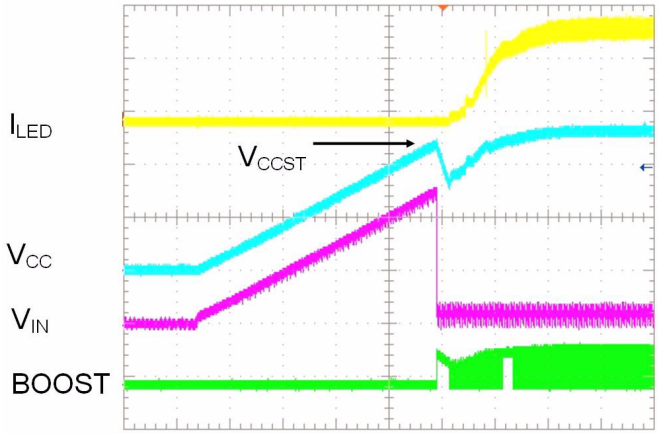
In the first four AC half cycles after startup, the BOOST pin is held high (see Figure 3 on page 6). During these half cycles the dimmer type is detected and the AC line period is measured. Following this, the controller enters an intermediate state and waits for the output voltage to ramp up. When the output voltage is higher than the forward voltage for the LED string, the controller enters constant current mode.

An adaptive soft start control algorithm is applied at startup, during which the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle-by-cycle by I_{PEAK} comparator.

If at any time the V_{CC} voltage drops below the V_{CCUVL} threshold, all the digital logic is reset. At this time the internal V_{IN} switch turns off allowing the V_{CC} capacitor to charge for a fresh startup.

If a faster startup is required, then an external active startup scheme can be used. Components R10, R11, Q3, and D5 enable active startup as illustrated in the "Typical Application Diagram" on page 14. Q3, a depletion type MOSFET, is initially on before startup. The V_{CC} capacitor C8 charges a lot quicker as the resistors R10 and R11 can be made much smaller than R3 and R4 lowering the overall charging resistance. When V_{CC} rises above V_{CCST}, the internal control logic gets enabled pulling the V_{IN} node low. The gate to source voltage across Q3 becomes negative, thus turning Q3 off. This technique substantially reduces startup time.

Figure 3. Device Startup Sequencing



Dimmer Detection

Intelligent Wall Dimmer detection includes automatically detecting presence or absence of a dimmer and, if present, detecting the dimmer type (leading or trailing edge).

Dimmer detection or discovery takes place during the first four AC half cycles after startup. During this phase the BOOST pin remains high, placing a purely resistive load across the dimmer. As wall dimmers are designed to work with resistive loads such as an incandescent lamp, loading the dimmer with a purely resistive load enables accurate dimmer detection.

The operation is broken into two stages. In the first stage, the controller simply determines whether a dimmer is present. If a dimmer is not detected, the dimmer type is set to 'no dimmer'. If a dimmer is detected, then in the next stage the dimmer type (leading or trailing edge) is determined.

The presence or absence of a dimmer is determined by monitoring how long the V_{IN} voltage stays below a zero-cross detect (ZCD) threshold. This threshold is determined by the controller using the peak of line and half line period measurements. An internal digital signal, V_{CROSS}, is generated which tracks the V_{IN} signal and determines the duration ($t_{PERIOD} - t_{CROSS}$) for which V_{IN} is below the ZCD threshold (see Figure 5 on page 7). This detection scheme is based on the fact that V_{IN} will remain below the ZCD threshold for a much longer duration in a single AC half cycle when a dimmer is present. In most cases V_{IN} is below the ZCD threshold for longer due to phase cut on the line. In cases when the dimmer does not exhibit any phase cut (at maximum setting) the duration is longer due to delays associated with dimmer operation.

If a dimmer is detected, then the V_{IN} pin voltage is filtered and differentiated to identify the largest positive and negative slopes in the AC half cycle. If the positive (rising) slope is greater than 1.5 times the negative (falling) slope, then a leading edge dimmer must be present. If not, a trailing edge dimmer must be present.

Figure 4. AC Line Waveforms with Leading Edge (left) and Trailing Edge (right) Dimmers

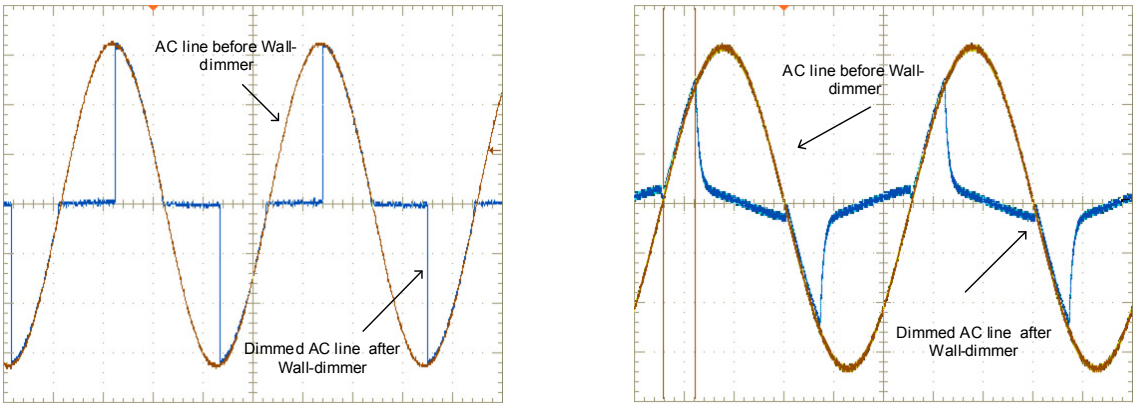
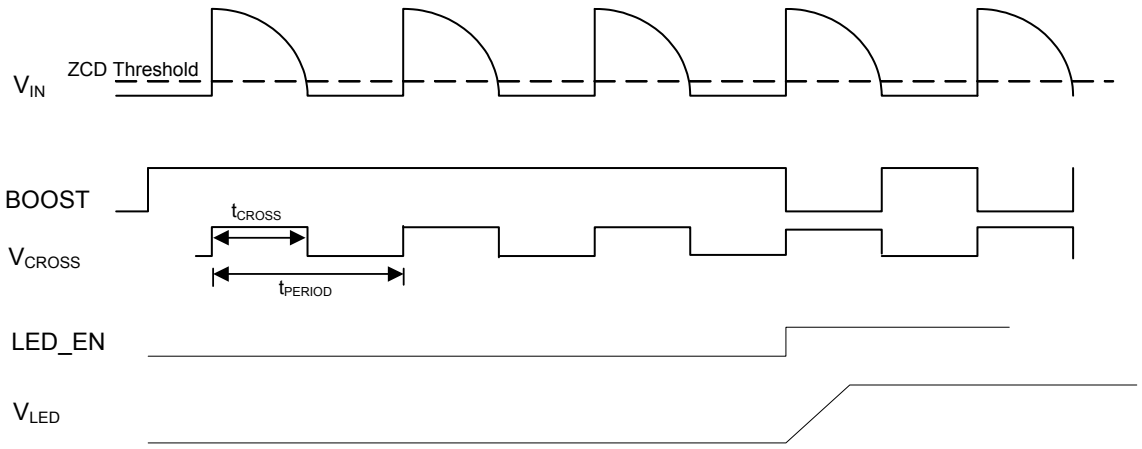


Figure 5. Dimmer Detection



Dimmer Tracking and Phase Measurement

Dimmer detection and tracking algorithms depend on accurate measurement of the V_{IN} period. The period is measured during the second cycle of the dimmer discovery process and is then latched for use. Using the measured V_{IN} period in subsequent calculations rather than a constant value enables automatic 50 or 60 Hz operation.

The phase measurement algorithm uses an internal counter that starts counting when the rising threshold on V_{IN} is exceeded and counts input voltage samples until the voltage is above the threshold. The counter is synchronized with the measured V_{IN} period and is restarted on every rising threshold (as shown in Figure 6).

The dimmer phase is calculated as:

Equation 1

$$D_{PHASE} = \frac{t_{CROSS}}{t_{PERIOD}}$$

The calculated D_{PHASE} is then used to generate a signal D_{RATIO}. When D_{PHASE} is less than 0.2, D_{RATIO} is set to 0.02 and when D_{PHASE} is greater than 0.8, D_{RATIO} is set to 1.0. For all other cases D_{RATIO} is set using the following equation:

Equation 2

$$D_{RATIO} = D_{PHASE} \times K1 - K2$$

where K1 and K2 are constants with values 1.63 and 0.3 respectively.

The output power to the LED load is modulated by D_{RATIO}. When D_{RATIO} is 1, 100 percent power is provided to the LED load, and when D_{RATIO} of 0.1, 10 percent power is provided to the LED load.

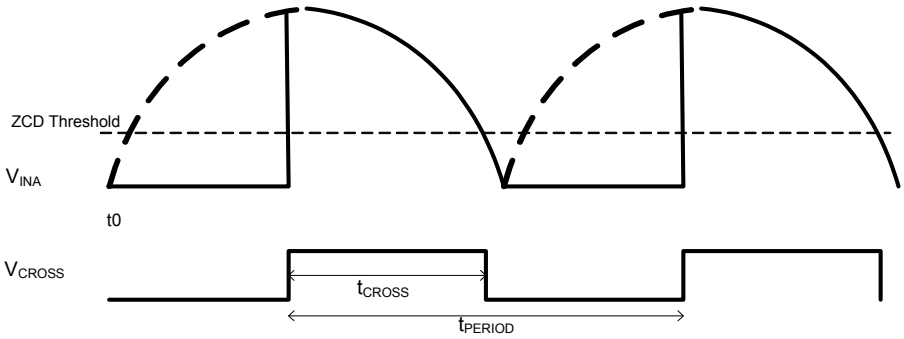
The voltage at the I_{SENSE} pin V_{ISENSE}, which modulates the output LED current can be set at a nominal value and modulated using the following equation:

Equation 3

$$V_{ISENSE} = V_{I\ SENSE\ (NOM)} \times D_{RATIO}$$

This equation provides a mapping from the measured dimmer phase to actual light output.

Figure 6. Dimmer Tracking and Phase Measurement



Chopping Operation

The chopping circuit provides four key functions:

- At startup, it provides a low impedance load on the wall dimmer enabling the type of dimmer (none, leading edge, or trailing edge) to be determined.
- Each cycle intelligently provides a low impedance load to:
  - Enable accurate determination of mains zero crossing points.
  - Meet triac trigger current and latch current requirements for triac based (leading edge) dimmers.
- Improves Power Factor
- Minimizes mains cycle peak current for triac based (leading edge) dimmers by boosting energy into the bulk capacitor.

The chopping circuit is shown in Figure 8. When Q2 is driven with short on pulses, the circuit operates as a boost converter. When Q2 turns on, the chopping inductor L3 stores energy. When Q2 turns off, this energy is released to capacitor C3 through diode D3. Source resistor R6 is used to limit the current in the chopper path to optimize the efficiency of the circuit. A dithering algorithm is used to control the period for Q2 to minimize EMI generated by the mainly discontinuous operation of the boost circuit. The voltage on Z_{VIN} is the scaled rectified mains voltage, a voltage only available internal to the device.

During the chopping period, the average current in L3 is in phase with and proportional to the input mains voltage inherently generating high power factor.

If the circuit determines it is connected to a dimmer, Q2 is held on while the mains voltage in is low. This provides a load on the dimmer enabling the internal circuitry of the dimmer to reset correctly for each half cycle. For leading edge dimmers, Q2 is held on for a significant time after the triac in the dimmer fires each half cycle. During this period L3 will saturate and R6 provides the current necessary for the triac latch current to be reached. For trailing edge dimmers, Q2 is held high after the trailing edge. This load forces the line to quickly fall to zero when the dimmer turns off, enabling accurate detection of the dimmer on time.

D8 and D9 ensure C3 is charged to peak voltage output from the dimmer. This maximizes the voltage on C3 each half cycle, minimizing the in rush current when the triac fires on the next half cycle.

The chopper operates in three different modes as follows:

- No dimmer: Chopper operates when the internal voltage at Z_{VIN} is above a pre-defined chopping threshold. The chopper remains off otherwise.(see Figure 7)
- Leading edge dimmer mode: The chopping period is defined as the percentage of the dimming period (T_{CROSS}). The chopper FET remains hard on during the zero crossing section on V_{IN}.(see Figure 9)
- Trailing edge dimmer mode: Chopping circuit is active across the entire dimming period (T_{CROSS}). The chopper FET remains hard on otherwise (see Figure 10).

Figure 7. Chopping Operation (No Dimmer Mode)

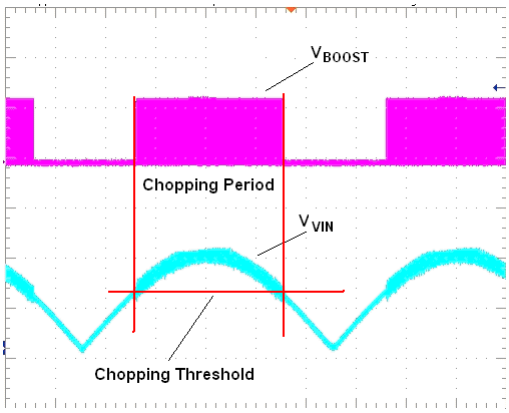


Figure 8. Chopper Circuit

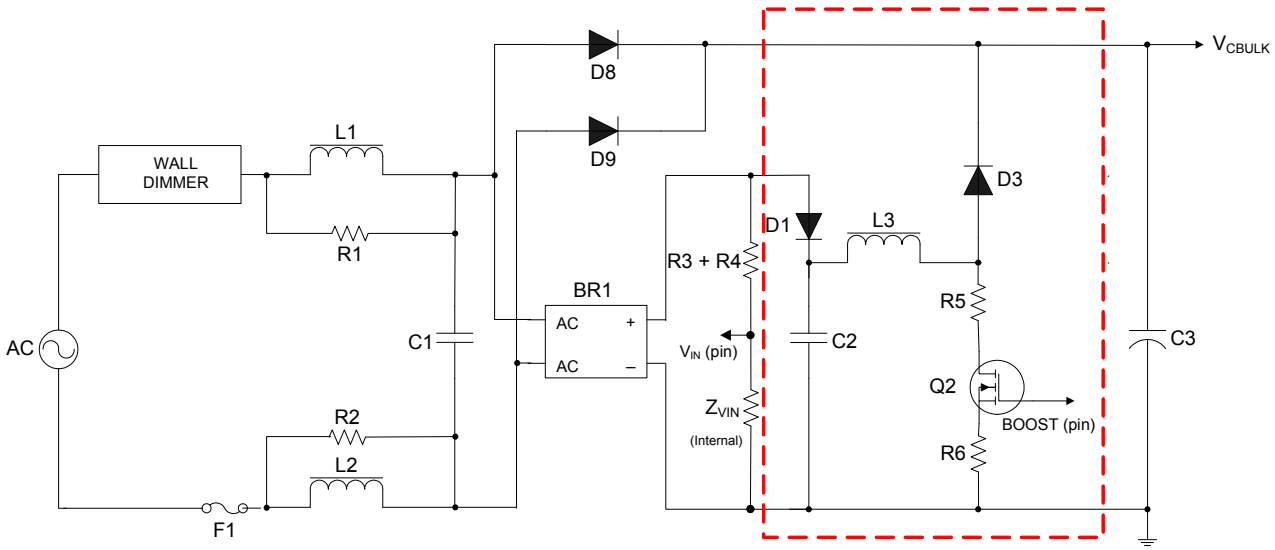


Figure 9. Chopper Operation (Leading Edge Dimmer Mode)

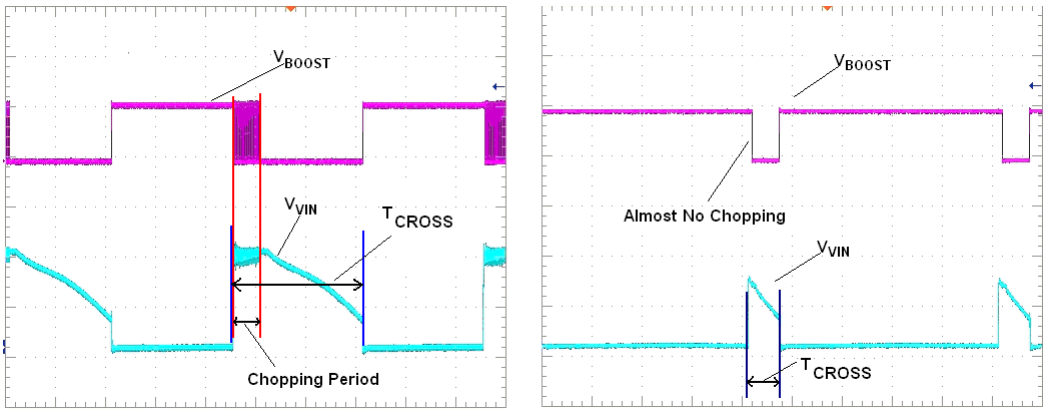
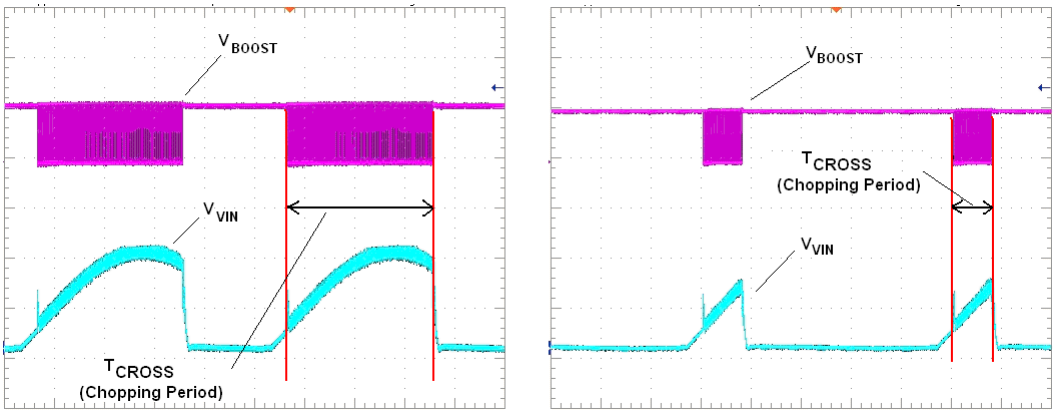


Figure 10. Chopper Operation (Trailing Edge Dimmer Mode)



Protection Features

The CY8CLEDAC02 has full featured circuit protection not normally available with other primary-side control solutions.

The built-in protection features include OOVP, OSCP, PCLP, CSSP, and OTP.

In an event a protection is triggered (except PCLP and OOVP), V_{CC} discharges below V_{CCUVL} and causes the digital logic to reset. The controller now initiates a new soft start cycle and continues to attempt startup. It is unable to startup until the fault condition is removed. PCLP does not trigger a shutdown. In case of OOVP the IC stays latched and cannot perform a reset unless the V_{CC} voltage drops approximately 1-2 V below V_{CCUVL} threshold.

Output Overvoltage Protection (OOVP)

The CY8CLEDAC02 includes a function that protects against an output overvoltage. The output voltage is monitored by the V_{SENSE} pin. The protection is triggered if the voltage at this pin exceeds the overvoltage threshold $V_{SENSE(MAX)}$.

Output Short Circuit Protection (OSCP)

The CY8CLEDAC02 includes a function that protects against an output short circuit. The output voltage is monitored by the V_{SENSE} pin. The protection is triggered if the voltage at this pin is below 0.22 V.

Overtemperature Protection (OTP)

The V_T pin along with an external NTC provides overtemperature protection. Having an internal current source to the pin allows for sensing the voltage across the NTC. The voltage across the pin is sampled once every AC half cycle and the protection mode is triggered if it reaches the V_T shutdown threshold (V_{SDTH}).

Current Sense Resistor Short Protection (CSSP)

If the I_{SENSE} sense resistor is shorted, there is a potential danger of an overcurrent condition not being detected. The CY8CLEDAC02 has a separate circuit to detect this fault. This protection mode is triggered if the I_{SENSE} voltage is below I_{SENSE} short protection reference (V_{RSNS}).

Peak Current Limit protection (PCLP)

The I_{SENSE} pin of the CY8CLEDAC02 monitors the primary peak current. This enables cycle-by-cycle peak current control and limiting. When the I_{SENSE} voltage is greater than the overcurrent limit threshold V_{OCP}, an overcurrent condition is detected and the IC immediately turns off the MOSFET driver. During the next switching cycle, the driver sends out a regular switching pulse and turns off again if the OCP threshold is still reached. Normal

switching resumes if the fault is removed and the OCP threshold is not reached.

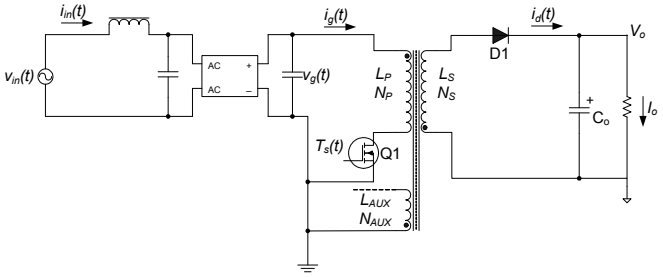
Single Point Fault Protection

The CY8CLEDAC02 can detect a short on any of the following pins V_{IN}, I_{SENSE}, V_{SENSE}, V_{CC}, OUTPUT, and V_T. Therefore any single point fault is protected against.

Understanding Primary Feedback

Figure 11 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_P. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

Figure 11. Simplified Flyback Converter



To tightly regulate output current, information about the load current needs to be accurately sensed. To achieve CC regulation, this information can be derived indirectly by sensing the primary current.

To detect faults with output voltage, information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read through the auxiliary winding.

During the Q1 on time, the load current is supplied from the output filter capacitor C_O. The voltage across L_P is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

Equation 4

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_P}$$

At the end of on time, the current has ramped up to:

Equation 5

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_P}$$

This current represents a stored energy of:

Equation 6

$$E_g = \frac{L_P}{2} \times i_{g\_peak}(t)^2$$

When Q1 turns off, $i_g(t)$ in L_P forces a reversal of polarities on all windings. Ignoring the commutation time caused by the leakage inductance L_{KP} at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

Equation 7

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t)$$

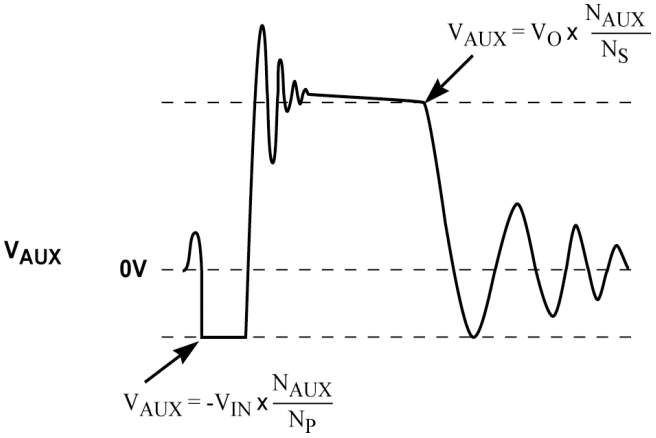
Assuming the secondary winding is master and the auxiliary winding is slave, the auxiliary voltage is given by:

Equation 8

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V)$$

and reflects the output voltage as shown in Figure 12 on page 11.

Figure 12. Auxiliary Voltage Waveforms



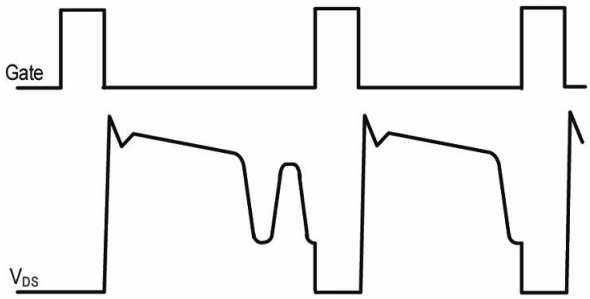
The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Further, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see Figure 12), then ΔV is also small. With the CY8CLEDAC02, ΔV can be ignored.

The real time waveform analyzer in the CY8CLEDAC02 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage V_{FB_C}. The V_{FB_C} signal precisely represents the output voltage and is used to sense the output voltage.

Valley Mode Switching

To reduce EMI and switching losses in the MOSFET, the CY8CLEDAC02 employs valley mode switching by switching at the lowest MOSFET V_{DS} (see Figure 13). It detects valleys in the MOSFET drain voltage indirectly through the V_{SENSE} pin. This voltage is provided by the auxiliary winding of the flyback transformer and represents a copy of the secondary side characteristics (see Figure 12).

Figure 13. Valley Mode Switching



Turning on at the lowest V_{DS} generates lowest dV/dt; thus valley mode switching can also reduce EMI. To limit the switching frequency range, the CY8CLEDAC02 can skip valleys (as shown in the first cycle in Figure 13) when the switching frequency becomes too high.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLEDAC02. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/powerpsoc. Specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 125 °C, except where noted.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested

Symbol	Description	Min	Typ	Max	Units	Notes
V_{CC}	DC supply voltage range	–0.3	–	18	V	Pin 8, I_{CC} = 20 mA max
I_{CC}	DC supply current at V_{CC} pin	–	–	20	mA	Pin 8
V_{OUT}	OUTPUT pin voltage	–0.3	–	18	V	Pin 7
V_{BOOST}	BOOST pin voltage	–0.3	–	18	V	Pin 1
V_{VSENSE}	V_{SENSE} pin voltage	–0.7	–	4	V	Pin 2, I_{VSENSE} ≤ 10mA
V_{VIN}	V_{IN} pin voltage	–0.3	–	18	V	Pin 3
V_{ISENSE}	I_{SENSE} pin voltage	–0.3	–	4	V	Pin 6
V_{VT}	V_T pin voltage	–0.3	–	4	V	Pin 4
P_D	Power dissipation	–	–	526	mW	T_A ≤ 25 °C
$T_{J\ MAX}$	Maximum junction temperature	–	–	125	°C	
T_{STG}	Storage temperature	–65	–	150	°C	
T_{LEAD}	Lead temperature	–	–	260	°C	During IR reflow for ≤ 15 seconds
θ_{JB}[1]	Thermal resistance junction-to-PCB board surface	–	–	70	°C/W	
V_{ESD}	ESD voltage rating	–	–	2000	V	According to JEDEC JESD22-A114
I_{LU}	Latch-up current	–100	–	100	mA	According to JEDEC JESD78

Note
1. θ_{JB} provides an estimation of the die temperature relative to the printed circuit board (PCB) surface temperature. This data is measured at the ground pin (pin 5) without using any thermal adhesives.

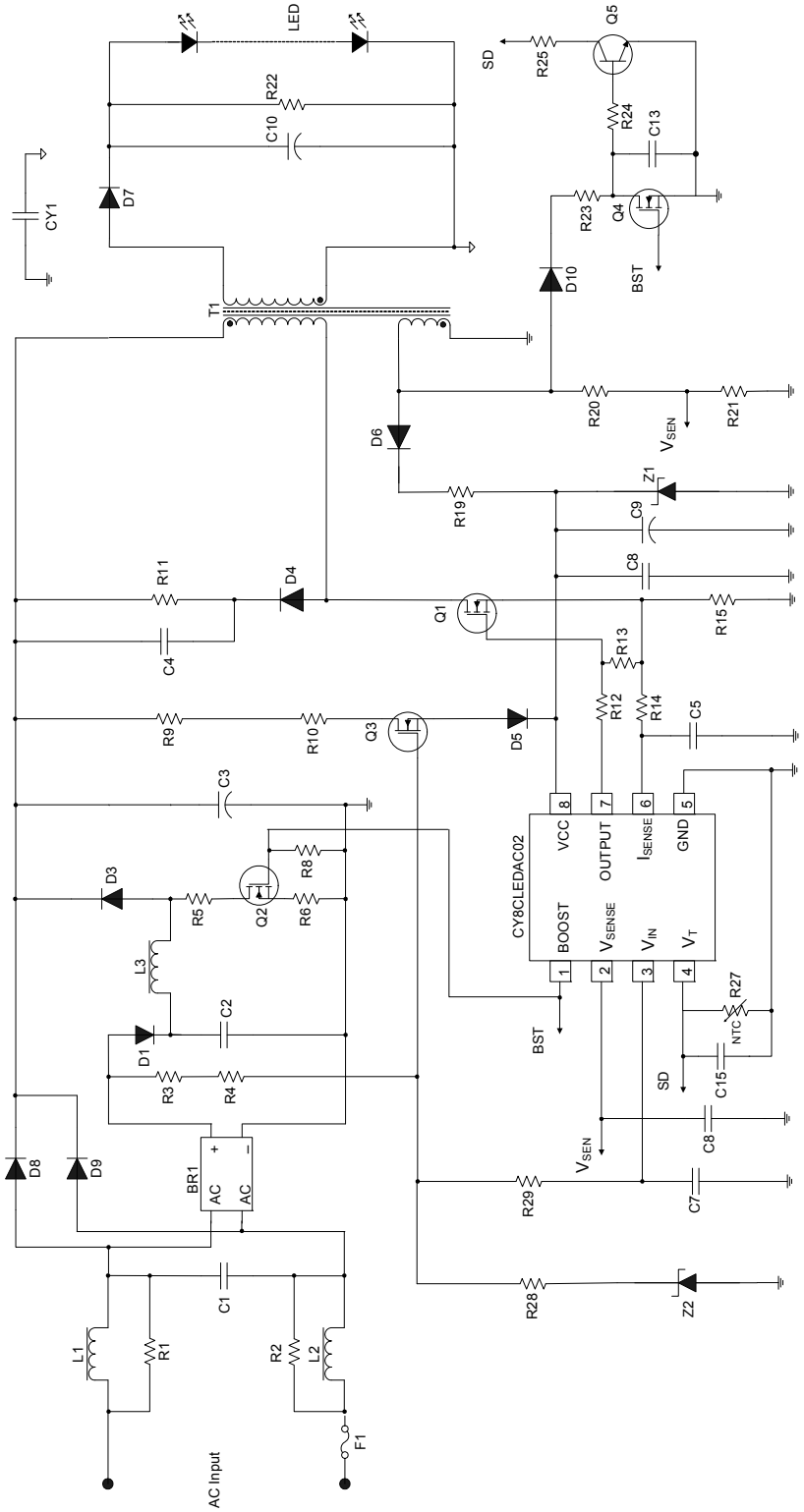
Electrical Characteristics

V_{CC}=12 V; –40 °C ≤ T_A ≤ 85 °C unless otherwise specified[2]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN} Section (pin 3)						
V_{IN}	Input voltage range	0	–	1.8	V	During normal operation (after startup)
I_{INST}	Startup current	–	10	15	µA	V_{IN} = 10 V, C_{VCC} = 10µF
Z_{VIN}	Input impedance	–	2.5	–	kΩ	During normal operation (after startup)
V_{SENSE} Section (pin 2)						
I_{BVS}	Input leakage current	–	–	1	µA	V_{SENSE} = 2 V
$V_{SENSENOM}$	Nominal voltage threshold	1.523	1.538	1.553	V	T_A = 25 °C, Negative edge
$V_{SENSEMAX}$	Output OVP threshold	1.683	1.700	1.717	V	T_A = 25 °C, Negative edge
OUTPUT Section (pin 7)						
$R_{DS(ON)LO}$	Output low level ON-Resistance	–	30	–	Ω	I_{SINK} = 5 mA
$R_{DS(ON)HI}$	Output high level ON-Resistance	–	60	–	Ω	I_{SOURCE} = 5 mA
t_R[3]	Rise time (10 percent to 90 percent)	–	50	–	ns	T_A = 25 °C, C_L = 330pF
t_F[3]	Fall time (90 percent to 10 percent)	–	30	–	ns	T_A = 25 °C, C_L = 330pF
f_{SWMAX}[4]	Maximum switching frequency	–	200	–	kHz	
V_{CC} Section (pin 8)						
V_{CCMAX}	Maximum operating voltage	–	–	16	V	
V_{CCST}	Startup threshold	11	12	13	V	V_{CC} Rising
V_{CCUVL}	Undervoltage lockout threshold	7.0	7.5	8.0	V	V_{CC} Falling
I_{CC}	Operating current	–	3.9	4.5	mA	C_L = 330pF, V_{SENSE} = 1.5 V
$V_{CC-CLAMP}$	Zener diode clamp voltage	–	19	–	V	Test current of 10 mA
I_{SENSE} Section (pin 6)						
V_{OCP}	Overcurrent threshold limit	–	1.9	–	V	
V_{RSNS}	I_{SENSE} short protection reference	–	0.16	–	V	
V_{REGTH}	CC regulation threshold limit	–	1.8	–	V	
V_T Section (pin 4)						
V_{SDTH}	Shutdown threshold	–	0.09	–	V	
I_{BVSD}	Input leakage current	–	–	1.0	µA	V_{SD} = 1.0V
I_{SD}	Pull-up current source	95	100	105	µA	
BOOST Section (pin 1)						
$R_{DS(ON)LO-TR}$	Output low level ON-Resistance	–	100	–	Ω	I_{SINK} = 5 mA
$R_{DS(ON)HI-TR}$	Output high level ON-Resistance	–	200	–	Ω	I_{SOURCE} = 5 mA
t_{R-BST}[3]	Rise time	–	60	–	ns	
t_{F-BST}[3]	Fall time	–	60	–	ns	

Notes
2. Adjust V_{CC} above startup threshold before setting at 12 V.
3. These parameters are not 100 percent tested, guaranteed by design and characterization.
4. Operating frequency varies based on line and load conditions.

Typical Application Diagram



Typical Performance Characteristics

Figure 14. V_{CC} vs. V_{CC} Supply Startup Current

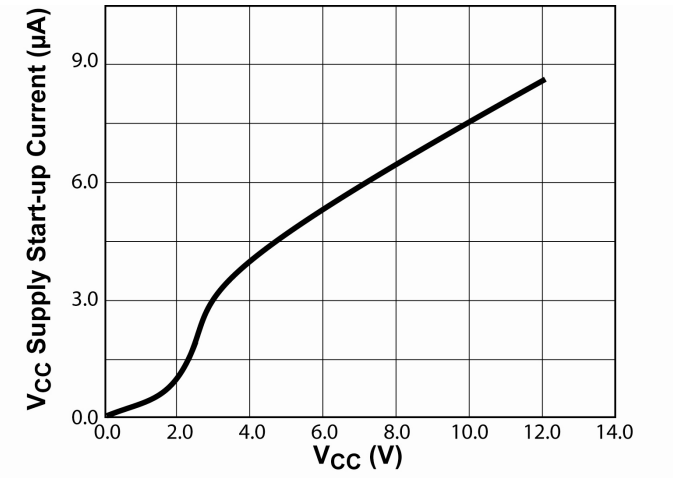


Figure 15. V_{CC} Startup Threshold Vs. Temperature

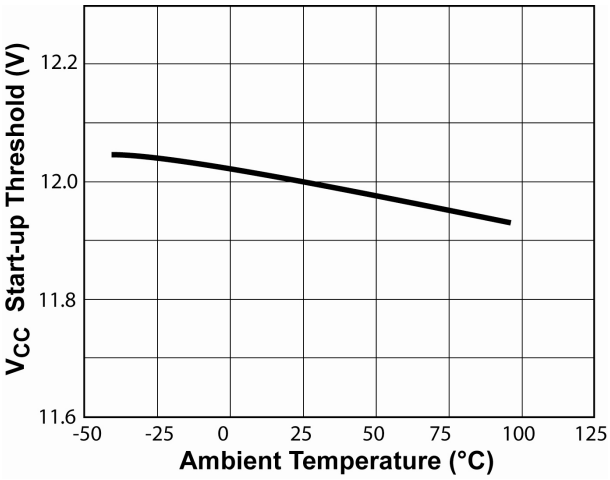


Figure 16. Percent Deviation of Switching Frequency to Ideal Switching Frequency With Temperature

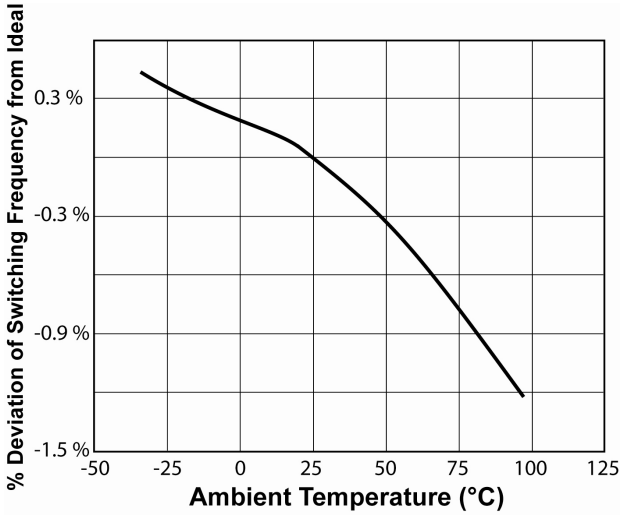
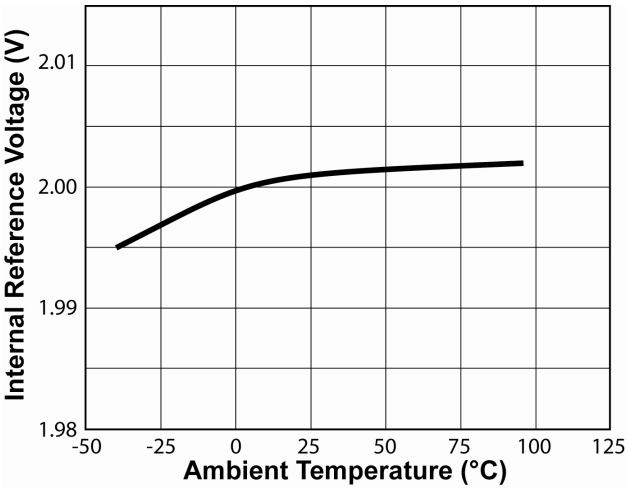


Figure 17. Internal Reference Voltage Vs. Temperature



Performance Information

Figure 18. Inrush and AC Peak Current (Trailing Edge)

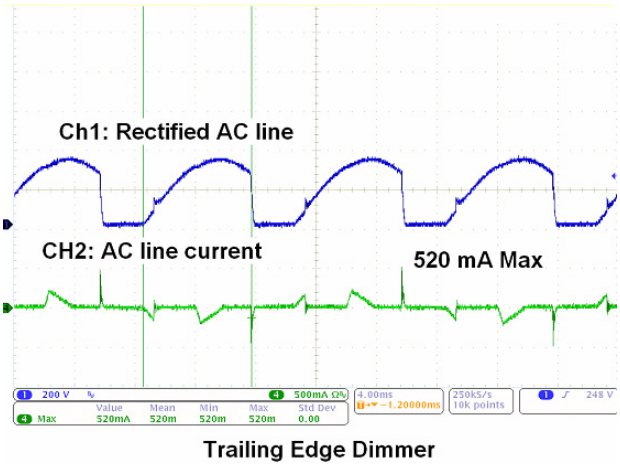


Figure 19. Inrush and AC Peak Current (Trailing Edge)

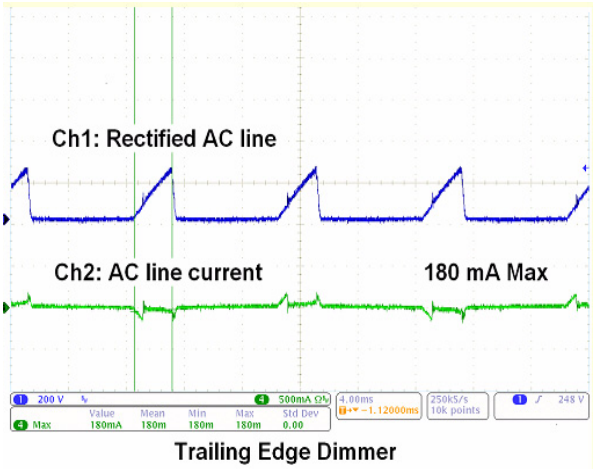


Figure 20. Inrush and AC Peak Current (Leading Edge)

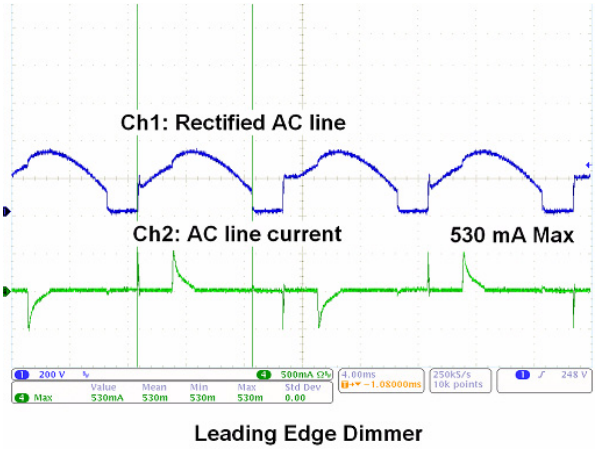


Figure 21. Inrush and AC Peak Current (Leading Edge)

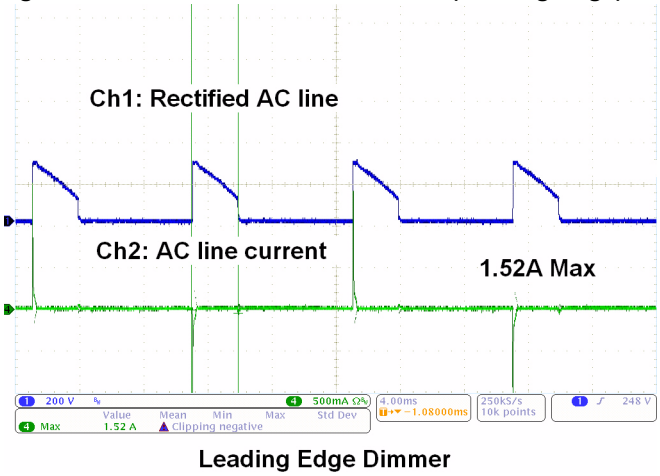


Figure 22. Inrush and AC Peak Current (No Dimmer)

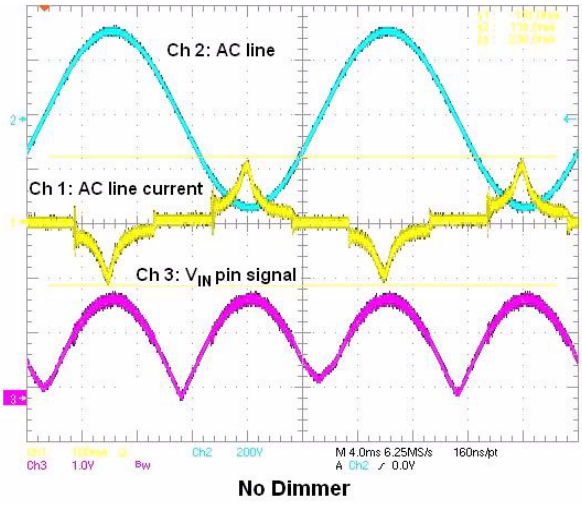
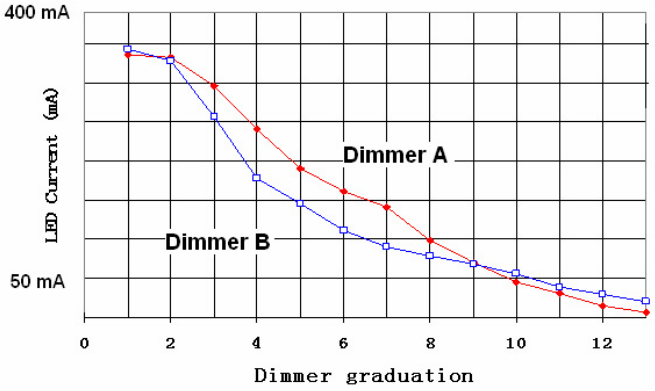


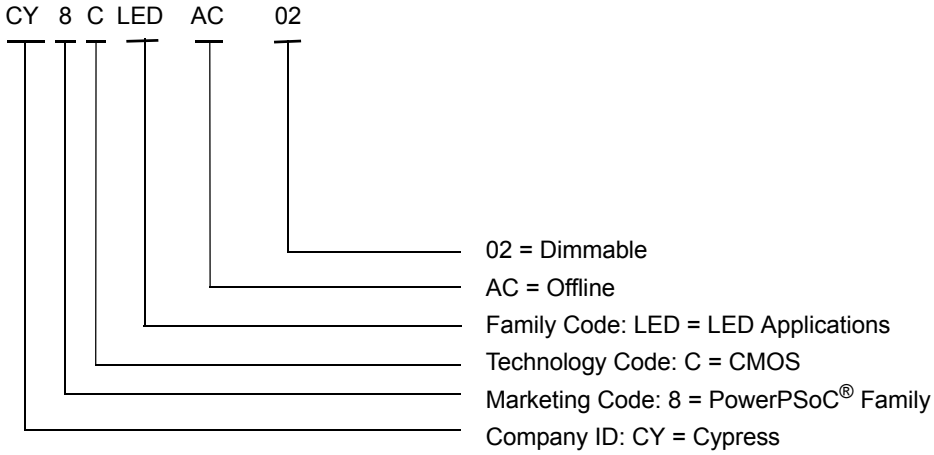
Figure 23. Dimming Curve



Ordering Information

Ordering Code	No. of Pins	Package	Temperature Range
CY8CLEDAC02	8	SOIC	–40 °C to 85 °C

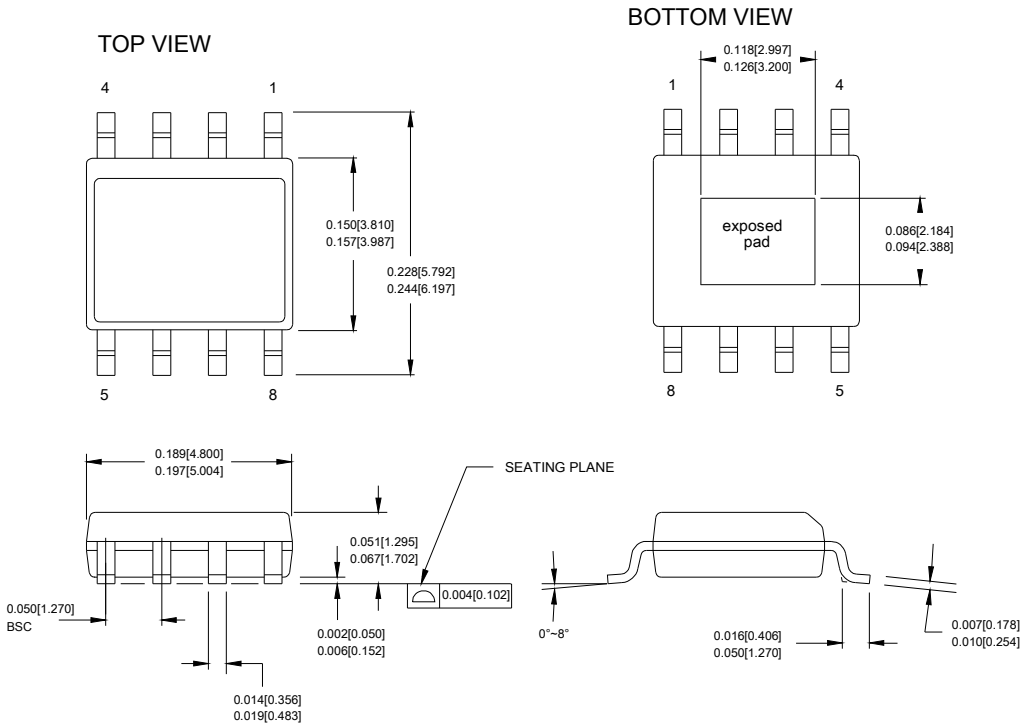
Ordering Code Definitions



Packaging Information

Physical Package Dimensions

Figure 14. 8-Pin Small Outline (SOIC) Package



1. DIMENSIONS IN INCHES[MM]
2. REFERENCE JEDEC MS-012F
3. PACKAGE WEIGHT 0.07 gm

001-54263 *A

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CDCM	critical discontinuous conduction mode
CSSP	current-sense resistor short protection
OSCP	output short circuit protection
OTP	over-temperature protection
OVP	output over-voltage protection
OOVP	output overvoltage protection
PCB	printed circuit board
PCLP	peak current limit protection
PWM	pulse width modulation
ZCD	zero-cross detect

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	Kbit	1024 bits	mA	milliampere
dB	decibels	KHz	kilohertz	ms	millisecond
Hz	Hertz	KΩ	kilohms	mV	millivolts
pp	peak-to-peak	MHz	megahertz	mA	milliwatts
σ	sigma:one standard deviation	MΩ	megaohms	nA	nanoamperes
V	volts	µA	microamperes	ns	nanoseconds
Ω	ohms	µF	microfarads	nV	nanovolts
KB	1024 bytes	µH	microhenrys	pA	picoamperes
ppm	parts per million	µs	microseconds	pF	picofarads
sps	samples per second	µV	microvolts	ps	picoseconds
W	watts	µVrms	microvolts root-mean-square	fF	femtofarads
A	amperes	µW	microwatts		

Document History Page

Document Title: CY8CLEDAC02 AC-DC Controller for Dimmable LED Lighting Document Number: 001-54879				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2746461	KJV	07/30/09	Preliminary data sheet
*A	2882776	KJV/AESA	02/22/2010	Updated Features, Description, and Functional Description sections. Updated Electrical Specifications. Updated package diagram. Added Contents. Updated links in Sales, Solutions, and Legal Information.
*B	2901104	KJV/VED	03/29/2010	Release to web
*C	3071772	KJV	10/26/2010	Updated "Pin Information" on page 4 and "Chopping Operation" on page 8 Updated Template

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