TDA9885; TDA9886

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

Rev. 03 — 16 December 2008 Product data sheet

1. General description

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal Phase-Locked Loop (PLL) demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

2. Features

- 5 V supply voltage
- Gain controlled wideband Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage-Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4 MHz, 33.9 MHz, 38.0 MHz, 38.9 MHz, 45.75 MHz and 58.75 MHz
- 4 MHz reference frequency input: signal from PLL tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C-bus
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
- SIF AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise

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- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module ADdress (MAD)

3. Applications

- TV, VTR, PC, and STB applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
τ_P	time constant (R × C) for network at pin V_P	for applications without I²C-bus		1.2	-	-	µs
Video part							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output		-	60	100	µV
$G_{VIF(cr)}$	control range VIF gain	see Figure 9		60	66	-	dB
f_{VIF}	vision carrier operating frequencies	see Table 13		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Figure 12		-	±2.3	-	MHz
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7					
		normal mode (sound carrier trap active) and sound carrier on		1.7	2.0	2.3	V
		trap bypass mode and sound carrier off	[2]	0.95	1.10	1.25	V
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[3]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	2	4	deg
$B_{v(-1dB)}$	–1 dB video bandwidth	trap bypass mode and sound carrier off; AC load: C_L < 20 pF, R_L > 1 kΩ	[2]	5	6	-	MHz
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[4]	3.95	4.05	-	MHz
		f_{trap} = 5.5 MHz	[4]	4.90	5.00	-	MHz
		f_{trap} = 6.0 MHz	[4]	5.40	5.50	-	MHz
		f_{trap} = 6.5 MHz	[4]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz		30	36	-	dB
		f = 5.5 MHz		30	36	-	dB

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Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S/N_W	weighted signal-to-noise ratio	unified weighting filter (*"ITU-T J.61"*); see Figure 13	[5]	56	59	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC} / \Delta f_{VIF}$		0.85	1.05	1.25	µA/kHz
Audio part							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
THD	total harmonic distortion	25 kHz FM deviation; 50 µs de-emphasis		-	0.15	0.50	%
		54 % AM modulation		-	0.5	1.0	%
$B_{AF(-3dB)}$	−3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter of Figure 26		80	100	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	black picture; see Figure 21		50	56	-	dB
		in accordance with *"ITU-R BS.468-4"*		45	50	-	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		40	46	-	dB
$PSRR_{AM}$	power supply ripple rejection	see Figure 8		20	26	-	dB
$PSRR_{FM}$	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 8		14	20	-	dB
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off		90	140	180	mV
		L standard; without modulation		90	140	180	mV
		intercarrier mode; PC / SC_1 = 20 dB; SC_2 off	[6]	-	75	-	mV
Reference frequency input; pin REF							
f_{ref}	reference signal frequency		[7]	-	4	-	MHz
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal		80	-	400	mV

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).

[3] Condition: luminance range (5 steps) from 0 % to 100 %.

[4] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figure 15 to Figure 20; $|H(s)|$ is the absolute value of transfer function).

[5] S/N is the ratio of black-to-white amplitude to the noise voltage (RMS value measured on pin CVBS and tested at video black level, 'quiet line'). Noise analyzer settings: B = 5 MHz, 200 kHz high-pass and sound carrier trap on. In case of S/N_W weighted in accordance with *"ITU-T J.61"*. Measurements taken for B/G standard.

[6] The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference: $V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^{r}\ V$ and $r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6\ dB \pm 3\ dB\right)$, where: $\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(dB)$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

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[7] Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V3	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
TDA9886T/V4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886HN/V4	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
TDA9885T/V5	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V5	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
TDA9886T/V5	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V5	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886HN/V5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

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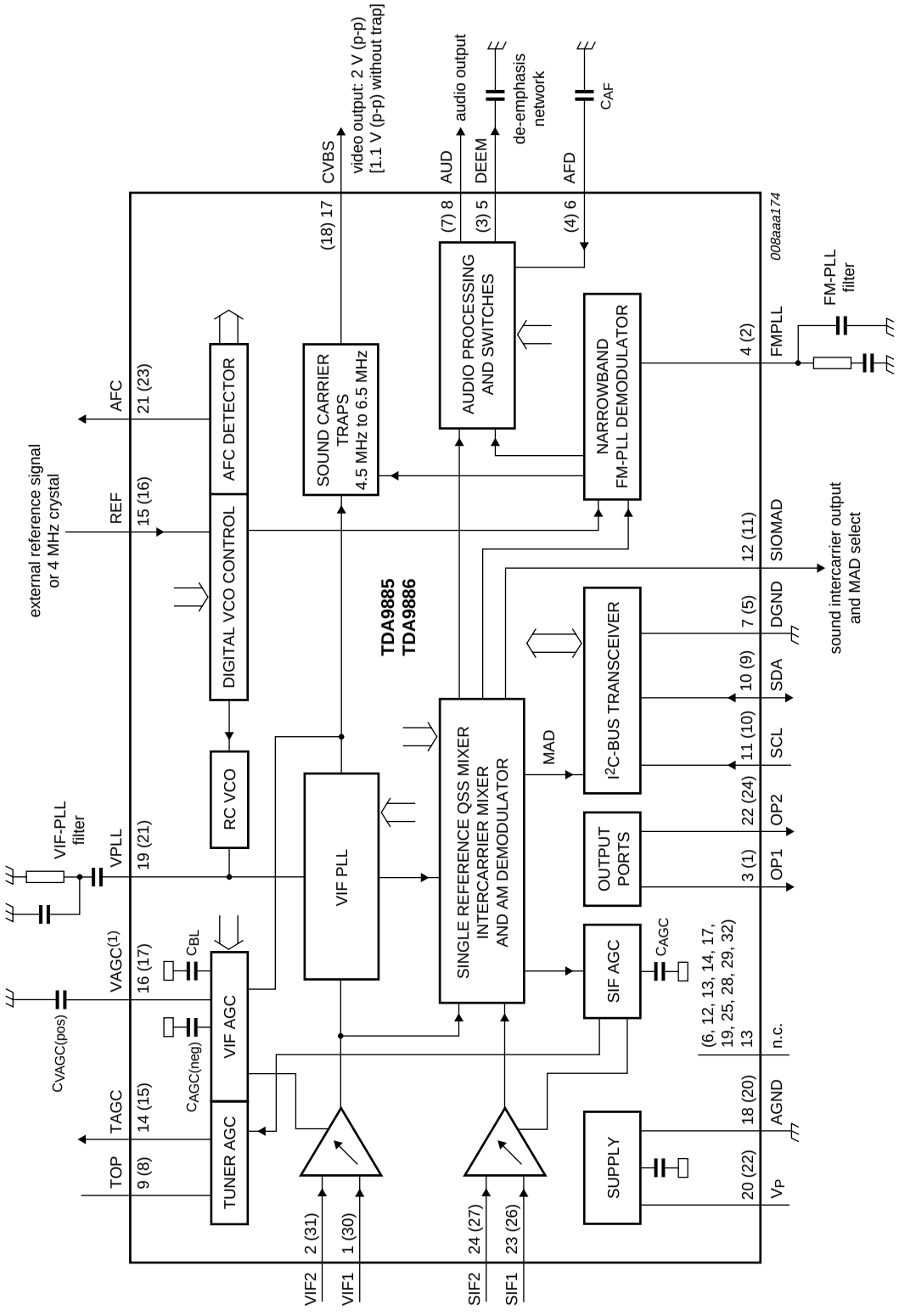
6. Block diagram



Pin numbers for TDA9885HN and TDA9886HN in parentheses.

(1) Not connected for TDA9885

Fig 1. Block diagram of TDA9885; TDA9886

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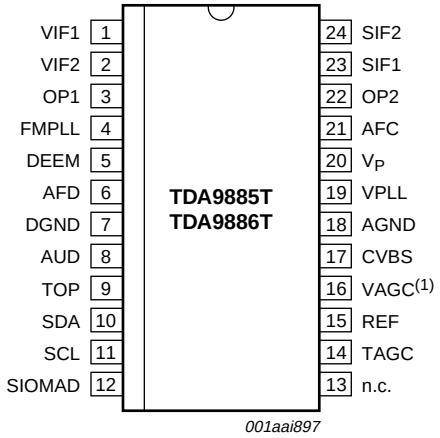
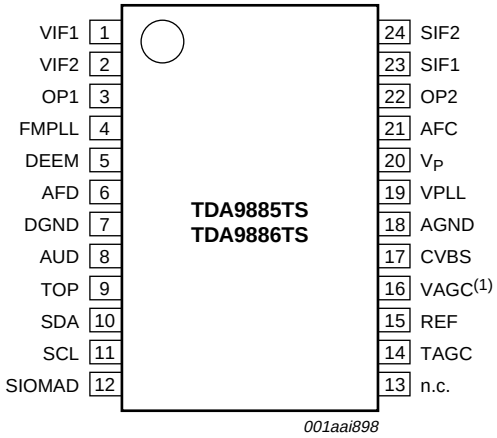
7. Pinning information

7.1 Pinning



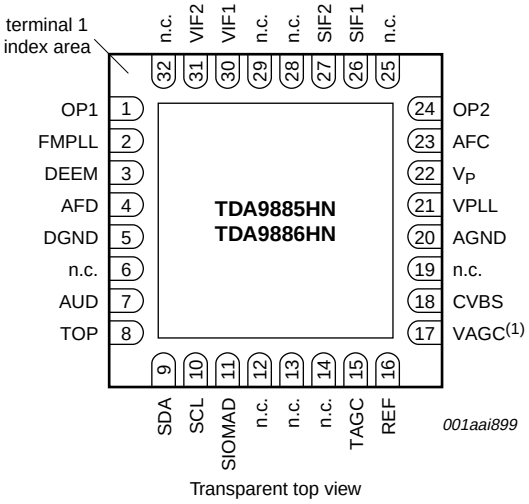
(1) Not connected for TDA9885T

Fig 2. Pin configuration for SO24



(1) Not connected for TDA9885TS

Fig 3. Pin configuration for SSOP24



(1) Not connected for TDA9885HN

Fig 4. Pin configuration for HVQFN32

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7.2 Pin description

Table 3. Pin description

Symbol	Pin				Description
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	-	-	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF DC-decoupling capacitor
DGND	7	7	5	5	digital ground
n.c.	-	-	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TOP for resistor adjustment
SDA	10	10	9	9	I²C-bus data input and output
SCL	11	11	10	10	I²C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	-	-	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	-	-	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	-	16	-	17	VIF AGC for capacitor
n.c.	16	-	17	-	not connected
CVBS	17	17	18	18	composite video output
n.c.	-	-	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	-	-	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	-	-	28	28	not connected
n.c.	-	-	29	29	not connected

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8. Functional description

Figure 1 shows the simplified block diagram of the device which comprises the following functional blocks:

- VIF amplifier
- Tuner AGC and VIF AGC
- VIF-AGC detector
- Frequency Phase-Locked Loop (FPLL) detector
- VCO and divider
- AFC and digital acquisition help
- Video demodulator and amplifier
- Sound carrier trap
- SIF amplifier
- SIF-AGC detector
- Single reference QSS mixer
- AM demodulator
- FM demodulator and acquisition help
- Audio amplifier and mute time constant
- Internal voltage stabilizer
- I²C-bus transceiver and MAD

8.1 VIF amplifier

The VIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration and collector resistor variation. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

8.2 Tuner AGC and VIF AGC

This block adapts the voltage, generated at the VIF-AGC detector, to the internal signal processing at the VIF amplifier and performs the tuner AGC control current generation. The onset of the tuner AGC control current generation can be set either via the I²C-bus (see Table 12) or optionally by a potentiometer at pin TOP (in case that the I²C-bus information cannot be stored, related to the device). The presence of a potentiometer is automatically detected and the I²C-bus setting is disabled.

Furthermore, derived from the AGC detector voltage, a comparator is used to detect if the corresponding VIF input voltage is higher than 200 μV. This information can be read out via the I²C-bus (bit VIFLEV = 1).

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8.3 VIF-AGC detector

Gain control is performed by sync level detection (negative modulation) or peak white detection (positive modulation).

For negative modulation, the sync level voltage is stored at an integrated capacitor by means of a fast peak detector. This voltage is compared with a reference voltage (nominal sync level) by a comparator which charges or discharges the integrated AGC capacitor for providing of the required VIF gain. The time constants for decreasing or increasing the gain are nearly equal and the total AGC reaction time is fast to cope with 'aeroplane fluttering'.

For positive modulation, the white peak level voltage is compared with a reference voltage (nominal white level) by a comparator which charges (fast) or discharges (slow) the external AGC capacitor directly for providing the required VIF gain. The need of a very long time constant for VIF gain increase is due to peak white level may appear only once in a field. In order to reduce this time constant, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step controlled by the detected actual black level voltage. The threshold level for fast mode AGC is typically −6 dB video amplitude. The fast mode state is also transferred to the SIF-AGC detector for speed-up. In case of missing peak white pulses, the VIF gain increase is limited to typically +3 dB by comparing the detected actual black level voltage with a corresponding reference voltage.

8.4 FPLL detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier for removing the video AM.

During acquisition the frequency detector produces a current proportional to the frequency difference between the VIF and the VCO signals. After frequency lock-in the phase detector produces a current proportional to the phase difference between the VIF and the VCO signals. The currents from the frequency and phase detectors are charged into the loop filter which controls the VIF VCO and locks it to the frequency and phase of the VIF carrier.

For a positive modulated VIF signal, the charging currents are optional gated by the composite sync in order to avoid signal distortion in case of overmodulation. The gating depth is switchable via the I²C-bus.

8.5 VCO and divider

The VCO of the VIF FPLL operates as an integrated low radiation relaxation oscillator at double the picture carrier frequency. The control voltage, required to tune the VCO to double the picture carrier frequency, is generated at the loop filter by the frequency phase detector. The possible frequency range is 50 MHz to 140 MHz (typical value).

The oscillator frequency is divided-by-two to provide two differential square wave signals with exactly 90 degrees phase difference, independent of the frequency, for use in the FPLL detectors, the video demodulator and the intercarrier mixer.

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8.6 AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL.

The in-window and out-window control at the FM PLL is additionally used to mute the audio stage (if auto mute is selected via the I²C-bus).

The working principle of the digital acquisition help is as follows. The PLL VCO output is connected to a down counter which has a predefined start value (standard dependent). The VCO frequency clocks the down counter for a fixed gate time. Thereafter, the down counter stop value is analyzed. In case the stop value is higher (lower) than the expected value range, the VCO frequency is lower (higher) than the wanted lock-in window frequency range. A positive (negative) control current is injected into the PLL loop filter and consequently the VCO frequency is increased (decreased) and a new counting cycle starts.

The gate time as well as the control logic of the acquisition help circuit is dependent on the precision of the reference signal at pin REF. Operation as a crystal oscillator is possible as well as connecting this input via a serial capacitor to an external reference frequency, e.g. the tuning system oscillator.

The AFC signal is derived from the corresponding down counter stop value after a counting cycle. The last four bits are latched and can be read out via the I²C-bus (see Table 8). Also the digital-to-analog converted value is given as current at pin AFC.

8.7 Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The VIF signal is multiplied with the ‘in phase’ signal of the VIF-PLL VCO.

The demodulator output signal is fed into the video preamplifier via a level shift stage with integrated low-pass filter to achieve carrier harmonics attenuation.

The output signal of the preamplifier is fed to the VIF-AGC detector (see Section 8.3) and in the sound trap mode also fed internally to the integrated sound carrier trap (see Section 8.8). The differential trap output signal is converted to a single-ended signal and amplified by the following post-amplifier. The video output level at pin CVBS is 2 V (p-p).

In the trap bypass mode the output signal of the preamplifier is fed directly through the post-amplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10 % overall loss.

Noise clipping is provided in both cases.

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8.8 Sound carrier trap

The sound trap is constructed of three separate traps to realize sufficient suppression of the first and second sound carriers.

For frequency control of the sound trap additionally a reference low-pass filter and a phase detector are built in.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces a DC voltage by charging or discharging an integrated capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage controls the frequency position of the reference filter and the sound trap. So the accurate frequency position for the different standards is set by the sound carrier reference signal.

8.9 SIF amplifier

The SIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration and collector resistor variation. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

8.10 SIF-AGC detector

SIF gain control is performed by detection and controlling to a reference value of the DC component of the AM demodulator output signal. This DC signal corresponds directly to the SIF voltage at the output of the SIF amplifier so that a constant SIF signal is supplied to the AM demodulator and to the single reference QSS mixer.

By switching the gain of the input amplifier of the SIF-AGC detector via the I²C-bus, the internal SIF level for FM sound is 5.5 dB lower than for AM sound. This is to adapt the SIF-AGC characteristic to the VIF-AGC characteristic. The adaption is ideal for a picture-to-sound FM carrier ratio of 13 dB.

Via a comparator, the integrated AGC capacitor is charged or discharged for providing the required SIF gain. Due to AM sound, the AGC reaction time is slow (f_c < 20 Hz for the GC cc-tr11m3[amula4rg t0psrg t0pTD 215(viding)-252(the)]TJ 0 -2-273(A)30(G)0(C)-2p(C)hM(1;)-25

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9.2.1 Subaddress (A data)

If more than one data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 9.

Table 9. Definition of the subaddress (second byte after slave address)
X = don't care.

Register	MSB							LSB
	A7[1]	A6[2]	A5[2]	A4[2]	A3[2]	A2[2]	A1	A0
SAD for switching mode	0	X	X	X	X	X	0	0
SAD for adjust mode	0	X	X	X	X	X	0	1
SAD for data mode	0	X	X	X	X	X	1	0

[1] Bit A7 = 1 is not allowed.

[2] Bits A6 to A2 will be ignored by the internal hardware.

9.2.2 Data byte for switching mode (B data)

Table 10. Bit description of SAD register for switching mode (SAD = 00)

Bit	Symbol	Description
7	B7	output port 2 for SAW switching or monitoring
		1 = high-impedance, disabled or HIGH
		0 = low-impedance, active or LOW
6	B6	output port 1 for SAW switching or external input
		1 = high-impedance, disabled or HIGH
		0 = low-impedance, active or LOW
5	B5	forced audio mute
		1 = on
		0 = off
4 and 3	B[4:3]	TV standard modulation
		00 = positive AM TV[1]
		01 = not used
		10 = negative FM TV
		11 = not used
2	B2	carrier mode
		1 = QSS mode
		0 = intercarrier mode
1	B1	auto mute of FM AF output
		1 = active
		0 = inactive
0	B0	video mode (sound trap)
		1 = sound trap bypass
		0 = sound trap active

[1] For positive AM TV choose 6.5 MHz for the second SIF.

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9.2.3 Data byte for adjust mode (C data)

Table 11. Bit description of SAD register for adjust mode (SAD = 01)

Bit	Symbol	Description
7	C7	audio gain
		1 = –6 dB
		0 = 0 dB
6	C6	de-emphasis time constant
		1 = 50 µs
		0 = 75 µs
5	C5	de-emphasis
		1 = on
		0 = off
4 to 0	C[4:0]	tuner TOP adjustment; see Table 12

Table 12. Tuner takeover point adjustment bits

Bit					TOP adjustment (dB)
C4	C3	C2	C1	C0	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0[1]
0	1	1	1	1	–1
0	1	1	1	0	–2
0	1	1	0	1	–3
0	1	1	0	0	–4
0	1	0	1	1	–5
0	1	0	1	0	–6
0	1	0	0	1	–7
0	1	0	0	0	–8
0	0	1	1	1	–9
0	0	1	1	0	–10

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Table 12. Tuner takeover point adjustment bits *…continued*

Bit					TOP adjustment (dB)
C4	C3	C2	C1	C0	
0	0	1	0	1	–11
0	0	1	0	0	–12
0	0	0	1	1	–13
0	0	0	1	0	–14
0	0	0	0	1	–15
0	0	0	0	0	–16

[1] For 0 dB refer to Section 12 symbol QV_{TOP}.

9.2.4 Data byte for data mode (E data)

Table 13. Bit description of SAD register for data mode (SAD = 10)

Bit	Symbol	Description
7	E7	VIF AGC and port features; dependent on bit E5; see Table 14
6	E6	L standard PLL gating
		1 = gating in case of 36 % positive modulation
		0 = gating in case of 0 % positive modulation
5	E5	VIF, SIF and tuner minimum gain; dependent on bit E7; see Table 14
4 to 2	E[4:2]	vision intermediate frequency selection; see Table 15
1 and 0	E[1:0]	sound intercarrier frequency selection (sound 2nd IF)
		00 = f_{FM} = 4.5 MHz
		01 = f_{FM} = 5.5 MHz
		10 = f_{FM} = 6.0 MHz
		11 = f_{FM} = 6.5 MHz[1]

[1] For positive modulation choose 6.5 MHz.

Table 14. Options in extended TV mode; bit B3 = 0 of SAD 00 register

Function	Bit E7 = 0		Bit E7 = 1	
	Bit E5 = 0	Bit E5 = 1	Bit E5 = 0	Bit E5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input[1]
Pin OP2	port function	port function	VIF-AGC output[1]	port function
Gain	normal gain	minimum gain	normal gain	external gain

[1] The corresponding port function has to be disabled (set to ‘high-impedance’); see Table 10 and Table note 12 of Table 20.

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Table 15. TV standard selection for VIF

Video IF select bits			f_{VIF} (MHz)
E4	E3	E2	
0	0	0	58.75[1]
0	0	1	45.75[1]
0	1	0	38.9
0	1	1	38.0
1	0	0	33.9
1	0	1	33.4
1	1	0	not applicable
1	1	1	not applicable

[1] Pin SIOMAD can be used for the selection of the different NTSC standards without I²C-bus. With a resistor on pin SIOMAD, f_{VIF} = 58.75 MHz; without a resistor on pin SIOMAD, f_{VIF} = 45.75 MHz (NTSC-M).

Table 16. Data setting after power-on reset (default setting with a resistor on pin SIOMAD)

Register	Byte							
	MSB							LSB
	7	6	5	4	3	2	1	0
Switching mode (B data)	1	1	0	1	0	1	1	0
Adjust mode (C data)	0	0	1	1	0	0	0	0
Data mode (E data)	0	0	0	0	0	0	0	0

Table 17. Data setting after power-on reset (default setting without a resistor on pin SIOMAD)

Register	Byte							
	MSB							LSB
	7	6	5	4	3	2	1	0
Switching mode (B data)	1	1	0	1	0	1	1	0
Adjust mode (C data)	0	0	1	1	0	0	0	0
Data mode (E data)	0	0	0	0	0	1	0	0

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10. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage			-	5.5	V
V_n	voltage on					
	pins VIF1, VIF2, SIF1, SIF2, OP1, OP2, V_P and FMPLL			0	V_P	V
	pin TAGC			0	8.8	V
t_{sc}	short-circuit time	to ground or V_P		-	10	s
T_{stg}	storage temperature			–25	+150	°C
T_{amb}	ambient temperature	TDA9885T (SO24), TDA9885TS (SSOP24), TDA9886T (SO24) and TDA9886TS (SSOP24)		–20	+70	°C
		TDA9885HN (HVQFN32) and TDA9886HN (HVQFN32)		–20	+85	°C
V_{esd}	electrostatic discharge voltage	machine model	[1]	–400	+400	V
		human body model	[2]	–4000	+3500	V

[1] Class C according to EIA/JESD22-A115.

[2] Class 2 according to JESD22-A114.

11. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9885T (SO24)		76	K/W
	TDA9885TS (SSOP24)		118	K/W
	TDA9885HN (HVQFN32)		40	K/W
	TDA9886T (SO24)		76	K/W
	TDA9886TS (SSOP24)		118	K/W
	TDA9886HN (HVQFN32)		40	K/W

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12. Characteristics

Table 20. Characteristics

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply; pin V_P							
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
P_{tot}	total power dissipation			-	305	385	mW
Power-on reset							
$V_{P(start)}$	supply voltage for start of reset	decreasing supply voltage		2.5	3.0	3.5	V
$V_{P(stop)}$	supply voltage for end of reset	increasing supply voltage; I²C-bus transmission enable		-	-	4.4	V
τ_P	time constant (R × C) for network at pin V_P	for applications without I²C-bus		1.2	-	-	µs
VIF amplifier; pins VIF1 and VIF2							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output		-	60	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	+1 dB video at output		150	190	-	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)		[2]	-	-	440	mV
$\Delta V_{IF(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5.5 MHz		-	0.7	-	dB
$G_{VIF(cr)}$	control range VIF gain	see Figure 9		60	66	-	dB
$B_{VIF(-3dB)(ll)}$	lower limit –3 dB VIF bandwidth			-	15	-	MHz
$B_{VIF(-3dB)(ul)}$	upper limit –3 dB VIF bandwidth			-	80	-	MHz
$R_{i(dif)}$	differential input resistance		[3]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[3]	-	3	-	pF
V_I	DC input voltage			-	1.93	-	V
FPLL and true synchronous video demodulator			[4]				
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$		120	140	-	MHz
f_{VIF}	vision carrier operating frequencies	see Table 13		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Figure 12		-	±2.3	-	MHz

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{acq}	acquisition time	BL = 70 kHz	[5]	-	-	30	ms
$V_{i(lock)(rms)}$	input voltage sensitivity for PLL to be locked (RMS value)	measured on pins VIF1 and VIF2; maximum IF gain		-	30	70	µV
$T_{cy(dah)}$	digital acquisition help cycle time			-	64	-	µs
$K_{O(VIF)}$	VIF VCO steepness	definition: $\Delta f_{VIF} / \Delta V_{VPLL}$		-	20	-	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	definition: $\Delta I_{VPLL} / \Delta \varphi_{VIF}$		-	23	-	µA/rad
Video output 2 V; pin CVBS							
Normal mode (sound carrier trap active) and sound carrier on							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7		1.7	2.0	2.3	V
ΔV_o	video output voltage difference	difference between L and B/G standard		–12	-	+12	%
V/S	ratio between video (black-to-white) and sync level			1.90	2.33	3.00	
V_{sync}	sync voltage level			1.0	1.2	1.4	V
$V_{clip(u)}$	upper video clipping voltage level			V_P – 1.1	V_P – 1	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.7	0.9	V
R_o	output resistance		[3]	-	-	30	Ω
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower		1.5	2.0	-	mA
$I_{sink(o)(max)}$	maximum output sink current	AC and DC		1	-	-	mA
$I_{source(o)(max)}$	maximum output source current	AC and DC		3.9	-	-	mA
$\Delta V_{o(CVBS)}$	deviation of CVBS output voltage	50 dB gain control		-	-	0.5	dB
		30 dB gain control		-	-	0.1	dB
$\Delta V_{o(bl)}$	black level tilt	negative modulation		-	-	1	%
$\Delta V_{o(bl)(v)}$	vertical black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only		-	-	3	%
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[6]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	2	4	deg
S/N_W	weighted signal-to-noise ratio	unified weighting filter (*"ITU-T J.61"*); see Figure 13	[7]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[7]	47	51	-	dB
$\alpha_{IM(blue)}$	intermodulation attenuation at 'blue'	see Figure 14	[8]				
		f = 1.1 MHz		58	64	-	dB
		f = 3.3 MHz		58	64	-	dB

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\alpha_{IM(yellow)}$	intermodulation attenuation at 'yellow'	see Figure 14	[8]				
		f = 1.1 MHz		60	66	-	dB
		f = 3.3 MHz		59	65	-	dB
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics		-	2	5	mV
$\Delta f_{unw(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	3 % residual carrier; 50 % serration pulses; L standard	[3]	-	-	12	kHz
$\Delta\varphi$	robustness for modulator imbalance	0 % residual carrier; 50 % serration pulses; L standard; L-gating = 0 %	[3]	-	-	3	%
α_H	suppression of video signal harmonics	AC load: C_L < 20 pF, R_L > 1 kΩ	[9]	35	40	-	dB
α_{spur}	suppression of spurious elements		[10]	40	-	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB
M/N standard including Korea; see Figure 15							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[11]	3.95	4.05	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 4.5 MHz		21	27	-	dB
α_{SC2}	attenuation at second sound carrier	f = 4.724 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 4.724 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 3.58 MHz; see Figure 16		110	180	250	ns
B/G standard; see Figure 17							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 5.5 MHz	[11]	4.90	5.00	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 5.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 5.5 MHz		24	30	-	dB
α_{SC2}	attenuation at second sound carrier	f = 5.742 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 5.742 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz; see Figure 18		110	180	250	ns

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I standard; see Figure 19							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.0 MHz	[11]	5.40	5.50	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.0 MHz		26	32	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.0 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.55 MHz		12	18	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.55 MHz		10	15	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz		-	90	160	ns
D/K standard; see Figure 20							
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.5 MHz	[11]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.5 MHz		26	32	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.5 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.742 MHz		18	24	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.742 MHz		13	18	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.28 MHz		-	60	130	ns
Video output 1.1 V; pin CVBS							
Trap bypass mode and sound carrier off[12]							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7		0.95	1.10	1.25	V
V_{sync}	sync voltage level			1.35	1.5	1.6	V
$V_{clip(u)}$	upper video clipping voltage level			3.5	3.6	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.9	1.0	V
$B_{v(-1dB)}$	–1 dB video bandwidth	AC load: C_L < 20 pF, R_L > 1 kΩ		5	6	-	MHz
$B_{v(-3dB)}$	–3 dB video bandwidth	AC load: C_L < 20 pF, R_L > 1 kΩ		7	8	-	MHz
S/N_W	weighted signal-to-noise ratio	unified weighting filter (*"ITU-T J.61"*); see Figure 13	[7]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[7]	48	52	-	dB

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIF AGC[13]							
$t_{resp(inc)}$	AGC response time to an increasing VIF step	negative modulation; 20 dB	[14]	-	4	-	ms
		positive modulation; 20 dB	[14]	-	2.6	-	ms
$t_{resp(dec)}$	AGC response time to a decreasing VIF step	negative modulation; 20 dB	[14]	-	3	-	ms
		positive modulation; 20 dB	[14]	-	890	-	ms
		L standard; fast mode		-	2.6	-	ms/dB
		L standard; normal mode	[14]	-	143	-	ms/dB
$\Delta V_{i(VIF)}$	VIF amplitude step for activating AGC fast mode	L standard		–2	–6	–10	dB
V_{VAGC}	gain control voltage range	see Figure 9		0.8	-	3.5	V
CR_{stps}	control steepness	definition: $\Delta G_{VIF} / \Delta V_{VAGC}$; V_{VAGC} = 2 V to 3 V		-	–80	-	dB/V
$V_{th(VIF)}$	threshold voltage for high level VIF input	see Table 6 and Table 7		120	200	320	µV
Pin VAGC							
$I_{ch(max)}$	maximum charge current	L standard		-	100	-	µA
$I_{ch(add)}$	additional charge current	L standard: in the event of missing VITS pulses and no white video content		-	100	-	nA
I_{dch}	discharge current	L standard; normal mode		-	35	-	nA
		L standard; fast mode		-	1.8	-	µA
Tuner AGC; pin TAGC; see Figure 9 to Figure 11							
$V_{i(VIF)(start1)(rms)}$	VIF input signal voltage for minimum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 µA; R_{TOP} = 22 kΩ or no R_{TOP} and –15 dB via I²C-bus (see Table 12)		-	2	5	mV
$V_{i(VIF)(start2)(rms)}$	VIF input signal voltage for maximum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 µA; R_{TOP} = 0 Ω or no R_{TOP} and +15 dB via I²C-bus (see Table 12)		45	90	-	mV
QV_{TOP}	tuner takeover point accuracy	I_{TAGC} = 120 µA; R_{TOP} = 10 kΩ or no R_{TOP} and 0 dB via I²C-bus (see Table 12)		7	17	43	mV
$\Delta QV_{TOP}/\Delta T$	takeover point variation with temperature	I_{TAGC} = 120 µA		-	0.03	0.07	dB/K
V_o	permissible output voltage	from external source		-	-	8.8	V
V_{sat}	saturation voltage	I_{TAGC} = 450 µA		-	-	0.5	V
I_{sink}	sink current	no tuner gain reduction; V_{TAGC} = 8.8 V		-	-	0.75	µA
		maximum tuner gain reduction; V_{TAGC} = 1 V		450	600	750	µA

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 % to 80 %		3	5	8	dB
AFC circuit; pin AFC[15][16]; see Figure 12							
$V_{sat(ul)}$	upper limit saturation voltage			V_P – 0.6	V_P – 0.3	-	V
$V_{sat(ll)}$	lower limit saturation voltage			-	0.3	0.6	V
$I_{source(o)}$	output source current			160	200	240	µA
$I_{sink(o)}$	output sink current			160	200	240	µA
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC} / \Delta f_{VIF}$		0.85	1.05	1.25	µA/kHz
$Qf_{VIF(a)}$	analog accuracy of AFC circuit	I_{AFC} = 0 µA; f_{REF} = 4 MHz		–20	-	+20	kHz
$Qf_{VIF(d)}$	digital accuracy of AFC circuit via I²C-bus	I_{AFC} = 0 µA; f_{REF} = 4 MHz; 1 digit = 25 kHz		–20 – 1 digit	-	+20 + 1 digit	kHz
SIF amplifier; pins SIF1 and SIF2							
$V_{i(SIF)(rms)}$	SIF input voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin SIOMAD		-	30	70	µV
		AM mode; –3 dB at AF output pin AUD		-	70	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	FM mode; +1 dB at intercarrier output pin SIOMAD		50	70	-	mV
		AM mode; +1 dB at AF output pin AUD		80	140	-	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)		[2]	-	-	320	mV
$G_{SIF(cr)}$	SIF gain control range	FM and AM mode; see Figure 11		60	66	-	dB
$B_{SIF(-3dB)(ll)}$	lower limit –3 dB SIF bandwidth			-	15	-	MHz
$B_{SIF(-3dB)(ul)}$	upper limit –3 dB SIF bandwidth			-	80	-	MHz
$R_{i(dif)}$	differential input resistance		[3]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[3]	-	3	-	pF
V_I	DC input voltage			-	1.93	-	V
SIF-AGC detector							
t_{resp}	AGC response time to an increasing or decreasing SIF step of 20 dB	FM or AM fast step					
		increasing		-	8	-	ms
		decreasing		-	25	-	ms
		AM slow step					
		increasing		-	80	-	ms
		decreasing		-	250	-	ms

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Single reference QSS intercarrier mixer; pin SIOMAD							
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off		90	140	180	mV
		L standard; without modulation		90	140	180	mV
		intercarrier mode; PC / SC_1 = 20 dB; SC_2 off	[17]	-	75	-	mV
$B_{intc(-3dB)(ul)}$	upper limit −3 dB intercarrier bandwidth			12	15	-	MHz
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics					
		QSS mode		-	2	5	mV
		intercarrier mode		-	2	5	mV
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics					
		QSS mode		-	2	5	mV
		intercarrier mode		-	5	20	mV
α_H	suppression of video signal harmonics	intercarrier mode; f_{video} = 5 MHz		35	40	-	dB
R_o	output resistance		[3]	-	-	30	Ω
V_O	DC output voltage			-	2	-	V
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower		0.90	1.15	-	mA
$I_{sink(o)(max)}$	maximum output sink current	AC		0.6	0.8	-	mA
$I_{source(o)(max)}$	maximum output source current	AC		0.6	0.8	-	mA
$I_{source(o)}$	output source current	DC; MAD2 activated	[18]	0.75	0.93	1.20	mA
FM-PLL demodulator[16][19][20][21][22][23]							
Sound intercarrier output; pin SIOMAD							
$V_{FM(rms)}$	IF intercarrier level for gain controlled operation of FM PLL (RMS value)	corresponding PC / SC ratio at input pins VIF1 and VIF2 is 7 dB to 47 dB		3.2	-	320	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)			-	-	2	mV
$V_{FM(det)(rms)}$	IF intercarrier level for FM carrier detect (RMS value)	see Table 7		-	-	2.3	mV
f_{FM}	sound intercarrier operating FM frequencies	see Table 13	[24]	-	4.5	-	MHz
				-	5.5	-	MHz
				-	6.0	-	MHz
				-	6.5	-	MHz

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Audio output; pin AUD							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	25 kHz FM deviation; 75 µs de-emphasis		400	500	600	mV
		27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
$V_{o(AF)(cl)(rms)}$	AF output clipping level (RMS value)	THD < 1.5 %		1.3	1.4	-	V
$\Delta V_{o(AF)}/\Delta T$	AF output voltage variation with temperature			-	3×10^{-3}	7×10^{-3}	dB/K
THD	total harmonic distortion	25 kHz FM deviation; 50 µs de-emphasis		-	0.15	0.50	%
Δf_{AF}	frequency deviation	THD < 1.5 %	[20]	-	-	±55	kHz
		–6 dB AF output via I²C-bus	[20]	-	-	±110	kHz
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter of Figure 26		80	100	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM PLL only; 27 kHz FM deviation; 50 µs de-emphasis		52	56	-	dB
		black picture; see Figure 21		50	56	-	dB
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics; without de-emphasis		-	-	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		40	46	-	dB
$PSRR_{FM}$	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 8		14	20	-	dB
FM-PLL filter; pin FMPLL							
V_{loop}	DC loop voltage			1.5	-	3.3	V
$I_{source(o)PD(max)}$	maximum phase detector output source current			-	60	-	µA
$I_{sink(o)PD(max)}$	maximum phase detector output sink current			-	60	-	µA
$I_{source(o)(dah)}$	digital acquisition help output source current		[24]	-	55	-	µA
$I_{sink(o)(dah)}$	digital acquisition help output sink current		[24]	-	55	-	µA
$t_{w(dah)}$	digital acquisition help pulse width		[24]	-	16	-	µs
$T_{cy(dah)}$	digital acquisition help cycle time		[24]	-	64	-	µs

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$K_{O(FM)}$	VCO steepness	definition: $\Delta f_{FM} / \Delta V_{FMPLL}$		-	3.3	-	MHz/V
$K_{D(FM)}$	phase detector steepness	definition: $\Delta I_{FMPLL} / \Delta \varphi_{FM}$		-	4	-	µA/rad
Audio amplifier							
De-emphasis network; pin DEEM							
R_o	output resistance	50 µs de-emphasis; see Table 11		4.4	5.0	5.6	kΩ
		75 µs de-emphasis; see Table 11		6.6	7.5	8.4	kΩ
$V_{AF(rms)}$	audio signal (RMS value)	f_{AF} = 400 Hz; V_{AUD} = 500 mV		-	170	-	mV
V_O	DC output voltage			-	2.37	-	V
AF decoupling; pin AFD							
V_{dec}	decoupling voltage (DC)	dependent on f_{FM} intercarrier frequency		1.5	-	3.3	V
I_L	leakage current	$\Delta V_{O(AUD)}$ < ±50 mV		-	-	±25	nA
$I_{ch(max)}$	maximum charge current			1.15	1.50	1.85	µA
$I_{dch(max)}$	maximum discharge current			1.15	1.50	1.85	µA
Audio output; pin AUD							
R_o	output resistance		[3]	-	-	300	Ω
$V_{O(AUD)}$	DC output voltage			-	2.37	-	V
R_L	load resistance	AC-coupled		10	-	-	kΩ
$R_{L(DC)}$	DC load resistance			100	-	-	kΩ
C_L	load capacitance			-	-	1.5	nF
$B_{AF(-3dB)(ul)}$	upper limit –3 dB AF bandwidth of audio amplifier			150	-	-	kHz
$B_{AF(-3dB)(ll)}$	lower limit –3 dB AF bandwidth of audio amplifier		[21]	-	-	20	Hz
α_{mute}	mute attenuation of AF signal	via I²C-bus		70	75	-	dB
ΔV_{jump}	DC jump voltage for switching AF output to mute state or vice versa	activated by digital acquisition help or via I²C-bus mute		-	±50	±150	mV

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM operation[22][25]						
Intercarrier AF performance[26]						
S/N_W	weighted signal-to-noise ratio	PC / SC ratio is 21 dB to 27 dB at pins VIF1 and VIF2				
		black picture	50	56	-	dB
		white picture	45	51	-	dB
		6 kHz sine wave (black-to-white modulation)	40	46	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	35	40	-	dB
Single reference QSS AF performance[27][28]						
$S/N_{W(SC1)}$	weighted signal-to-noise ratio for SC_1	PC / SC_1 ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); *"ITU-R BS.468-4"*	40	-	-	dB
		black picture	53	58	-	dB
		white picture	50	53	-	dB
		6 kHz sine wave (black-to-white modulation)	44	48	-	dB
		250 kHz square wave (black-to-white modulation)	40	45	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz	45	51	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz	46	52	-	dB

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$S/N_{W(SC2)}$	weighted signal-to-noise ratio for SC_2	PC / SC_2 ratio at pins VIF1 and VIF2; 27 kHz (54 % FM deviation); *"ITU-R BS.468-4"*		40	-	-	dB
		black picture		48	55	-	dB
		white picture		46	51	-	dB
		6 kHz sine wave (black-to-white modulation)		42	46	-	dB
		250 kHz square wave (black-to-white modulation)		29	34	-	dB
		sound carrier subharmonics; f = 2.75 MHz ± 3 kHz		44	50	-	dB
		sound carrier subharmonics; f = 2.87 MHz ± 3 kHz		45	51	-	dB
AM operation							
L standard; pin AUD[29]; see Figure 22 and Figure 23							
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	54 % AM modulation		400	500	600	mV
THD	total harmonic distortion	54 % AM modulation		-	0.5	1.0	%
$B_{AF(-3dB)}$	−3 dB AF bandwidth			100	125	-	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	in accordance with *"ITU-R BS.468-4"*		45	50	-	dB
$V_{O(AUD)}$	DC potential voltage			-	2.37	-	V
$PSRR_{AM}$	power supply ripple rejection	see Figure 8		20	26	-	dB
Reference frequency input; pin REF							
V_I	DC input voltage			2.3	2.6	2.9	V
R_i	input resistance		[3]	-	5	-	kΩ
R_{xtal}	resonance resistance of crystal	operation as crystal oscillator		-	-	200	Ω
C_x	pull-up/down capacitance		[30]	-	-	-	pF
f_{ref}	reference signal frequency		[31]	-	4	-	MHz
Δf_{ref}	tolerance of reference signal frequency		[16]	-	-	±0.1	%
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal		80	-	400	mV
$R_{o(ref)}$	output resistance of reference signal source			-	-	4.7	kΩ
C_K	decoupling capacitance to external reference signal source	operation as input terminal		22	100	-	pF

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Table 20. Characteristics *...continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C-bus transceiver; pins SDA and SCL[32][33]						
f_{SCL}	SCL clock frequency		0	-	400	kHz
V_{IH}	HIGH-level input voltage		3	-	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	-	+1.5	V
I_{IH}	HIGH-level input current		–10	-	+10	µA
I_{IL}	LOW-level input current		–10	-	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
$I_{sink(o)}$	output sink current	V_P = 0 V	-	-	10	µA
$I_{source(o)}$	output source current	V_P = 0 V	-	-	10	µA
Output ports; pins OP1 and OP2[34]						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA (sink current)	-	-	0.4	V
V_{OH}	HIGH-level output voltage		-	-	6	V
$I_{sink(o)}$	output sink current		-	-	2	mA
$I_{o(max)}$	maximum output current	sink or source; pin OP2 functions as VIF-AGC output	-	-	10	µA

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] Level headroom for input level jumps during gain control setting.

[3] This parameter is not tested during the production and is only given as application information for designing the receiver circuit.

[4] Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formula:

$$BL_{-3dB} = \frac{1}{2\pi} K_O K_D R \text{, valid for d} \geq 1.2$$

$$d = \frac{1}{2} R \sqrt{K_O K_D C},$$

where:

K_O is the VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{\mu A}{rad}\right)$;

R is the loop resistor (Ω); C is the loop capacitor (F); BL_{-3dB} is the loop bandwidth for –3 dB (Hz); d is the damping factor.

[5] $V_{i(VIF)}$ = 10 mV (RMS); Δf = 1 MHz (VCO frequency offset related to the picture carrier frequency); white picture video modulation.

[6] Condition: luminance range (5 steps) from 0 % to 100 %.

[7] S/N is the ratio of black-to-white amplitude to the noise voltage (RMS value measured on pin CVBS and tested at video black level, 'quiet line'). Noise analyzer settings: B = 5 MHz, 200 kHz high-pass and sound carrier trap on. In case of S/N_W weighted in accordance with *"ITU-T J.61"*. Measurements taken for B/G standard.

[8] The intermodulation figures are defined for:

a) f = 1.1 MHz (referenced to black and white signal) as $\alpha_{IM} = 20\ log\left(\frac{V_0\ at\ 4.4\ MHz}{V_0\ at\ 1.1\ MHz}\right) + 3.6\ dB$

b) f = 3.3 MHz (referenced to color carrier) as $\alpha_{IM} = 20\ log\left(\frac{V_0\ at\ 4.4\ MHz}{V_0\ at\ 3.3\ MHz}\right)$

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[9] Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz. Modulation VSB; sound carrier off; f_{video} > 0.5 MHz.

[10] Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz. Sound carrier on; f_{video} = 10 kHz to 10 MHz.

[11] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figure 15 to Figure 20; |H (s)| is the absolute value of transfer function).

[12] The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).

[13] If selected by the I²C-bus, the VIF-AGC voltage can be monitored at pin OP2, and pin OP1 can be used as input. In this case, both pins cannot be used for the normal port function.

[14] The response time is valid for a VIF input level range from 200 µV to 70 mV.

[15] To match the AFC output signal to different tuning systems a current output is provided. The test circuit is given in Figure 12. The AFC slope (voltage per frequency) can be changed by resistors R1 and R2.

[16] The tolerance of the reference frequency determines the accuracy of the VIF AFC, FM demodulator center frequency and maximum FM deviation.

[17] The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference: $V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^{r}\ V$ and $r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}}\ (dB) + 6\ dB \pm 3\ dB\right)$, where: $\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}\ (dB)$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

[18] For normal operation (with the I²C-bus) no DC load at pin SIOMAD is allowed. The second module address (MAD2) will be activated by the application of a 2.2 kΩ resistor between pin SIOMAD and ground. If this MAD2 is activated, also the power-on set-up state activates a VIF frequency of 58.75 MHz.

[19] SIF input level is 10 mV (RMS); VIF input level is 10 mV (RMS) unmodulated.

[20] Measured with an FM deviation of 25 kHz and the typical AF output voltage of 500 mV (RMS). The AF output signal can be attenuated by 6 dB to 250 mV (RMS) via the I²C-bus. For handling a frequency deviation of more than 55 kHz, the AF output signal has to be reduced in order to avoid clipping (THD < 1.5 %).

[21] The lower limit of the audio bandwidth depends on the value of the capacitor at pin AFD. A value of C_{AF} = 470 nF leads to $f_{AF(-3dB)} \approx$ 20 Hz and C_{AF} = 220 nF leads to $f_{AF(-3dB)} \approx$ 40 Hz.

[22] For all S/N measurements the VIF modulator in use has to meet the following specifications:

a) Incidental phase modulation for black-to-white jump less than 0.5 degrees

b) QSS AF performance, measured with the television demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (at deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation

c) Picture-to-sound carrier ratio PC / SC_1 = 13 dB (transmitter)

[23] Calculation of the loop filter parameters can be done approximately using the following formulae: $f_o = \frac{1}{2\pi}\sqrt{\frac{K_O K_D}{C_P}}$; $\vartheta = \frac{1}{2R\sqrt{K_O K_D C_P}}$; $BL_{-3dB} = f_o(1.55 - \vartheta^2)$. The formulae are only valid under the following conditions: $\vartheta \leq 1$ and $C_S > 5C_P$, where: K_O is the VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{\mu A}{rad}\right)$; R is the loop resistor; C_S is the series capacitor; C_P is the parallel capacitor; f_o is the natural frequency of the PLL; BL_{-3dB} is the loop bandwidth for –3 dB; ϑ is the damping factor. For examples, see Table 21.

[24] Window width of digital acquisition help ≤ 237.5 kHz.

[25] The PC / SC ratio is calculated as the addition of TV transmitter PC / SC_1 ratio and SAW filter PC / SC_1 ratio. This PC / SC ratio is necessary to achieve the S/N_W values as noted. A different PC / SC ratio will change these values.

[26] Measurements taken with SAW filter G1984 (Siemens) for vision and sound IF (sound shelf: 14 dB). Picture-to-sound carrier ratio of transmitter PC / SC = 13 dB. Input level on pins VIF1 and VIF2 of $V_{i(SIF)}$ = 10 mV (RMS) sync level, 27 kHz FM deviation for sound carrier, f_{AF} = 400 Hz. Measurements in accordance with *"ITU-R BS.468-4"*. De-emphasis is 50 µs.

[27] The QSS signal output on pin SIOMAD is analyzed by a test demodulator TDA9820. The S/N ratio of this device is more than 60 dB, related to a deviation of ±27 kHz, in accordance with *"ITU-R BS.468-4"*.

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[28] Measurements taken with SAW filter K3953 for vision IF (suppressed sound carrier) and K9453 for sound IF (suppressed picture carrier). Input level $V_{i(SIF)}$ = 10 mV (RMS), 27 kHz (54 % FM deviation).

[29] Measurements taken with SAW filter K9453 (Siemens) for AM sound IF (suppressed picture carrier).

[30] The value of C_x determines the accuracy of the resonance frequency of the crystal. It depends on the type of crystal used.

[31] Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

[32] The SDA and SCL lines will not be pulled down if V_{CC} is switched off.

[33] The AC characteristics are in accordance with the I²C-bus specification for fast mode (maximum clock frequency is 400 kHz). Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

[34] Port P1 and port P2 are open-collector outputs.

Table 21. Examples to the FM-PLL filter

BL_{-3dB} (kHz)	C_S (nF)	C_P (pF)	R (kΩ)	ϑ
100	10	390	5.6	0.5
160	10	150	9.1	0.5

Table 22. Input frequencies and carrier ratios

Symbol	Parameter	B/G standard	M/N standard	L standard	L-accent standard	Unit
f_{PC}	picture carrier frequency	38.9	45.75 or 58.75	38.9	33.9	MHz
f_{SC1}	sound carrier frequency 1	33.4	41.25 or 54.25	32.4	40.4	MHz
f_{SC2}	sound carrier frequency 2	33.158	-	-	-	MHz
PC / SC_1	picture to first sound carrier ratio	13	7	10	10	dB
PC / SC_2	picture to second sound carrier ratio	20	-	-	-	dB

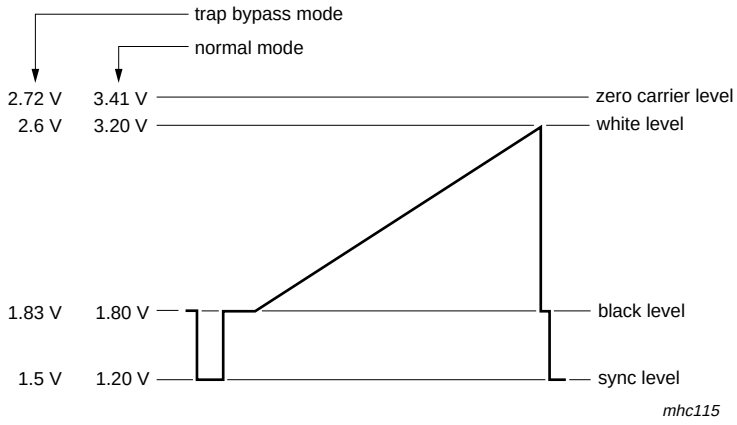

Fig 7. Typical video signal levels on output pin CVBS (sound carrier off)

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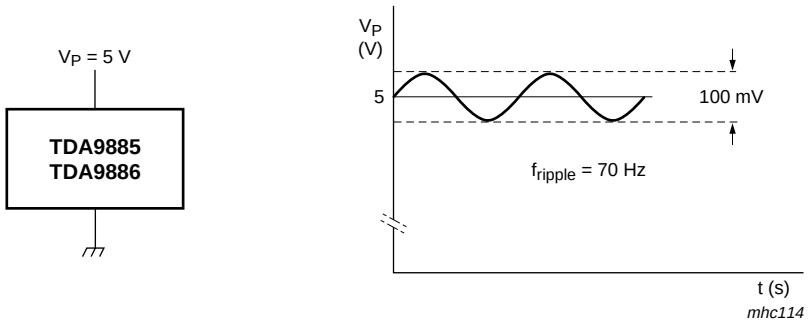
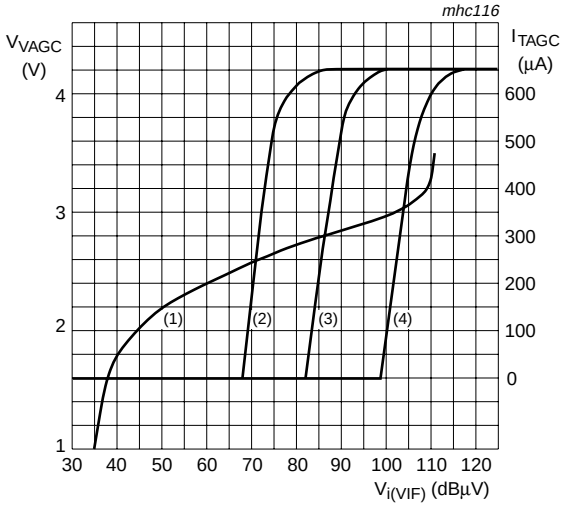


Fig 8. Ripple rejection condition



(1) V_{VAGC} is VIF-AGC voltage and can only be measured at pin OP2 controlled by the I²C-bus (see Table 14).

(2) I_{TAGC} is tuner current in TV mode with R_{TOP} = 22 kΩ or setting via I²C-bus at –15 dB.

(3) I_{TAGC} is tuner current in TV mode with R_{TOP} = 10 kΩ or setting via I²C-bus at 0 dB.

(4) I_{TAGC} is tuner current in TV mode with R_{TOP} = 0 kΩ or setting via I²C-bus at +15 dB.

Fig 9. Typical VIF and tuner AGC characteristic

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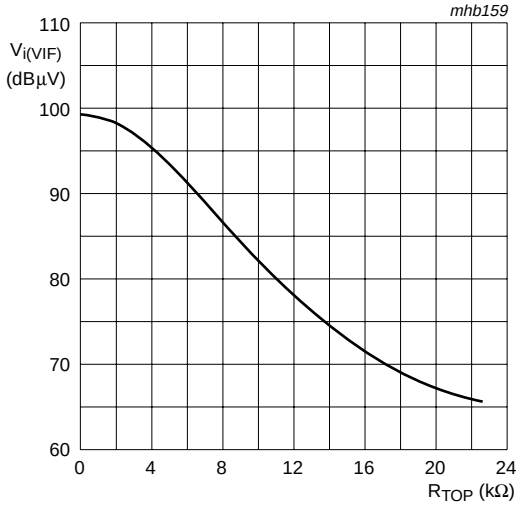
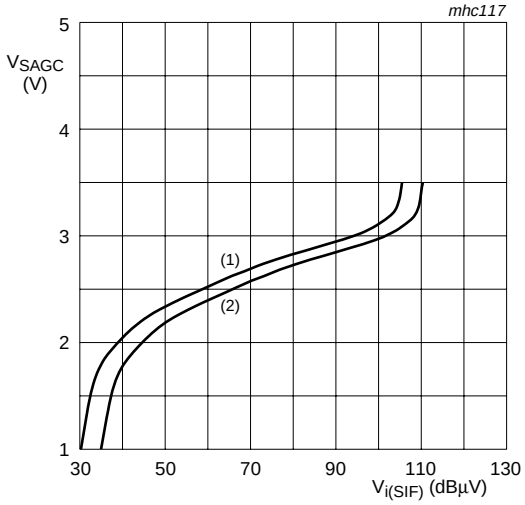


Fig 10. Typical tuner takeover point as a function of resistor R_{TOP}



(1) FM mode.

(2) AM mode.

Fig 11. Typical SIF-AGC characteristic

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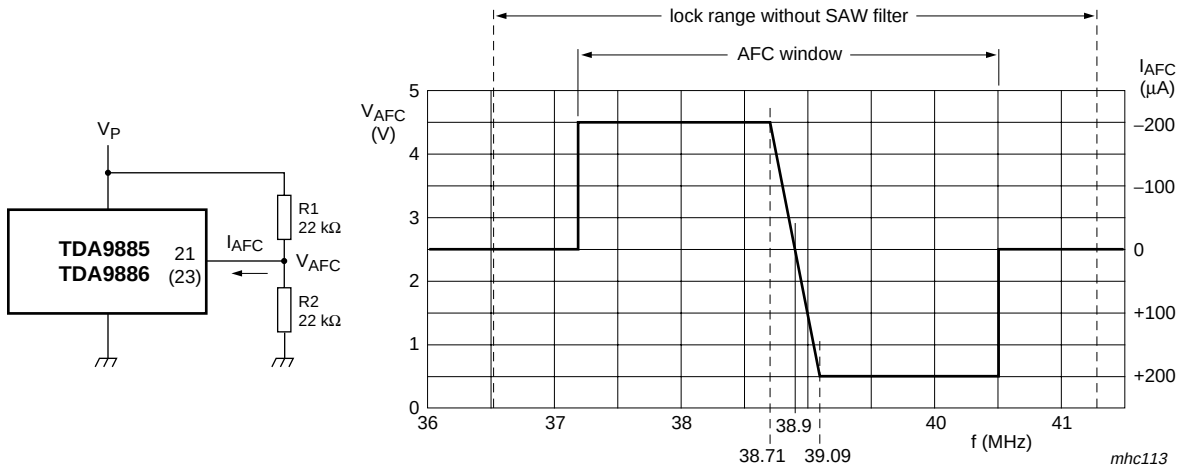


Pin numbers for TDA9885HN and TDA9886HN in parentheses.

Fig 12. Typical analog AFC characteristic

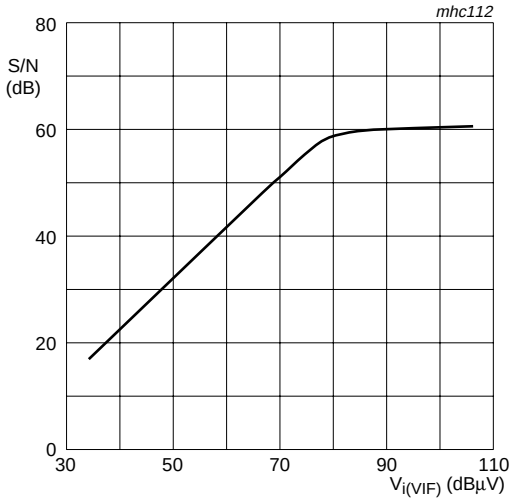
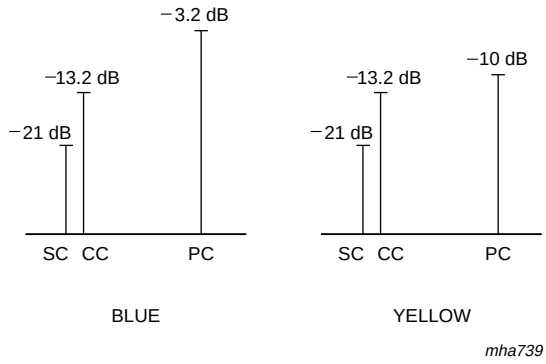


Fig 13. Typical signal-to-noise ratio as a function of VIF input voltage



SC is sound carrier, with respect to sync level.

CC is chrominance carrier, with respect to sync level.

PC is picture carrier, with respect to sync level.

The sound carrier level takes into account a sound shelf attenuation of 14 dB (SAW filter G1984M).

Fig 14. Input signal conditions

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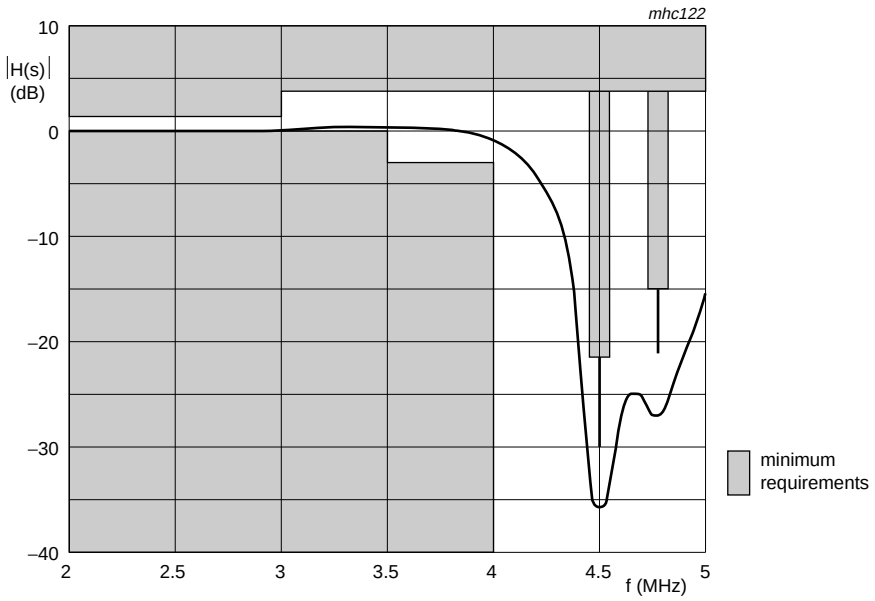
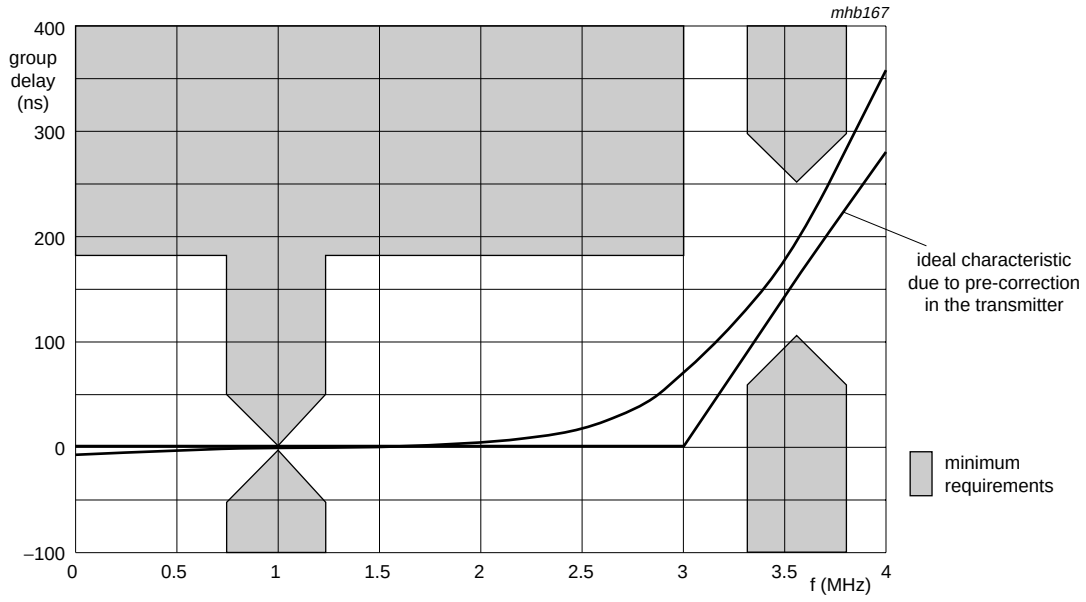


Fig 15. Typical amplitude response for sound trap at M/N standard (including Korea)



Overall delay is not shown, here the maximum ripple is specified.

Fig 16. Typical group delay for sound trap at M/N standard

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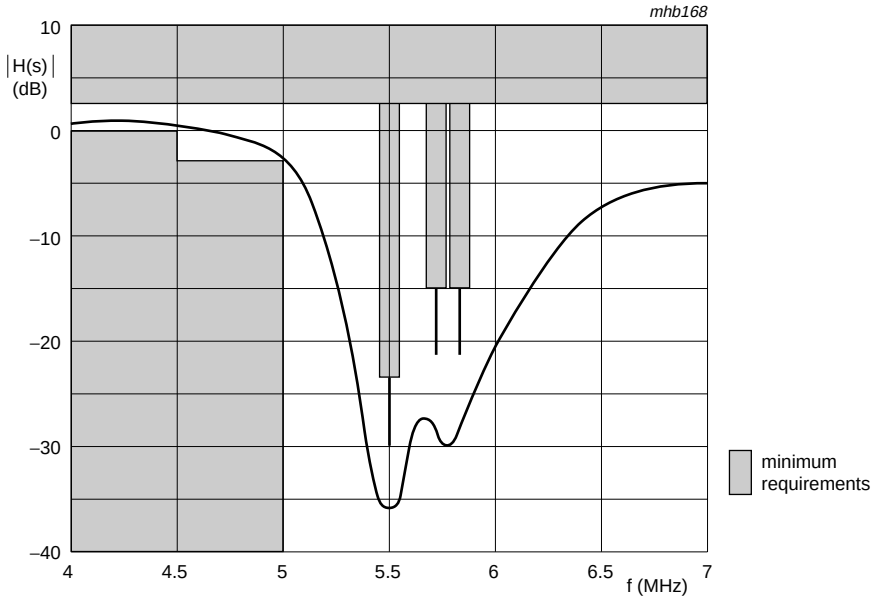
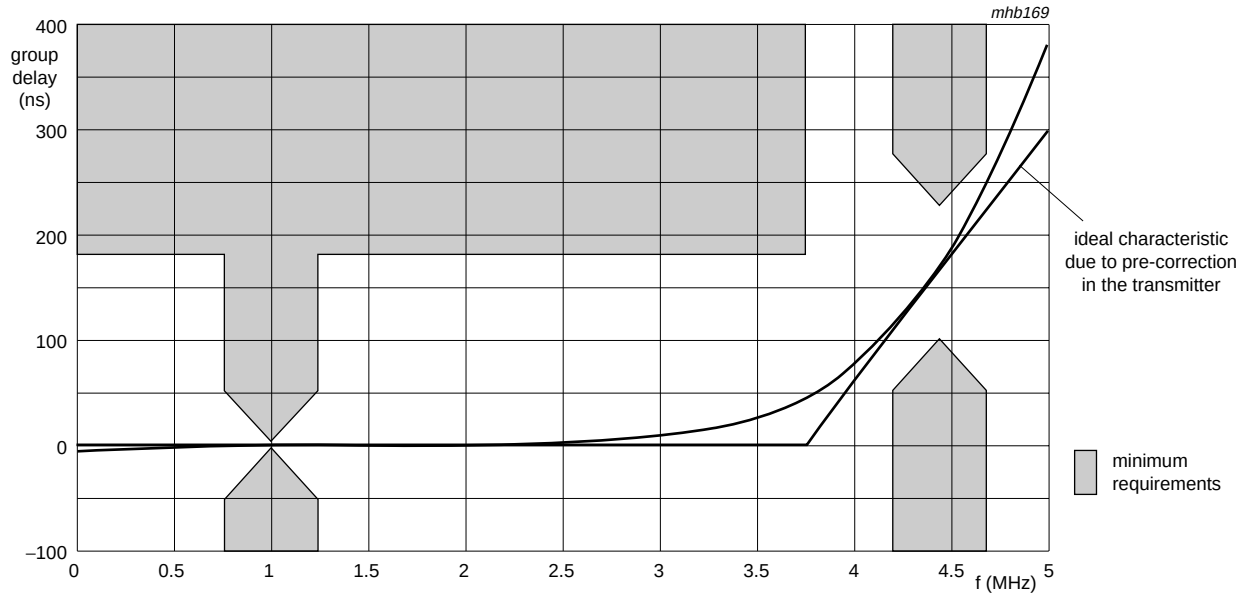


Fig 17. Typical amplitude response for sound trap at B/G standard



Overall delay is not shown, here the maximum ripple is specified.

Fig 18. Typical group delay for sound trap at B/G standard

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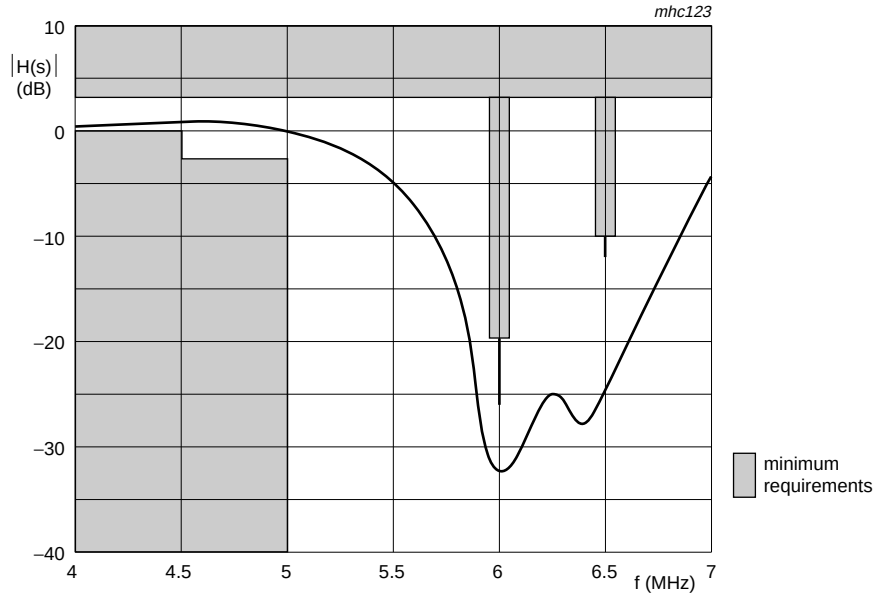

Fig 19. Typical amplitude response for sound trap at I standard

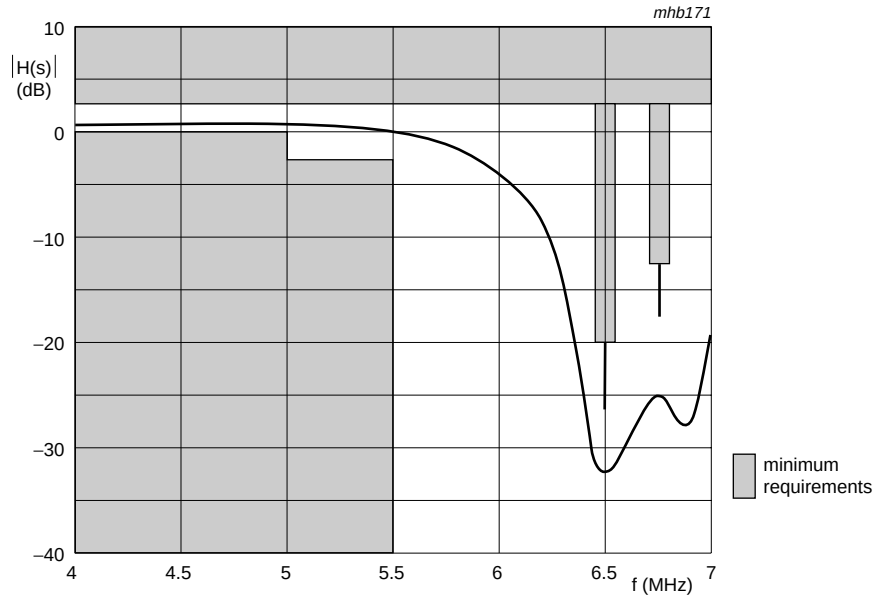

Fig 20. Typical amplitude response for sound trap at D/K standard

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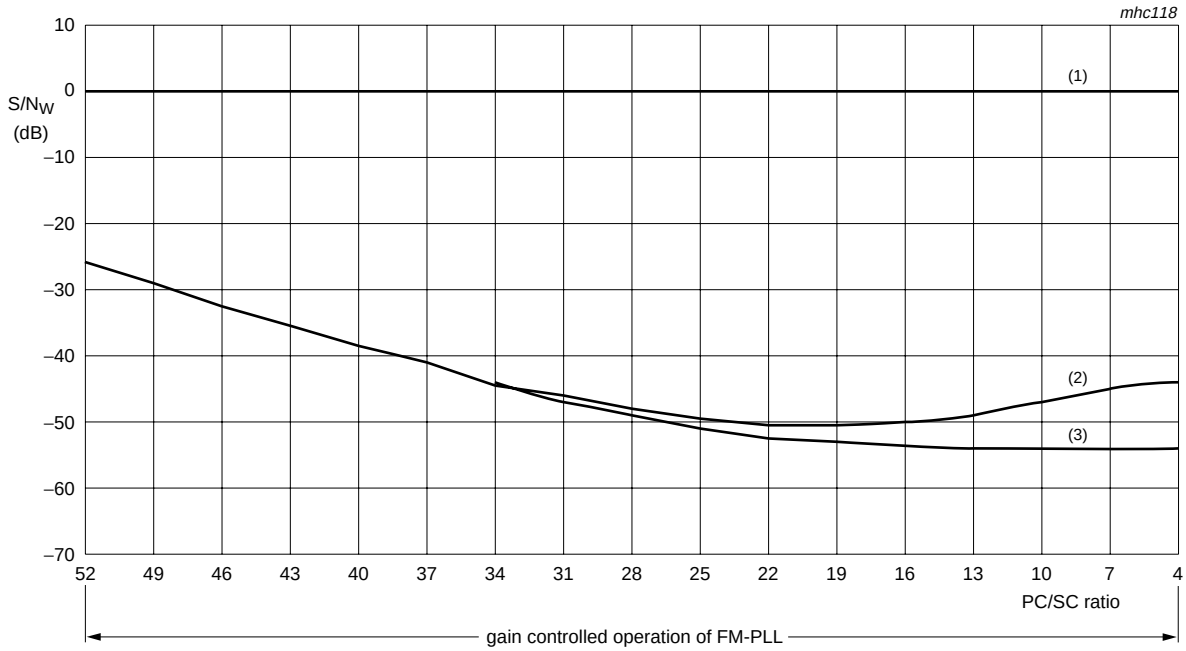


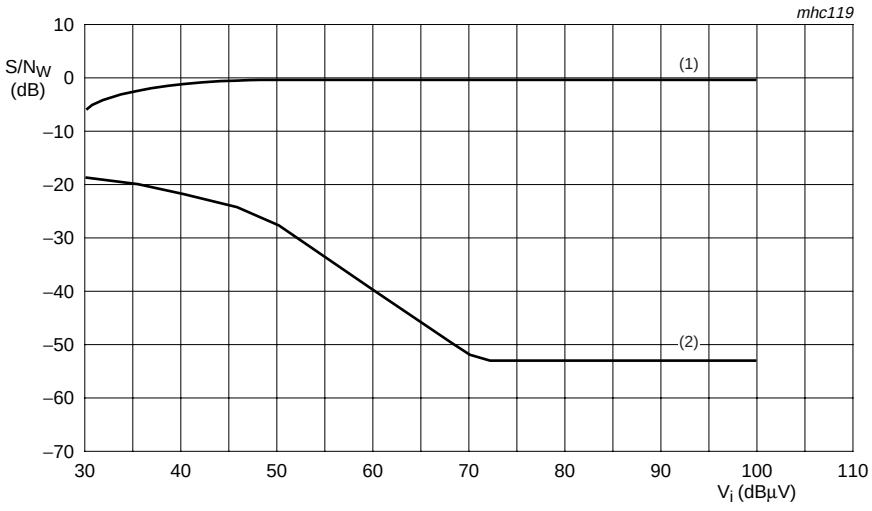
Conditions: PC / SC ratio measured at pins VIF1 and VIF2; via transformer; 27 kHz FM deviation; 50 µs de-emphasis.

(1) Signal.

(2) Noise at H-picture (*"ITU-R BS.468-4"* weighted quasi peak).

(3) Noise at black picture (*"ITU-R BS.468-4"* weighted quasi peak).

Fig 21. Audio signal-to-noise ratio as a function of picture-to-sound carrier ratio in intercarrier mode



Condition: m = 54 %.

(1) Signal.

(2) Noise.

Fig 22. Typical audio signal-to-noise ratio as a function of input signal at AM standard

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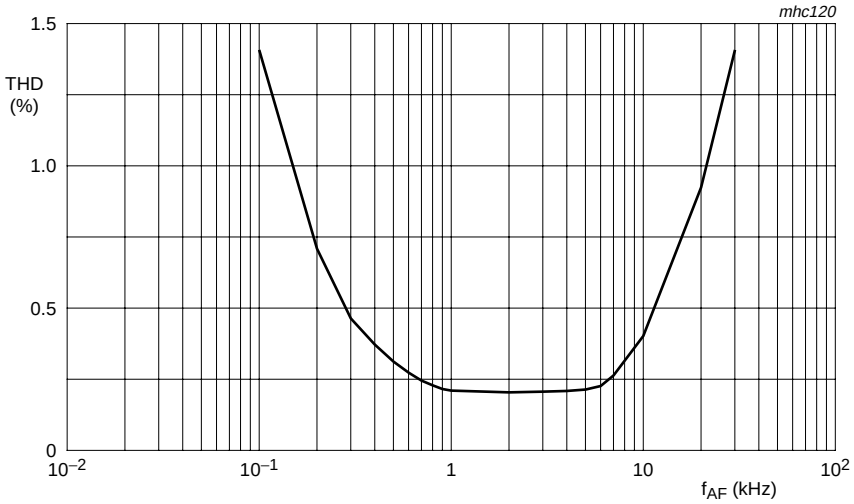

C_{AGC} = 2.2 µF; m = 54 %.

Fig 23. Typical total harmonic distortion as a function of audio frequency at AM standard

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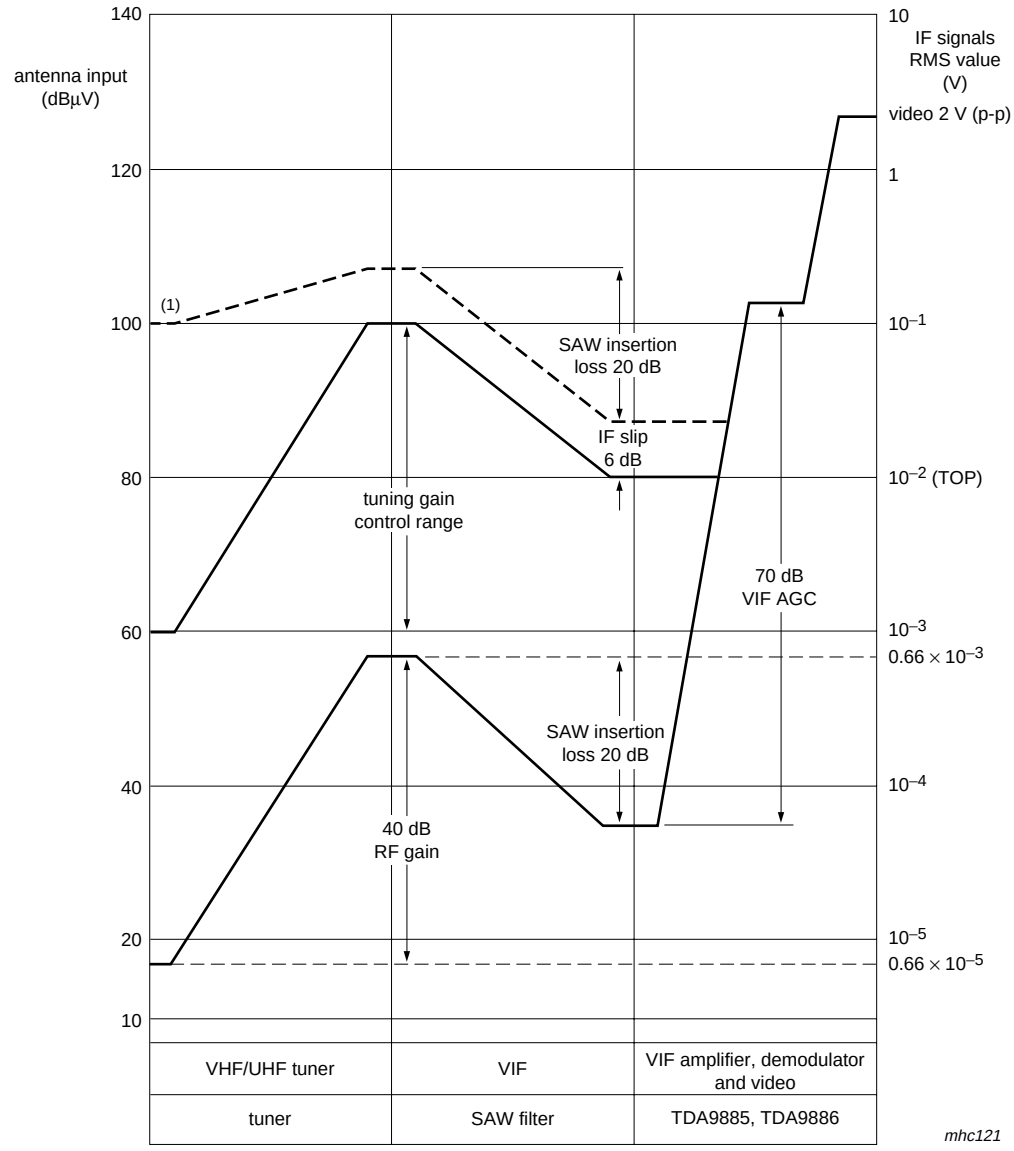

(1) Depends on TOP.

Fig 24. Front-end level diagram

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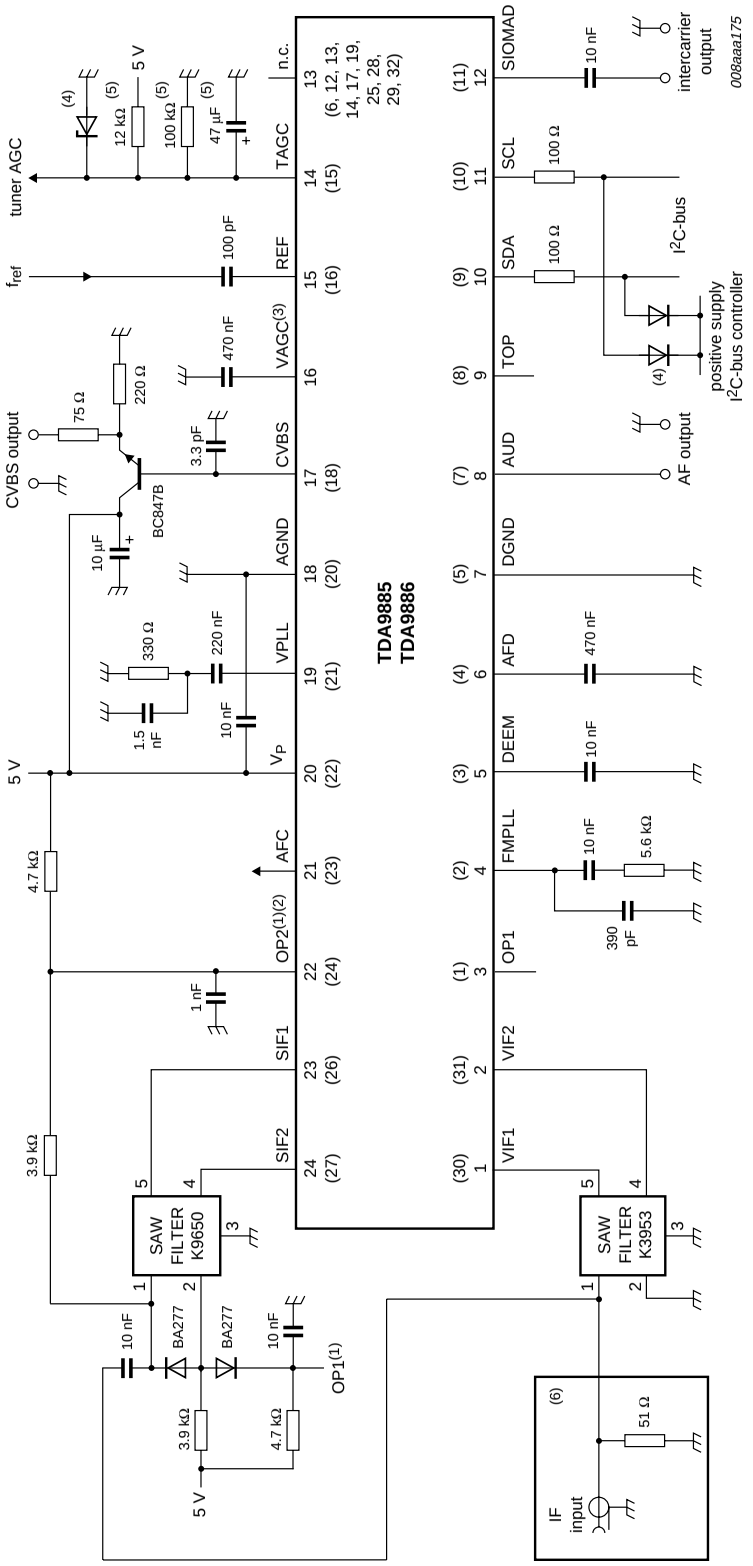
13. Application information



Pin numbers for TDA9885HN and TDA9886HN in parentheses.

(1) For L-accent standard OP1 = LOW and OP2 = HIGH, in other cases OP1 = HIGH and OP2 = LOW.

(2) If pin OP2 outputs VIF-AGC voltage, then pin OP1 can be used for SAW switching.

(3) Not connected for TDA9885.

(4) Optional measures to improve ESD performance within a TV-set application.

(5) Application dependent.

(6) For test signal input only.

Fig 25. Application diagram

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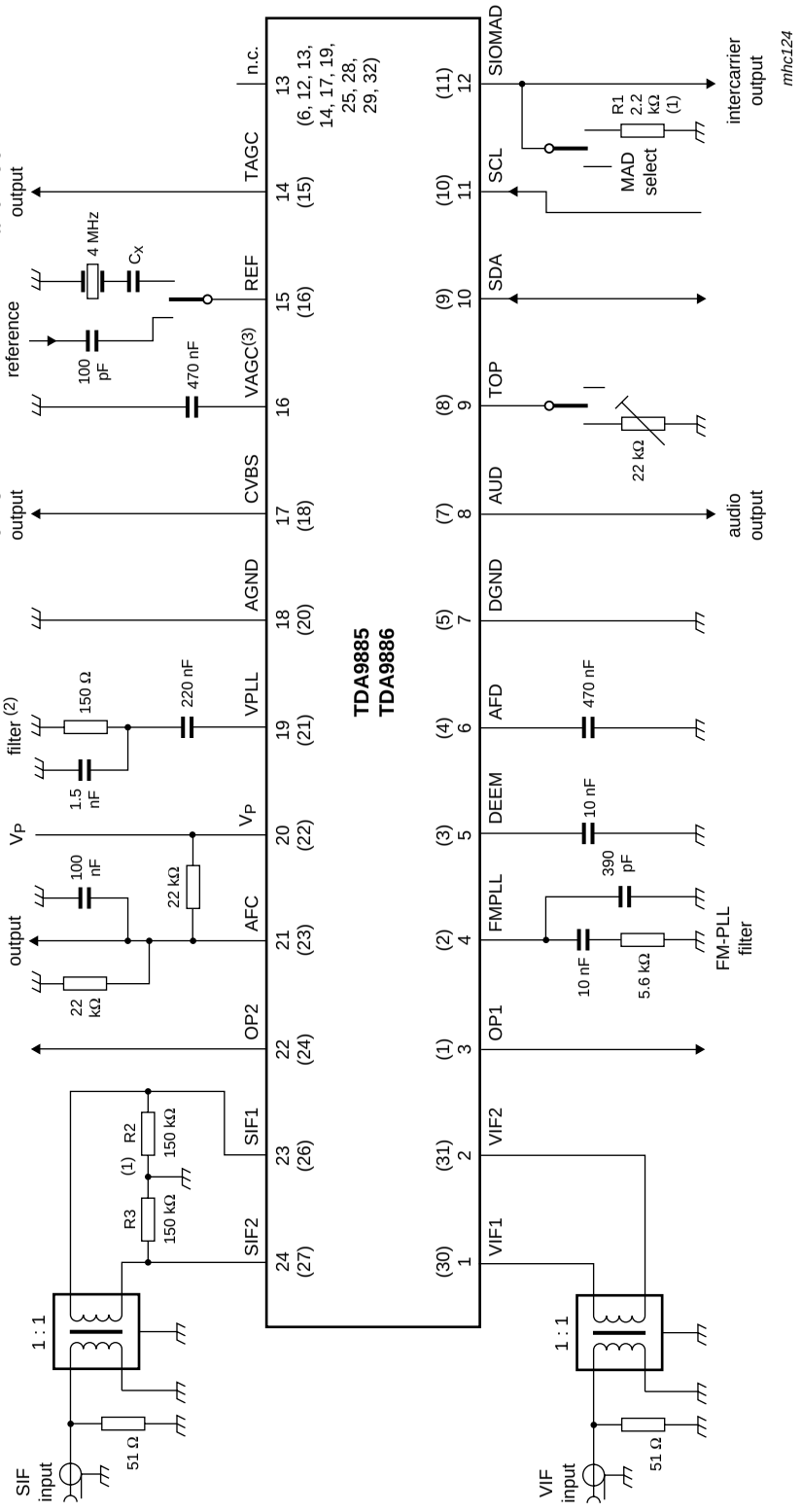
14. Test information



Pin numbers for TDA9885HN and TDA9886HN in parentheses.

(1) Optional for I²C-bus address selection; see Table 23.

(2) Different VIF loop filter in comparison with the application diagram due to different input characteristics (SAW filter or transformer).

(3) Not connected for TDA9885.

Fig 26. Test circuit

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Table 23. I²C-bus address selection

S = R/$\overline{W}$ selection bit.

Option	R1 not used	R1 = 2.2 kΩ
R2 and R3 not used	1000 011S	1000 010S
R2 = R3 = 150 kΩ	1001 011S	1001 010S

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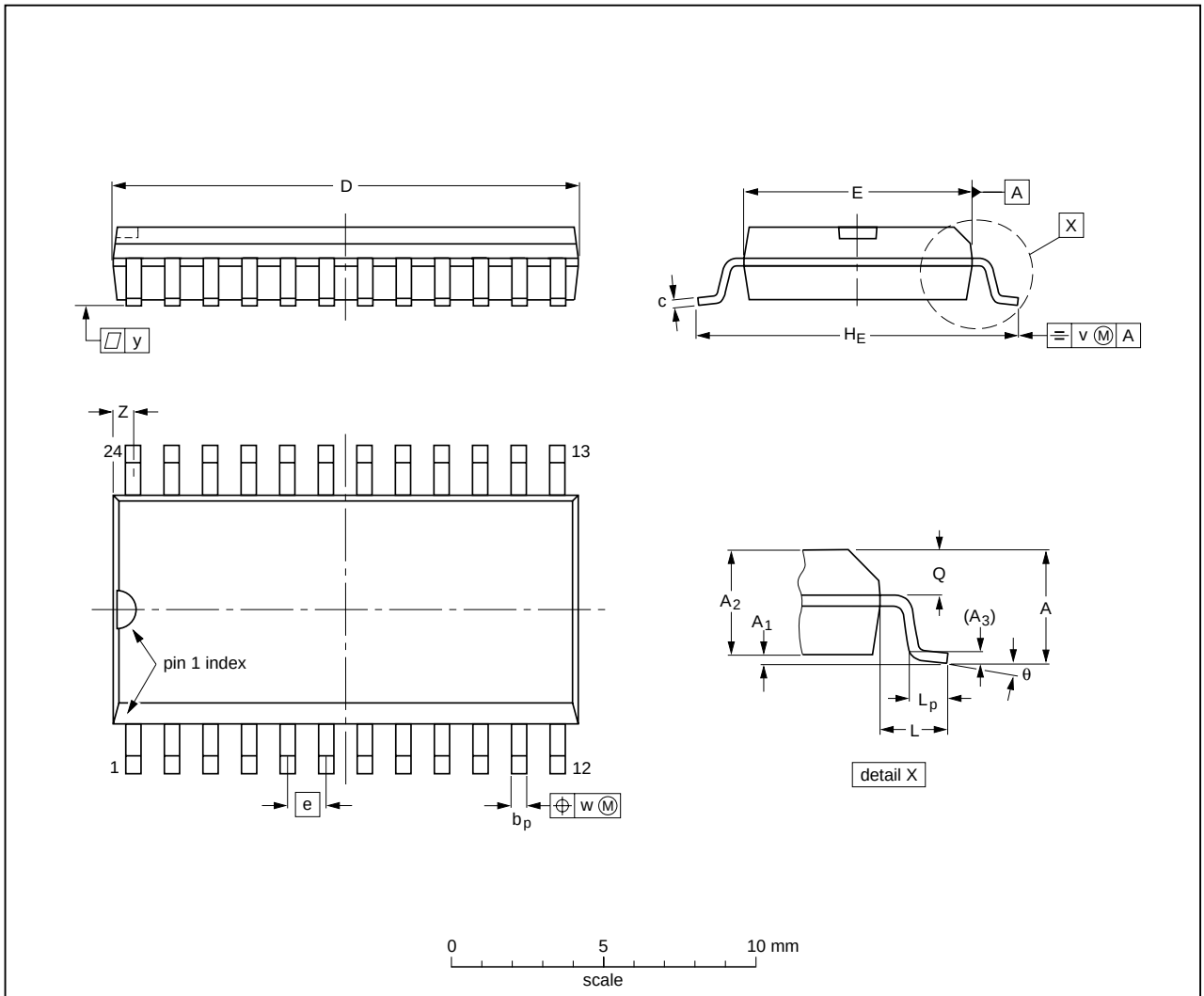
15. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 27. Package outline SOT137-1 (SO24)

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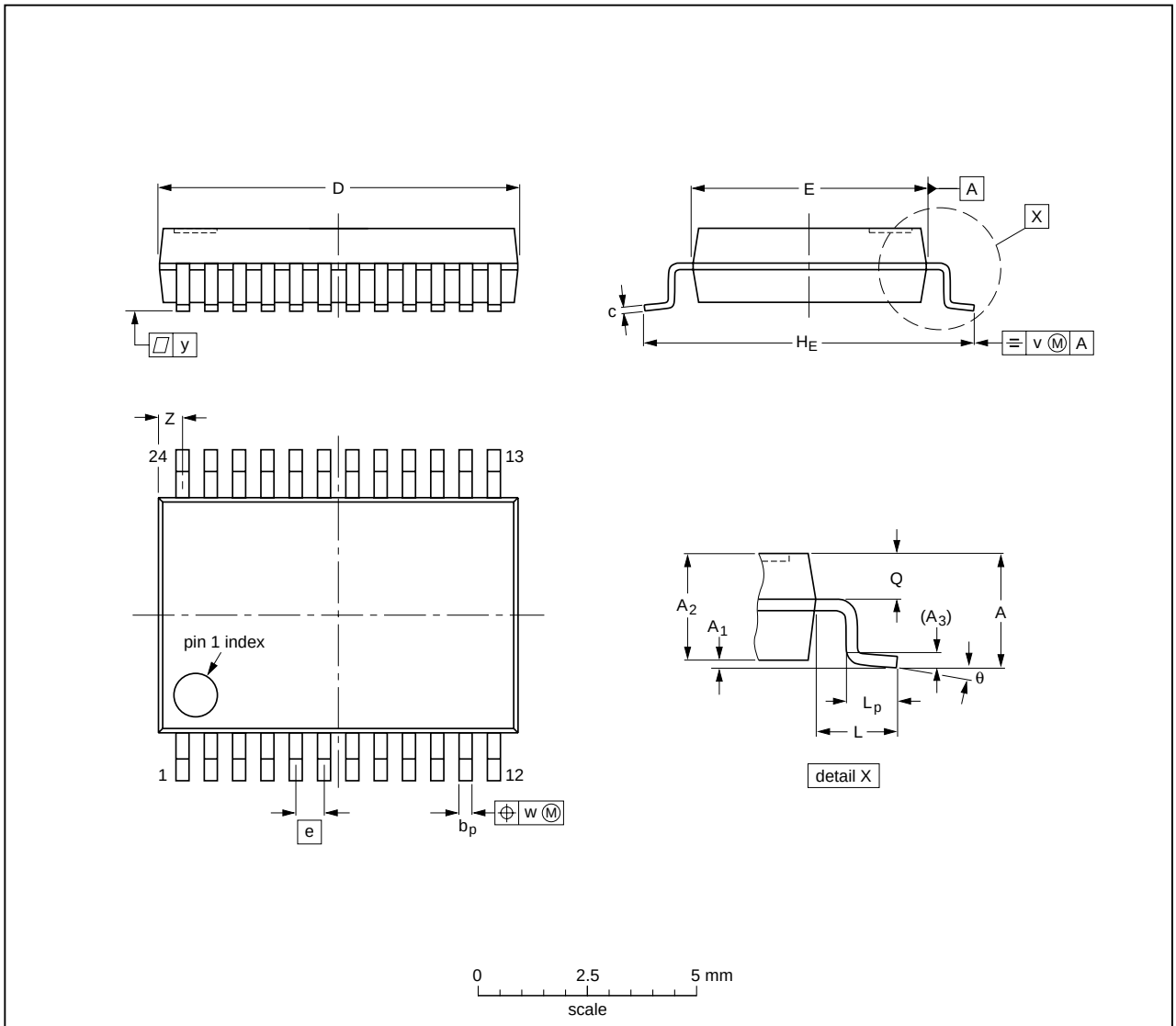
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 28. Package outline SOT340-1 (SSOP24)

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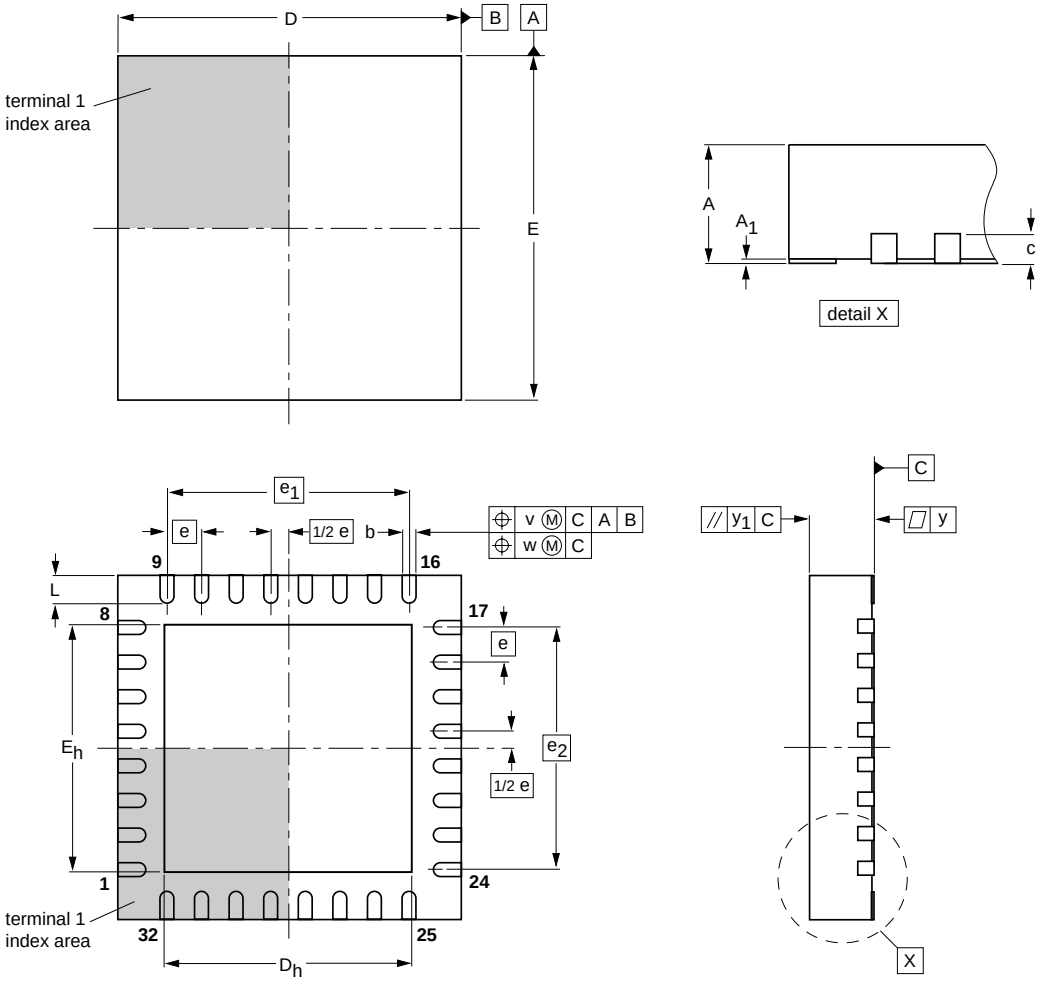
HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-3	- - -	MO-220	- - -			~~02-04-18~~ 02-10-22

Fig 29. Package outline SOT617-3 (HVQFN32)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 30) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 24 and 25

Table 24. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 25. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 30.

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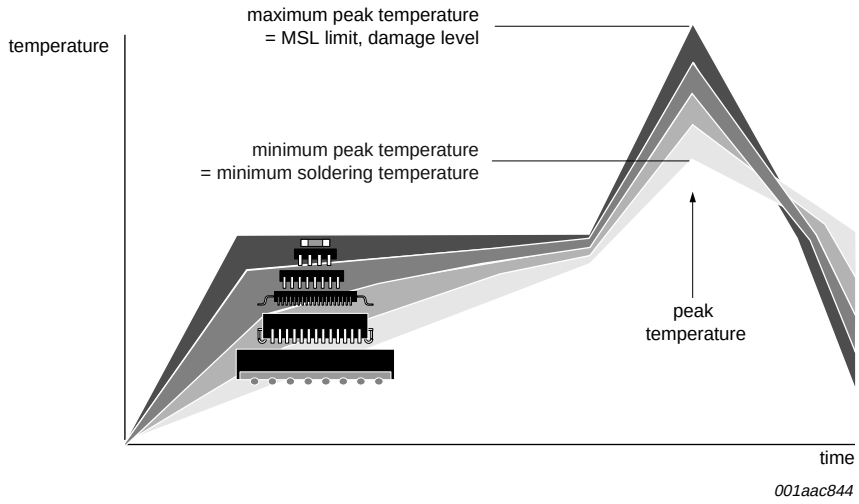

MSL: Moisture Sensitivity Level

Fig 30. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 26. Abbreviations

Acronym	Description
AF	Audio Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
DSB	Double SideBand
FPLL	Frequency Phase-Locked Loop
IF	Intermediate Frequency
MAD	Module ADdress
NTSC	National Television Standards Committee
PAL	Phase Alternating Line
PC	Personal Computer
PC	Picture Carrier
PLL	Phase-Locked Loop
QSS	Quasi Split Sound
SAD	SubADdress
SAW	Surface Acoustic Wave
SC	Sound Carrier
SECAM	SEquentiel Couleur Avec Memoire
SIF	Sound Intermediate Frequency
STB	Set-Top Box

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Table 26. Abbreviations *...continued*

Acronym	Description
TOP	TakeOver Point
VCO	Voltage-Controlled Oscillator
VIF	Vision Intermediate Frequency
VITS	Vertical Interval Test Signal
VTR	Video Tape Recorder

18. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9885_TDA9886_3	20081216	Product data sheet	-	TDA9885_TDA9886_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 5: added V5 versions • Figure 25; update on application diagram			
TDA9885_TDA9886_2	20031002	Product specification	-	TDA9885_TDA9886_1
TDA9885_TDA9886_1	20020305	Product specification	-	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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