

# FOD3184

## 3A Output Current, High Speed MOSFET/IGBT Gate Driver Optocoupler

### Features

- High noise immunity characterized by 50kV/μs (Typ.) common mode rejection @  $V_{CM} = 2,000V$
- Guaranteed operating temperature range of -40°C to +100°C
- 3A peak output current for medium power MOSFET/IGBT
- Fast switching speed
  - 210ns max. propagation delay
  - 65ns max pulse width distortion
- Fast output rise/fall time
  - Offers lower dynamic power dissipation
- 250kHz maximum switching speed
- Wide  $V_{DD}$  operating range from 15V to 30V
- Use of P-Channel MOSFETs at output stage enables output voltage swing close to the supply rail (rail-to-rail output)
- Under voltage lockout protection (UVLO) with hysteresis – optimized for driving IGBTs
- Safety and regulatory approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 min.
  - DIN EN/IEC 60747-5-2, 1,414 peak working insulation voltage
    - Minimum creepage distance of 8.0mm
    - Minimum clearance distance of 8mm to 16mm (option TV or TSV)
    - Minimum insulation thickness of 0.5mm

### Applications

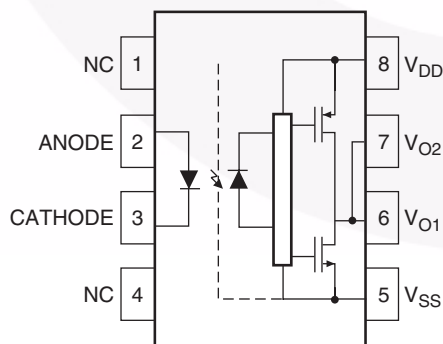
- Plasma Display Panel
- High performance DC/DC convertor
- High performance switch mode power supply
- High performance uninterruptible power supply
- Isolated Power MOSFET/IGBT gate drive

### Description

The FOD3184 is a 3A Output Current, High Speed MOSFET/IGBT Gate Drive Optocoupler. It consists of a aluminium gallium arsenide (AlGaAs) light emitting diode optically coupled to a CMOS detector with PMOS and NMOS output power transistors integrated circuit power stage. It is ideally suited for high frequency driving of power MOSFETs/IGBT used in Plasma Display Panels (PDPs), motor control inverter applications and high performance DC/DC converters.

The device is packaged in an 8-pin dual in-line housing compatible with 260°C reflow processes for lead free solder compliance.

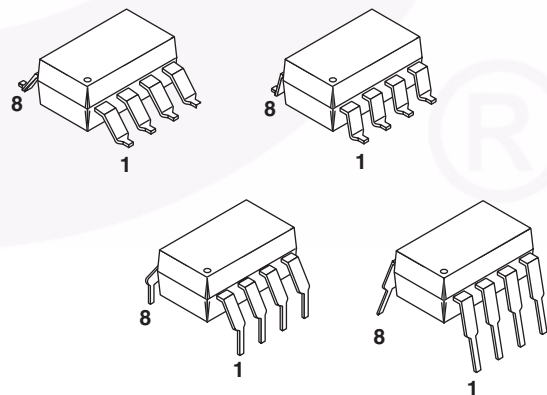
### Functional Block Diagram



**Note:**

A 0.1μF bypass capacitor must be connected between pins 5 and 8.

### Package Outlines



**Truth Table**

LED	$V_{DD}-V_{SS}$ "Positive Going" (Turn-on)	$V_{DD}-V_{SS}$ "Negative Going" (Turn-off)	$V_O$
Off	0V to 30V	0V to 30V	Low
On	0V to 11.5V	0V to 10V	Low
On	11.5V to 13.5V	10V to 12V	Transition
On	13.5V to 30V	12V to 30V	High

**Pin Definitions**

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	$V_{SS}$	Negative Supply Voltage
6	$V_{O2}$	Output Voltage 2 (internally connected to $V_{O1}$ )
7	$V_{O1}$	Output Voltage 1
8	$V_{DD}$	Positive Supply Voltage

## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-2. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150Vrms		I-IV		
	For Rated Mains Voltage < 300Vrms		I-IV		
	For Rated Mains Voltage < 450Vrms		I-III		
	For Rated Mains Voltage < 600Vrms		I-III		
	For Rated Mains Voltage < 1000Vrms (Option T, TS)		I-III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
$V_{PR}$	Input to Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec., Partial Discharge < 5pC	2651			
	Input to Output Test Voltage, Method a, $V_{IORM} \times 1.5 = V_{PR}$ , Type and Sample Test with $t_m = 60$ sec., Partial Discharge < 5 pC	2121			
$V_{IORM}$	Max Working Insulation Voltage	1,414			$V_{peak}$
$V_{IOTM}$	Highest Allowable Over Voltage	6000			$V_{peak}$
	External Creepage	8			mm
	External Clearance	7.4			mm
	External Clearance (for Option T or TS - 0.4" Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
$T_{Case}$	Case Temperature	150			°C
$I_{S,INPUT}$	Input Current	25			mA
$P_{S,OUTPUT}$	Output Power	250			mW
$R_{IO}$	Insulation Resistance at $T_S$ , $V_{IO} = 500V$	$10^9$			$\Omega$

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$T_{OPR}$	Operating Temperature	-40 to +100	$^\circ\text{C}$
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{SOL}$	Lead Solder Temperature – Wave solder (Refer to Reflow Temperature Profile, pg. 22)	260 for 10 sec.	$^\circ\text{C}$
$I_{F(AVG)}$	Average Input Current <sup>(1)</sup>	25	mA
$I_{F(tr, tf)}$	LED Current Minimum Rate of Rise/Fall	250	ns
$V_R$	Reverse Input Voltage	5	V
$I_{OH(PEAK)}$	“High” Peak Output Current <sup>(2)</sup>	3	A
$I_{OL(PEAK)}$	“Low” Peak Output Current <sup>(2)</sup>	3	A
$V_{DD} - V_{SS}$	Supply Voltage	-0.5 to 35	V
$V_{O(PEAK)}$	Output Voltage	0 to $V_{DD}$	V
$P_O$	Output Power Dissipation <sup>(3)</sup>	250	mW
$P_D$	Total Power Dissipation <sup>(3)</sup>	295	mW

**Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Value	Units
$V_{DD} - V_{SS}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	10 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	-3.0 to 0.8	V

## Electrical-Optical Characteristics (DC)

Apply over all recommended conditions, typical value is measured at  $V_{DD} = 30V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{OH}$	High Level Output Current	$V_{OH} = (V_{DD} - V_{SS} - 1V)$		-0.9	-0.5	A
		$V_{OH} = (V_{DD} - V_{SS} - 6V)$			-2.5	
$I_{OL}$	Low Level Output Current	$V_{OL} = (V_{DD} - V_{SS} + 1V)$	0.5	1		A
		$V_{OL} = (V_{DD} - V_{SS} + 6V)$	2.5			
$V_{OH}$	High Level Output Voltage <sup>(4)(5)</sup>	$I_O = -100mA$ , $I_F = 10mA$	$V_{DD} - 0.5$			V
		$I_O = -2.5A$ , $I_F = 10mA$	$V_{DD} - 7$			
$V_{OL}$	Low Level Output Voltage <sup>(4)(5)</sup>	$I_O = 100mA$ , $I_F = 0mA$			$V_{SS} + 0.5$	V
		$I_O = 2.5A$ , $I_F = 0mA$			$V_{SS} + 7$	
$I_{DDH}$	High Level Supply Current	Output Open, $I_F = 10$ to $16mA$		2.6	3.5	mA
$I_{DDL}$	Low Level Supply Current	Output Open, $V_F = -3.0$ to $0.8V$		2.5	3.5	mA
$I_{FLH}$	Threshold Input Current Low to High	$I_O = 0mA$ , $V_O > 5V$		3.0	7.5	mA
$V_{FHL}$	Threshold Input Voltage High to Low	$I_O = 0mA$ , $V_O < 5V$	0.8			V
$V_F$	Input Forward Voltage	$I_F = 10mA$	1.1	1.43	1.8	V
$\Delta V_F / T_A$	Temperature Coefficient of Forward Voltage	$I_F = 10mA$		-1.5		mV/°C
$V_{UVLO+}$	UVLO Threshold	$V_O > 5V$ , $I_F = 10mA$	11.5	13.0	13.5	V
$V_{UVLO-}$		$V_O < 5V$ , $I_F = 10mA$	10.0	11.5	12.0	V
$UVLO_{HYST}$	UVLO Hysteresis			1.5		V
$BV_R$	Input Reverse Breakdown Voltage	$I_R = 10\mu A$	5			V
$C_{IN}$	Input Capacitance	$f = 1MHz$ , $V_F = 0V$		25		pF

## Switching Characteristics

Apply over all recommended conditions, typical value is measured at  $V_{DD} = 30V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
$t_{PLH}$	Propagation Delay Time to High Output Level <sup>(6)</sup>	$I_F = 10mA$ , $R_g = 10\Omega$ , $f = 250kHz$ , Duty Cycle = 50%, $C_g = 10nF$	50	120	210	ns
$t_{PHL}$	Propagation Delay Time to Low Output Level <sup>(6)</sup>		50	145	210	ns
$P_{WD}$	Pulse Width Distortion <sup>(7)</sup>		35	65	ns	
$P_{DD}$ ( $t_{PHL} - t_{PLH}$ )	Propagation Delay Difference Between Any Two Parts <sup>(8)</sup>		-90		90	ns
$t_r$	Rise Time	$C_L = 10nF$ , $R_g = 10\Omega$		38		ns
$t_f$	Fall Time			24		ns
$t_{UVLO\ ON}$	UVLO Turn On Delay			2.0		$\mu s$
$t_{UVLO\ OFF}$	UVLO Turn Off Delay			0.3		$\mu s$
$ CM_H $	Output High Level Common Mode Transient Immunity <sup>(9) (10)</sup>	$T_A = +25^\circ C$ , $I_f = 10mA$ to $16mA$ , $V_{CM} = 2kV$ , $V_{DD} = 30V$	35	50		kV/ $\mu s$
$ CM_L $	Output Low Level Common Mode Transient Immunity <sup>(9) (11)</sup>	$T_A = +25^\circ C$ , $V_f = 0V$ , $V_{CM} = 2kV$ , $V_{DD} = 30V$	35	50		kV/ $\mu s$

\*Typical values at  $T_A = 25^\circ C$

## Isolation Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
$V_{ISO}$	Withstand Isolation Voltage <sup>(12) (13)</sup>	$T_A = 25^\circ C$ , R.H. < 50%, $t = 1min.$ , $I_{I-O} \leq 10\mu A$	5000			$V_{rms}$
$R_{I-O}$	Resistance (input to output) <sup>(13)</sup>	$V_{I-O} = 500V$		$10^{11}$		$\Omega$
$C_{I-O}$	Capacitance (input to output)	Freq. = 1MHz		1		pF

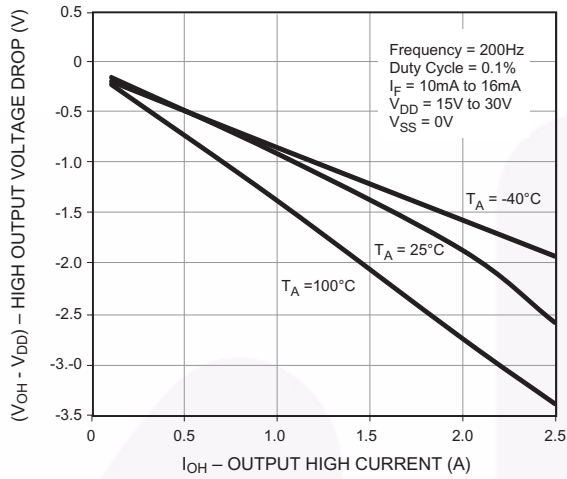
\*Typical values at  $T_A = 25^\circ C$

**Notes:**

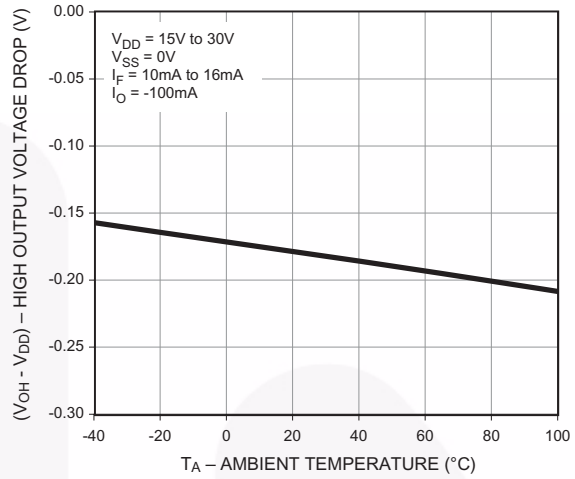
1. Derate linearly above +79°C free air temperature at a rate of 0.37mA/°C.
2. Maximum pulse width = 10μs.
3. Derate linearly above +79°C, free air temperature at the rate of 5.73mW/°C.
4. In this test,  $V_{OH}$  is measured with a dc load current of 100mA. When driving capacitive load  $V_{OH}$  will approach  $V_{DD}$  as  $I_{OH}$  approaches zero amps.
5. Maximum pulse width = 1ms, maximum duty cycle = 20%.
6.  $t_{PHL}$  propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the  $V_O$  signal.
7. PWD is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
8. The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two FOD3184 parts under same operating conditions, with equal loads.
9. Pin 1 and 4 need to be connected to LED common.
10. Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse  $V_{CM}$  to assure that the output will remain in the high state (i.e.  $V_O > 15V$ ).
11. Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (i.e.  $V_O < 1.0V$ ).
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000Vrms, 60Hz for 1 second (leakage detection current limit  $I_{L-O} < 10\mu A$ ).
13. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.

## Typical Performance Curves

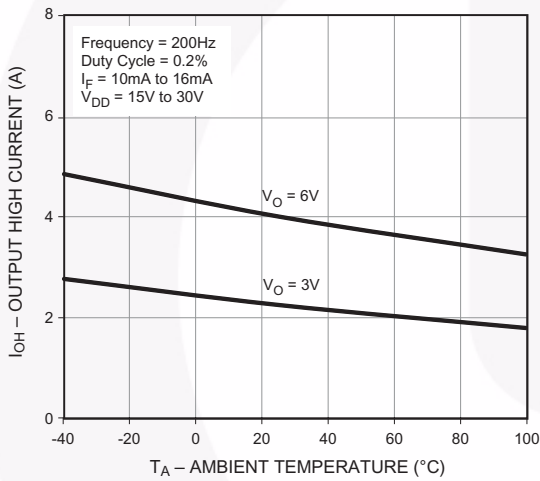
**Fig. 1 Output High Voltage Drop vs. Output High Current**



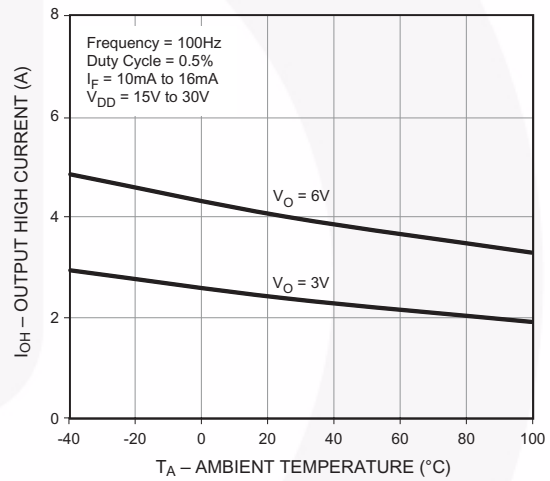
**Fig. 2 Output High Voltage Drop vs. Ambient Temperature**



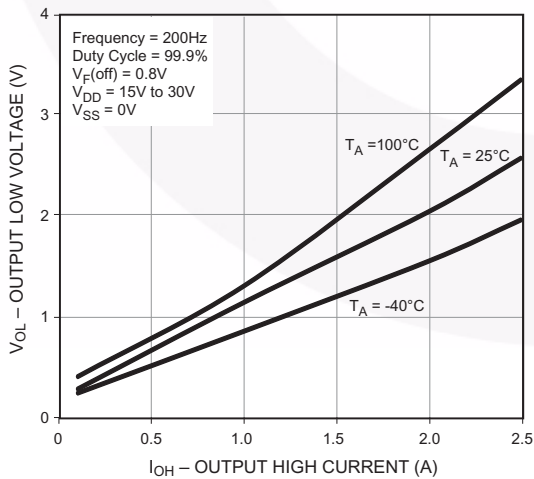
**Fig. 3 Output High Current vs. Ambient Temperature**



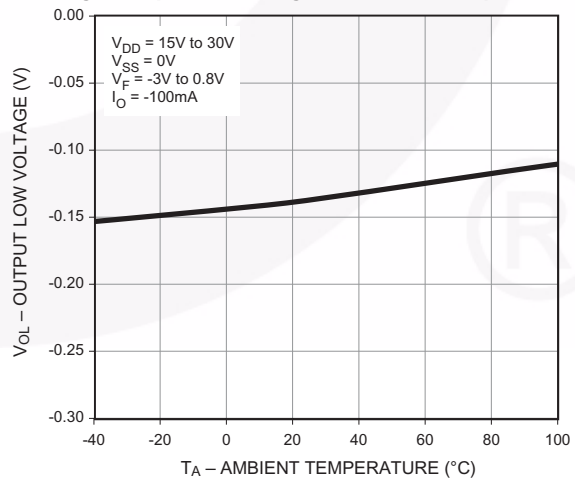
**Fig. 4 Output High Current vs. Ambient Temperature**



**Fig. 5 Output Low Voltage vs. Output High Current**



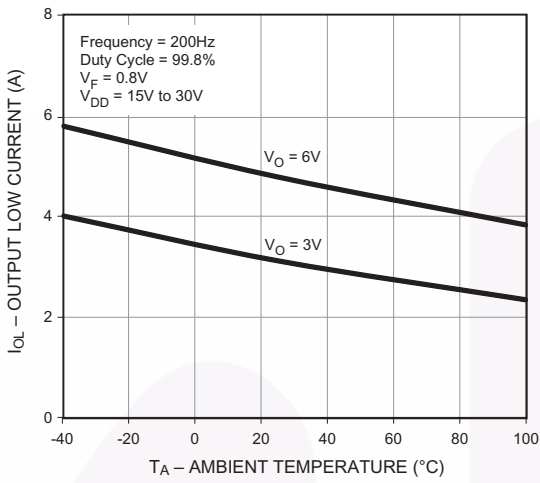
**Fig. 6 Output Low Voltage vs. Ambient Temperature**



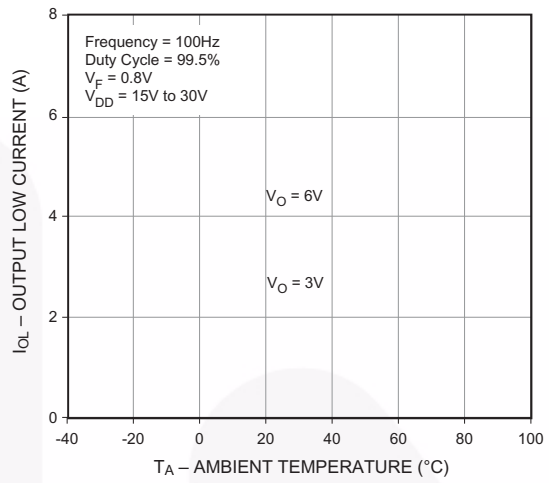


## Typical Performance Curves (Continued)

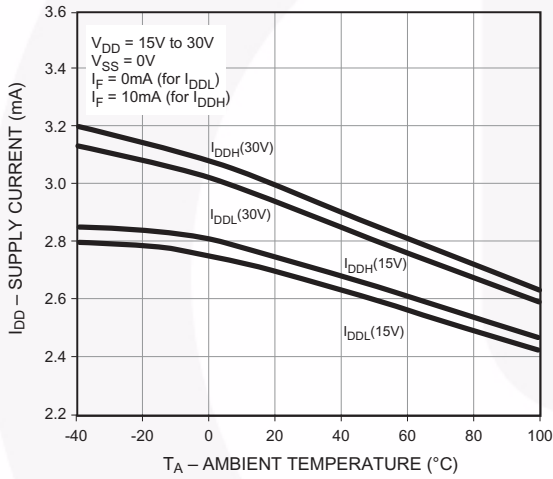
**Fig. 7 Output Low Current vs. Ambient Temperature**



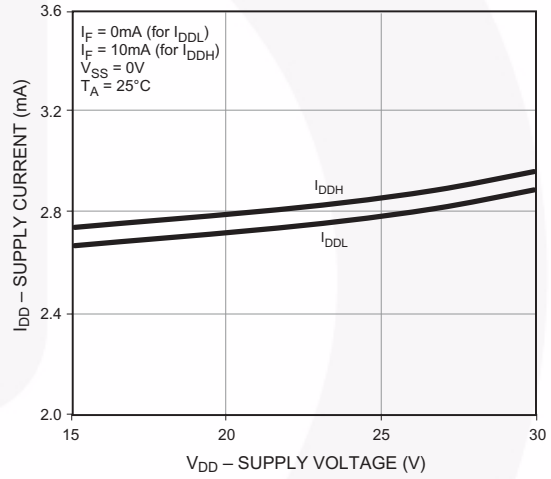
**Fig. 8 Output Low Current vs. Ambient Temperature**



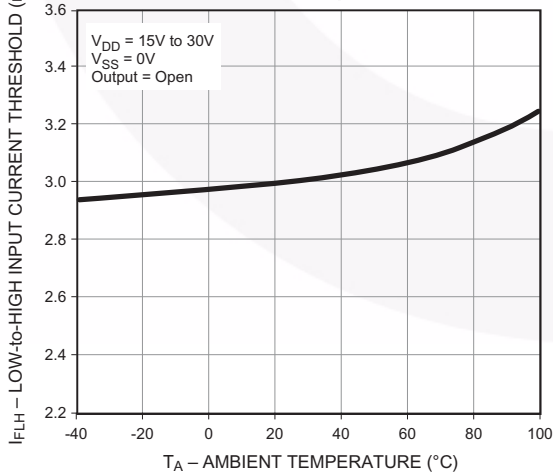
**Fig. 9 Supply Current vs. Ambient Temperature**



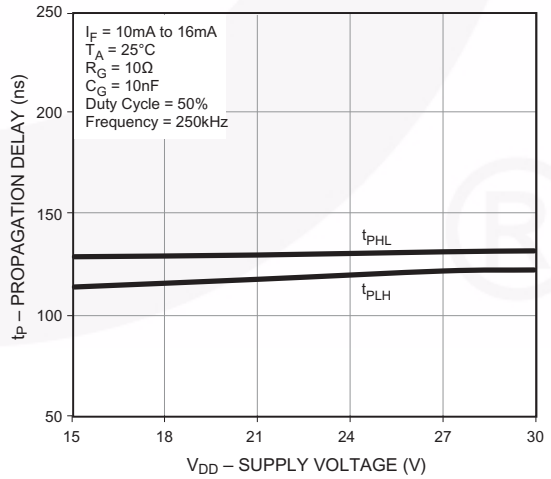
**Fig. 10 Supply Current vs. Supply Voltage**



**Fig. 11 Low-to-High Input Current Threshold vs. Ambient Temperature**

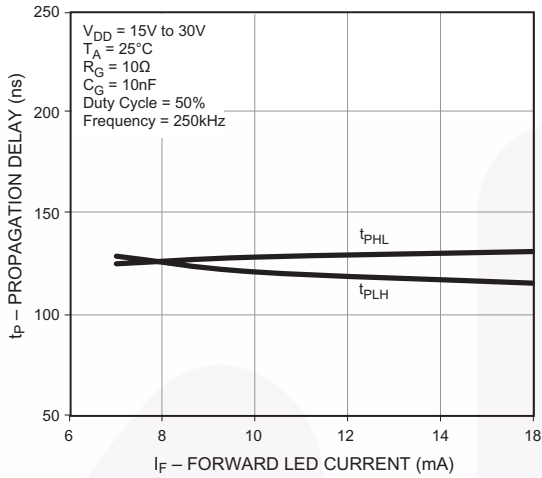


**Fig. 12 Propagation Delay vs. Supply Voltage**

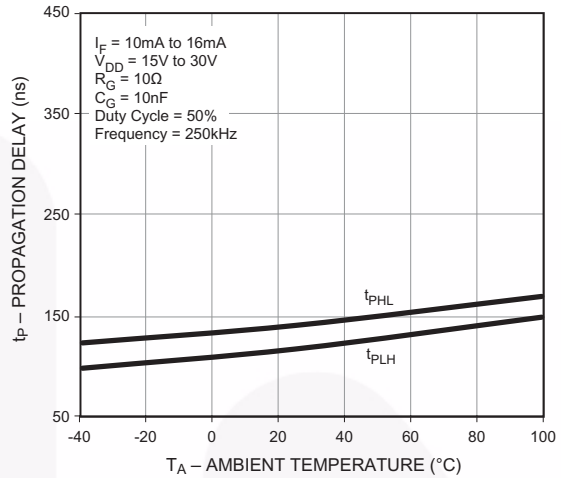


## Typical Performance Curves (Continued)

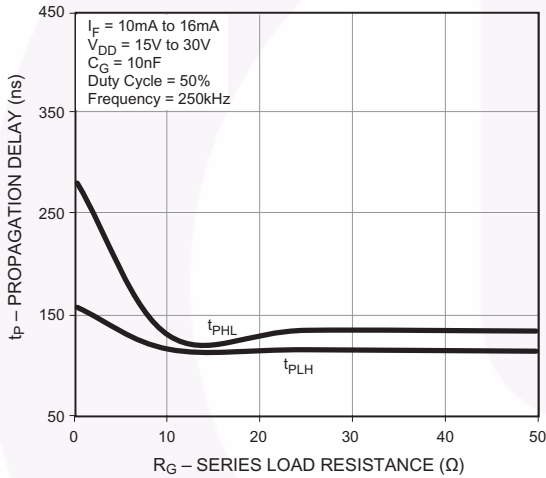
**Fig. 13 Propagation Delay vs. LED Forward Current**



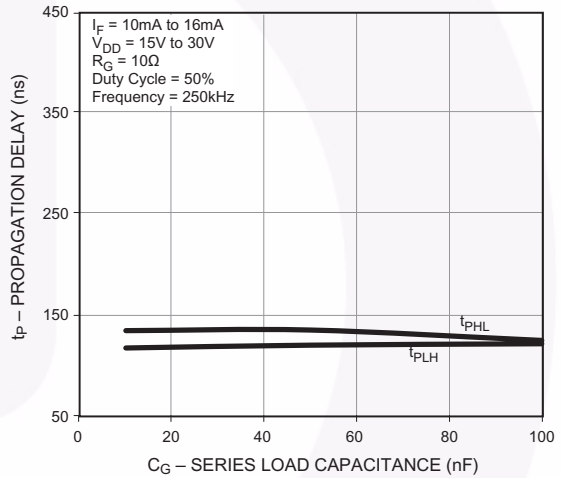
**Fig. 14 Propagation Delay vs. Ambient Temperature**



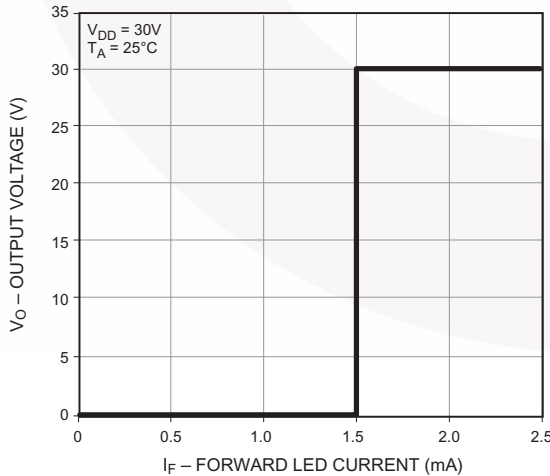
**Fig. 15 Propagation Delay vs. Series Load Resistance**



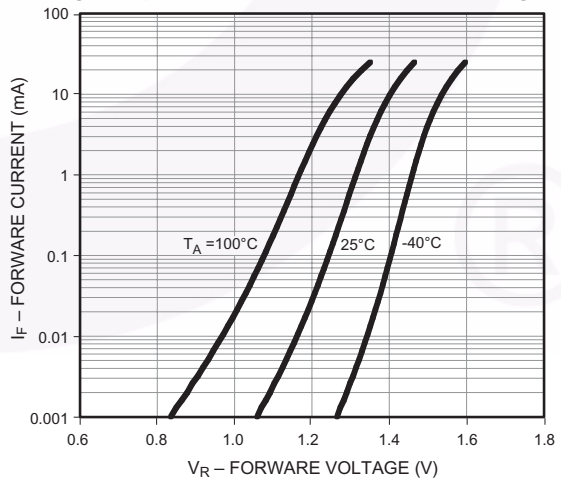
**Fig. 16 Propagation Delay vs. Series Load Capacitance**



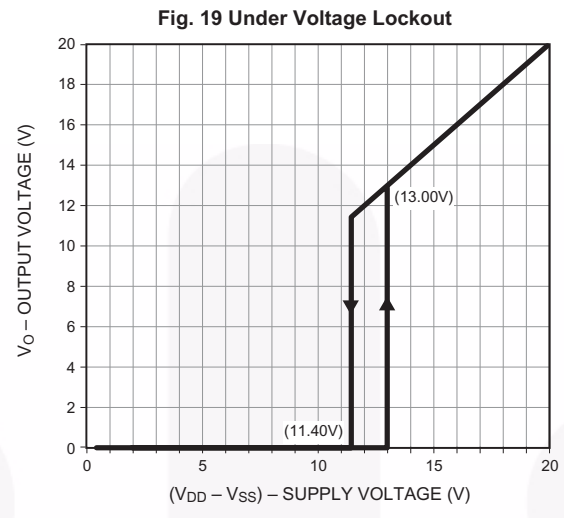
**Fig. 17 Transfer Characteristics**



**Fig. 18 Input Forward Current vs. Forward Voltage**



### Typical Performance Curves (Continued)



### Test Circuit

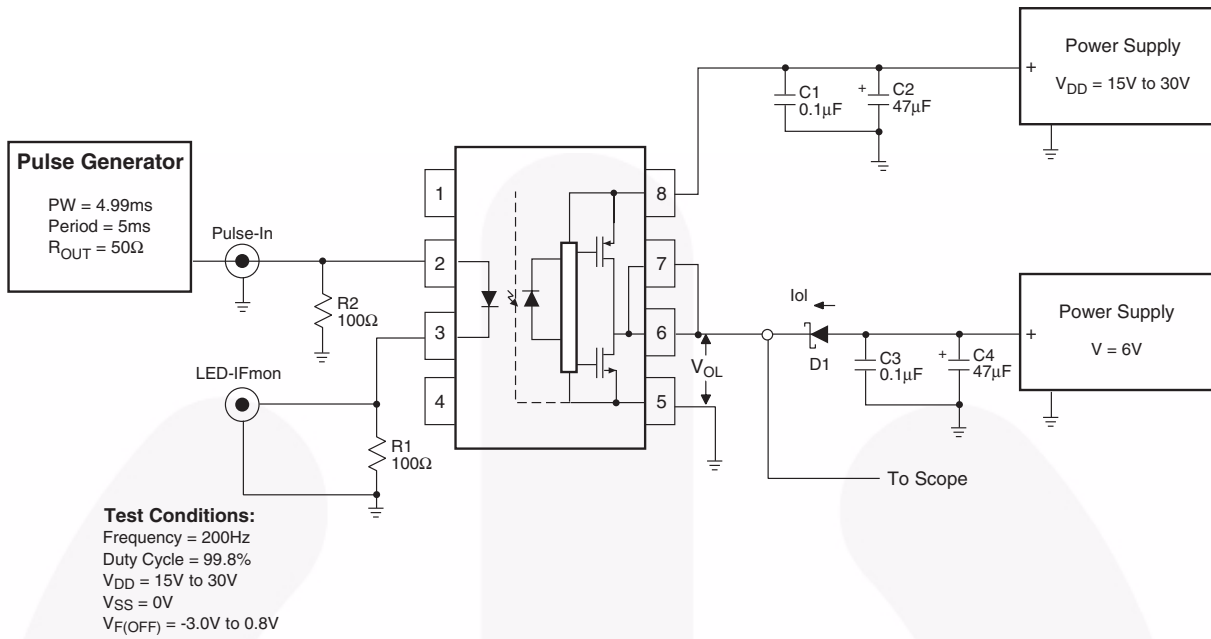


Figure 20. I<sub>OL</sub> Test Circuit

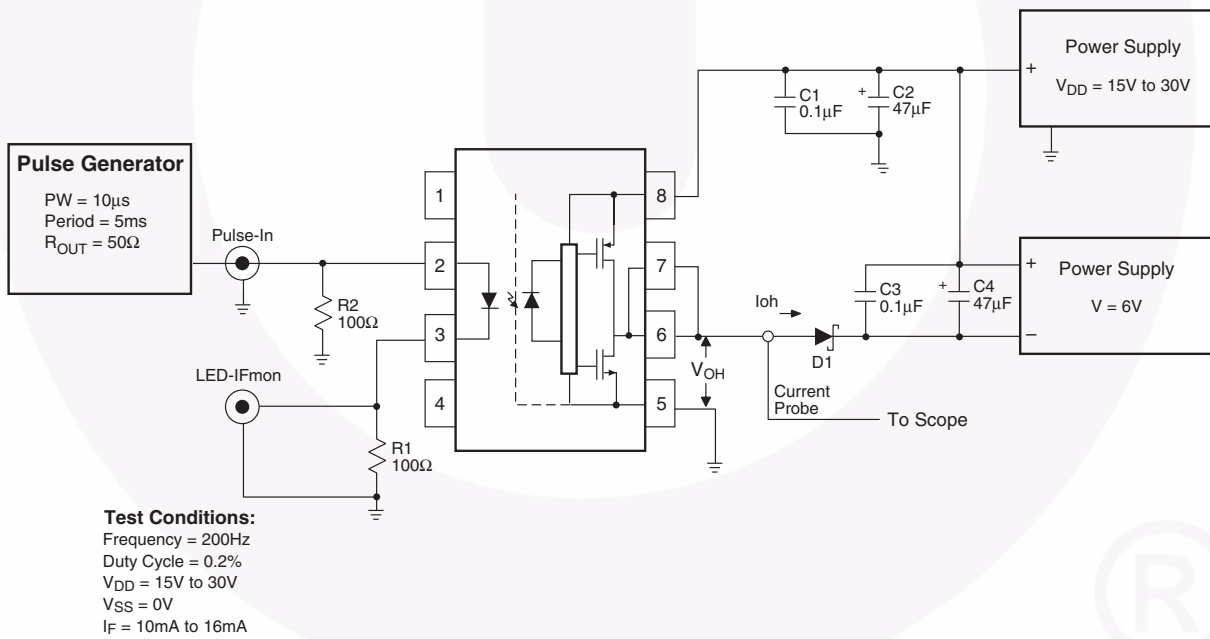
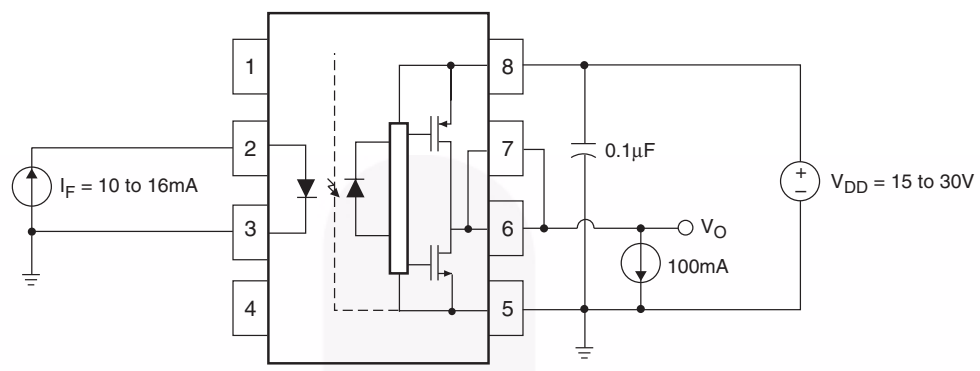
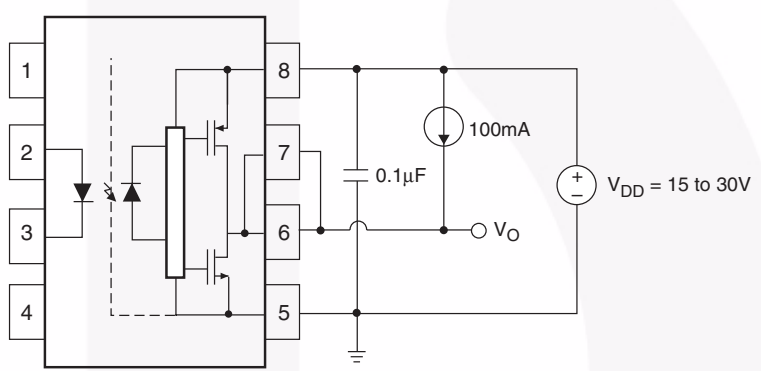


Figure 21. I<sub>OH</sub> Test Circuit

**Test Circuit** (Continued)



**Figure 22. V<sub>OH</sub> Test Circuit**



**Figure 23. V<sub>OL</sub> Test Circuit**

Test Circuit (Continued)

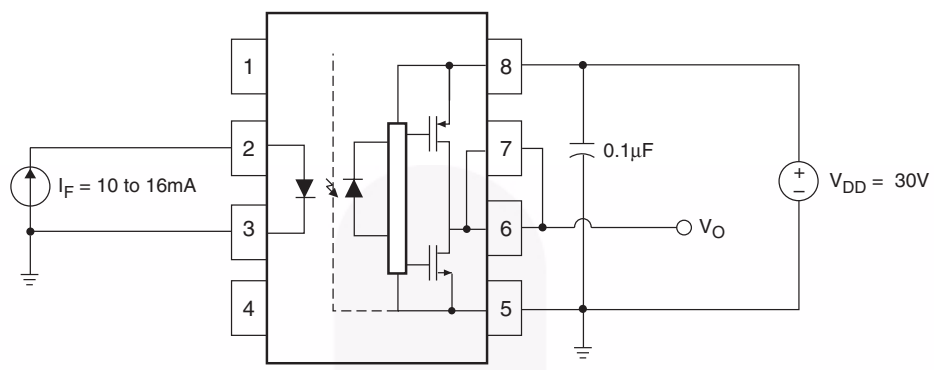


Figure 24.  $I_{DDH}$  Test Circuit

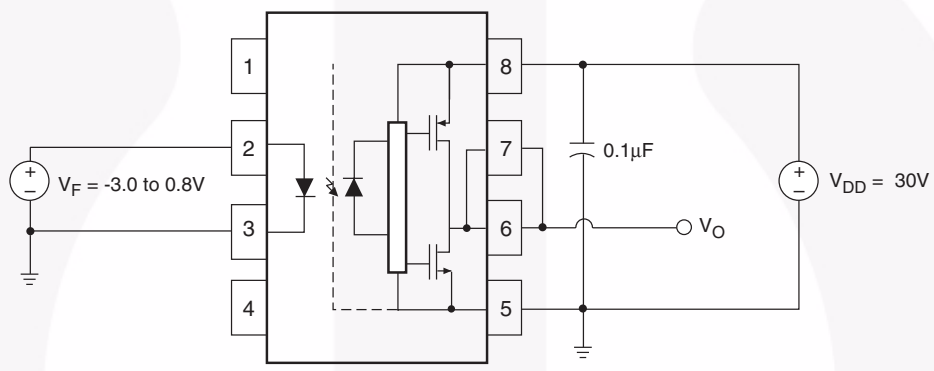
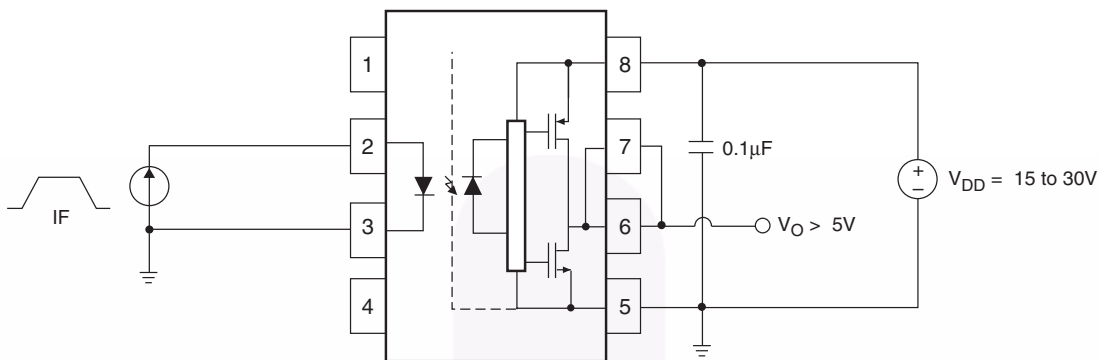
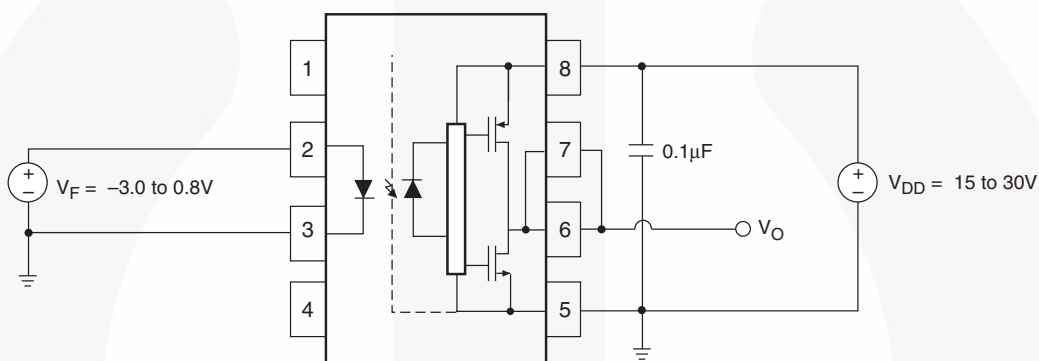


Figure 25.  $I_{DDL}$  Test Circuit

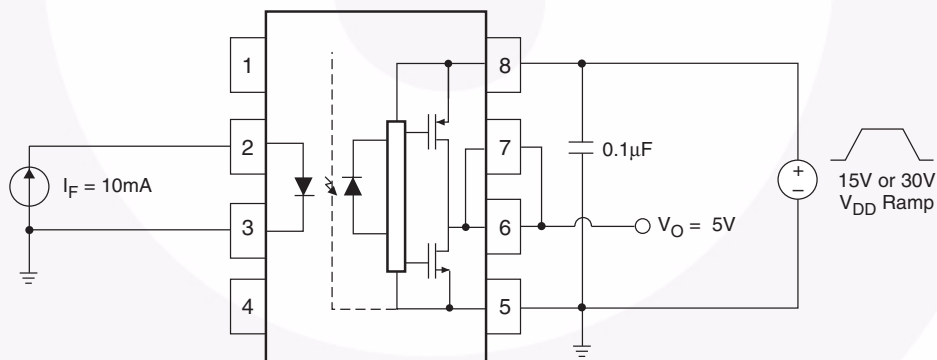
**Test Circuit** (Continued)



**Figure 26.  $I_{FLH}$  Test Circuit**

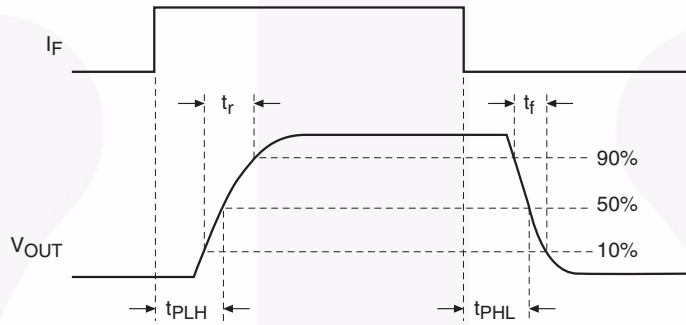
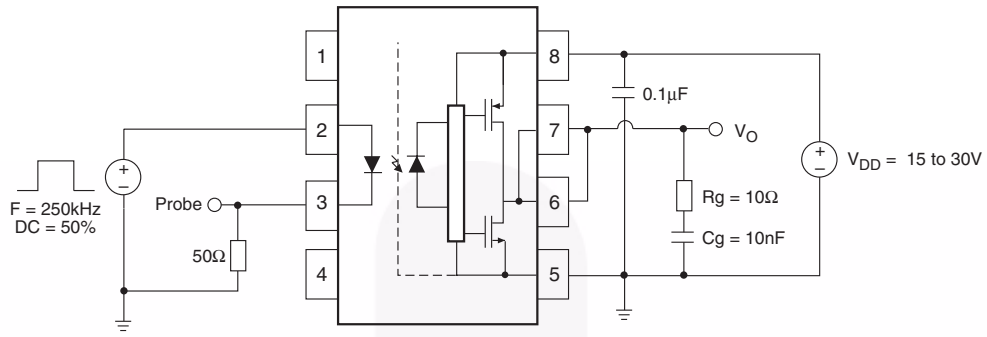


**Figure 27.  $V_{FHL}$  Test Circuit**

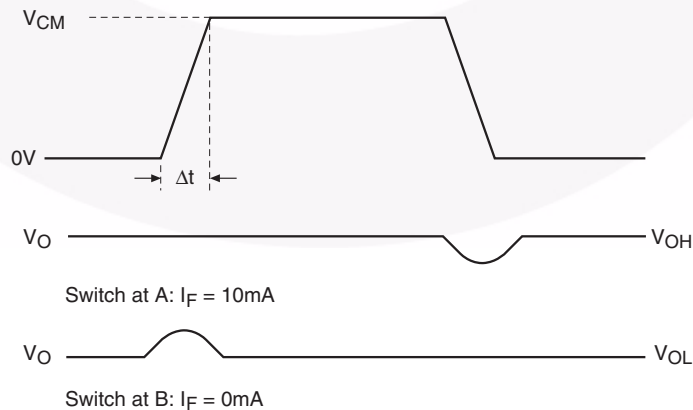
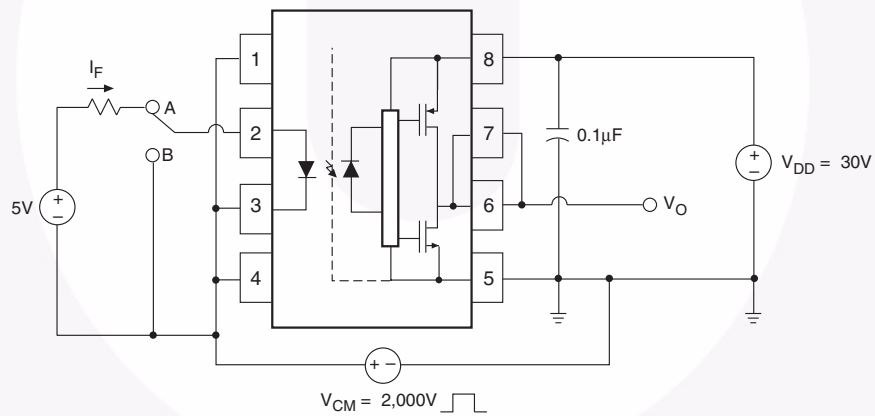


**Figure 28. UVLO Test Circuit**

**Test Circuit (Continued)**



**Figure 29. t<sub>PHL</sub>, t<sub>PLH</sub>, t<sub>r</sub> and t<sub>f</sub> Test Circuit and Waveforms**

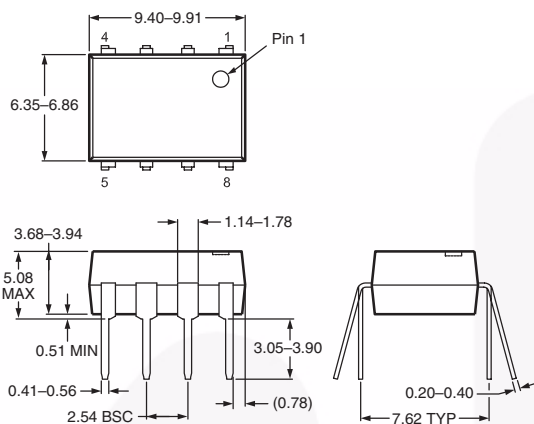


**Figure 30. CMR Test Circuit and Waveforms**

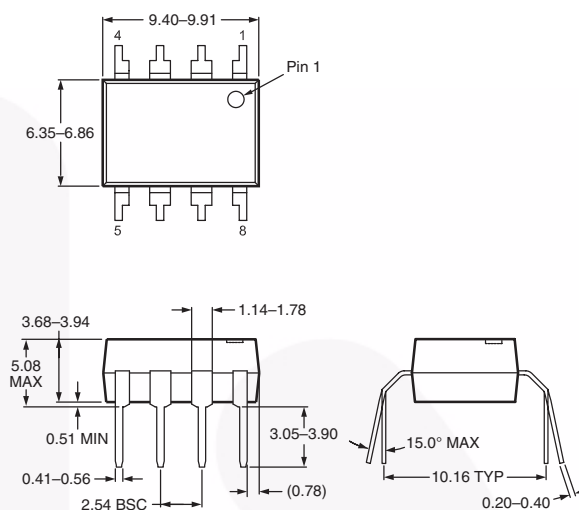


## Package Dimensions

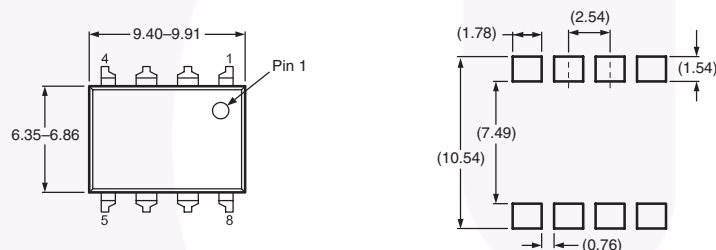
### Through Hole



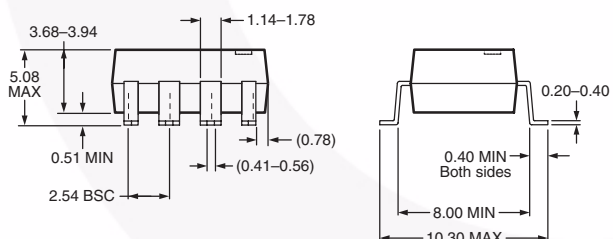
### 0.4" Lead Spacing (Option T)



### Surface Mount – 0.3" Lead Spacing (Option S)



### Recommended Land Pattern (Option S)



#### Note:

1. All dimensions are in millimeters.
2. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.

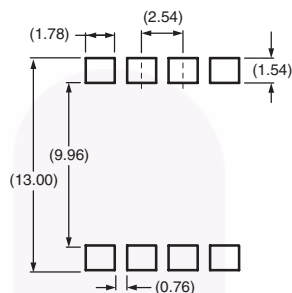
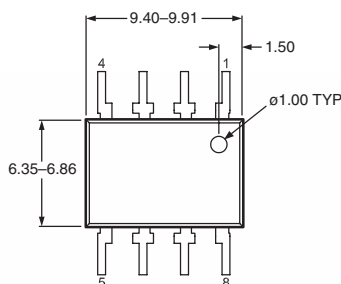
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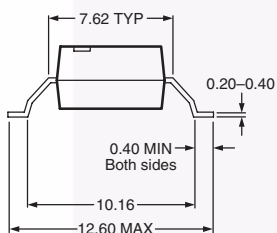
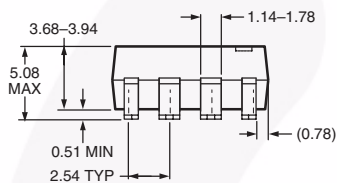
<http://www.fairchildsemi.com/packaging/>

## Package Dimensions (Continued)

### Surface Mount – 0.4" Lead Spacing (Option TS)



**Recommended Land Pattern (Option S)**



**Note:**

1. All dimensions are in millimeters.
2. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.

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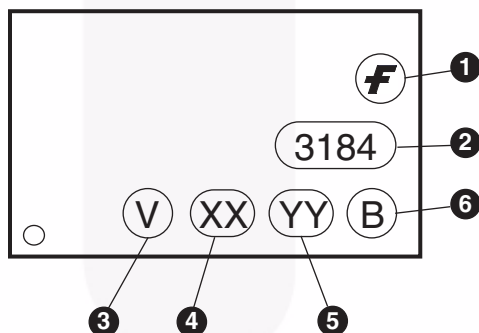
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

## Ordering Information

Part Number	Package	Packing Method
FOD3184	DIP 8-Pin	Tube (50 units per tube)
FOD3184S	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
FOD3184SD	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
FOD3184V	DIP 8-Pin, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD3184SV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD3184SDV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-2 option	Tape and Reel (1,000 units per reel)
FOD3184TV	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD3184TSV	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD3184TSR2V	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tape and Reel (700 units per reel)

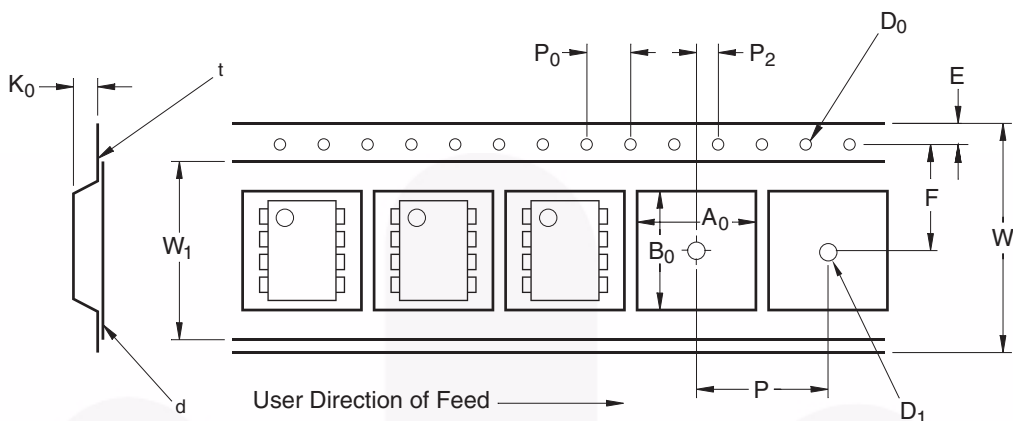
## Marking Information



### Definitions

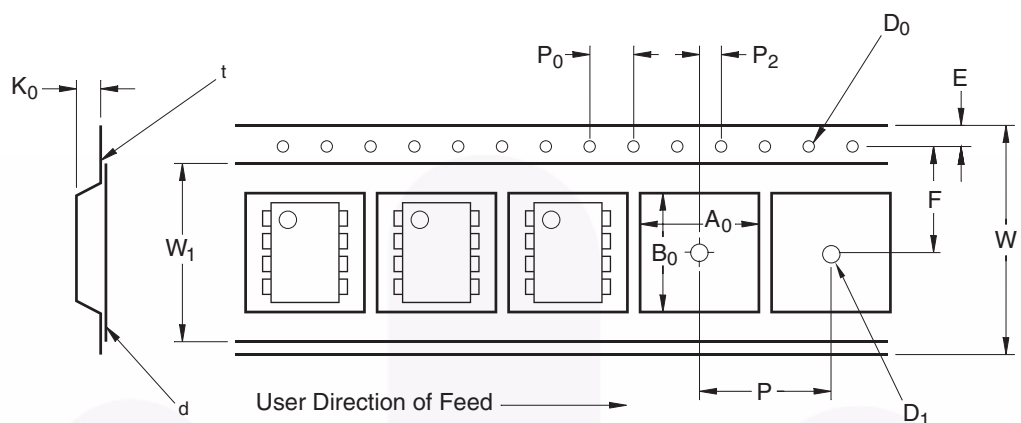
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with DIN EN/IEC 60747-5-2 option – See order entry table)
4	Two digit year code, e.g., '11'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

### Carrier Tape Specifications – Option S



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P <sub>0</sub>	Sprocket Hole Pitch	4.0 ± 0.1
D <sub>0</sub>	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P <sub>2</sub>		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A <sub>0</sub>	Pocket Dimensions	10.30 ± 0.20
B <sub>0</sub>		10.30 ± 0.20
K <sub>0</sub>		4.90 ± 0.20
W <sub>1</sub>	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

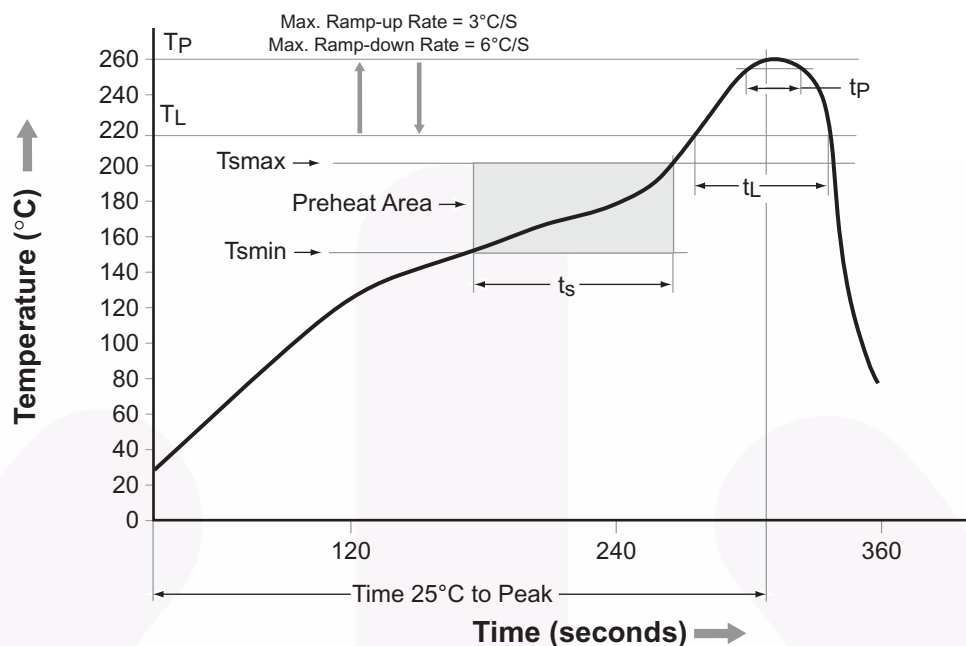
### Carrier Tape Specifications – Option TS



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P <sub>0</sub>	Sprocket Hole Pitch	4.0 ± 0.1
D <sub>0</sub>	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P <sub>2</sub>		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A <sub>0</sub>	Pocket Dimensions	12.80 ± 0.1
B <sub>0</sub>		10.35 ± 0.1
K <sub>0</sub>		5.7 ± 0.1
W <sub>1</sub>	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30



## Reflow Profile








Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60–120 seconds
Ramp-up Rate (tL to tp)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



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**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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