

**DESCRIPTION**

The LX1686E Backlight Controller IC provides all the control functions needed to implement Microsemi's direct drive inverters used to operate cold cathode fluorescent lamps (CCFL's). This IC can be used to control single or multiple-lamp configurations. CCFL's are used for back or edge lighting of liquid crystal flat panel displays (LCD's) and typically find application in notebook computers, web browsers, automotive and industrial instrumentation, and entertainment systems.

The LX1686E includes a PWM controlled lamp current burst circuit that can provide a > 100:1 dimming range from a simple zero to 2.5V potentiometer input. The PWM dimming burst rate is easily synchronized to the LCD panel's frame rate to prevent interference from optical beat frequencies.

Safety and reliability features include a new dual feedback control loop that permits regulation of maximum lamp strike voltage as well as lamp current. Regulating maximum lamp voltage permits the designer to provide for ample worst case lamp strike voltage while at the same time conservatively limit maximum open circuit voltage.

An innovative new strike voltage generation technique enables the module designer to optimize high voltage transformer design for maximum operating efficiency with no power dissipating overhead to guarantee strike capability

Direct drive topology is a non-resonant, oscillator-controlled PWM regulation method. The LX1686E allows a wide choice of fixed operating frequencies to match lamp current frequency to the lamp's most efficient operating point, and to minimize high frequency interference.

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>  
Protected by U.S. Patents 5,615,093; 5,923,129; 5,930,121; 6,198,234; Patents Pending

**KEY FEATURES**

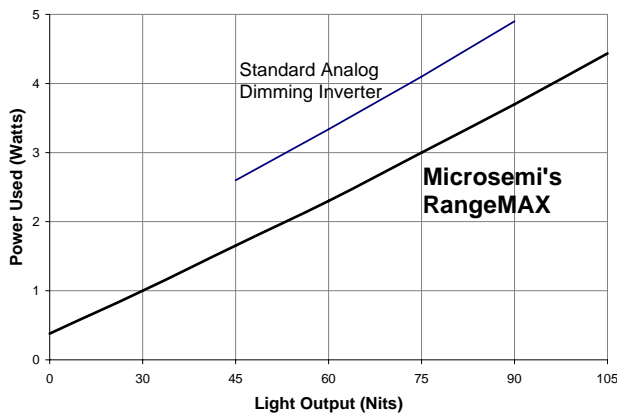
- RangeMAX™ Wide Range Dimming (>100:1)
- Synchronizable to Display Video Frequency
- High Voltage Feedback Loop Directly Controls Maximum Open Lamp
- Micro-Amp Sleep Mode
- User Programmable Fixed Frequency Operation
- Under-Voltage Lockout Feature With Power-Up Reset
- Built-In Soft-Start Feature
- Operates With 3.3V or 5V power Supplies
- 100mA Output Drive Capability

**APPLICATIONS**

- Notebooks
- Instrumentation Display
- Desktop Computer Monitors
- Low Ambient Light Displays (used in Aircraft, Automobiles, and Hand-Held Equipment)

**BENEFITS**

- Extremely High Efficiency From 3.3V to 5V Power Supplies
- Lower Cost Than Conventional Buck / Royer Inverter Topologies
- Improved Lamp Strike Capability
- Improved Over-Voltage Control

**PRODUCT HIGHLIGHT**


Light emitted by a CCFL is proportional to the current flowing through it. There are two ways to control the current: by adjusting the amplitude of a continuous AC current; or, as with RangeMAX technology, by varying the amount of time a burst of full current is present. RangeMAX technology frees the backlight inverter module designer to operate in a lower brightness and lower power consumption mode than is possible with conventional amplitude control methods.

**PACKAGE ORDER INFO**

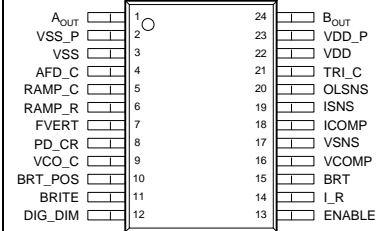
T <sub>A</sub> (°C)	<b>PW</b> Plastic TSSOP
	<b>24-PIN</b>
	RoHS compliant / Pb-free
0 to 85	<b>LX1686ECPW</b>
-40 to 85	<b>LX1686EIPW</b>

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1686ECPW-TR)

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VDD, VDD_P) .....	6.5V
Digital Inputs .....	-0.3 to VDD +0.5V
Analog Inputs .....	-0.3 to VDD +0.5V
Digital Outputs .....	-0.3 to VDD +0.5V
Analog Outputs .....	-0.3 to VDD +0.5V
Maximum Operating Junction Temperature .....	150°C
Storage Temperature .....	-65°C to 150°C
RoHS / Pb-free Peak Package Solder Reflow Temperature (40 second maximum exposure).....	260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal

**PACKAGE PIN OUT**


PW PACKAGE  
(Top View)

RoHS / Pb-free 100% Matte Tin lead Finish

**THERMAL DATA**
**PW PACKAGE**

<b>THERMAL RESISTANCE-JUNCTION TO AMBIENT, <math>\theta_{JA}</math></b>	<b>100°C/W</b>
---	----------------

Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .

The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

**FUNCTIONAL PIN DESCRIPTION**

PIN NAME	DESCRIPTION
AOUT	Output driver A, typical 10K pull down resistor to VSS_P.
VSS_P	Power ground for output drivers only.
VSS	Signal ground.
AFD_C	Connects to an external capacitor, $C_{AFD}$ . Forcing to ground or VDD will make the VCO oscillate at approximately 50% of the maximum VCO frequency. Forcing to VDD/2 will make the VCO oscillate at 2x the FVERT frequency.
RAMP_C	Connects to external capacitor $C_{RAMP}$ for setting Direct Drive PWM operating frequency.
RAMP_R	Connects to external resistor $R_{RAMP}$ for setting Direct Drive PWM operating frequency.
FVERT	Vertical frequency reference digital input. Has internal pull down.
PD_CR	Phase Detector Filter. Part of phase lock loop. Connects to external capacitor and resistor network.
VCO_C	Connects to external capacitor $C_{VCO}$
BRT_POS	Brightness control polarity. Has internal pull up. Leave open or pull up to VDD for dimming brightness proportional to BRITE voltage, connect to ground for brightness inversely proportional to BRITE voltage.
BRITE	Analog voltage input for brightness control.
DIG_DIM	Digital Dimming Enable internal pull up. Leave open or pull up to VDD for operating in digital dimming mode. Connect to ground for analog dimming mode.
ENABLE	Chip Enable internal pull up. High enables the chip. Low disables.
I_R	Current Reference Resistor. External resistor to ground ( $R_i$ ) determines internal capacitor $C_{ICOMP}$ .
BRT	Current Error Amplifier non-inverting input
VCOMP	Voltage Error Amplifier output. Connects to external frequency compensation capacitor $C_{VCOMP}$ . Controls soft-start timing.
VSNS	Voltage Error Amplifier inverting input.
ICOMP	Current Error Amplifier output. Connects to external frequency compensation capacitor $C_{ICOMP}$ .
ISNS	Current Error Amplifier inverting Input.
OLSNS	Open Lamp Sense Input.
TRI_C	Connects to external capacitor $C_{TRI}$ for setting strike Frequency ramp slope.
VDD	VDD
VDD_P	Dedicated VDD for output buffers only.
BOUT	Output Driver B typical 10K pull down resistor to VSS_P.

**ELECTRICAL CHARACTERISTICS**

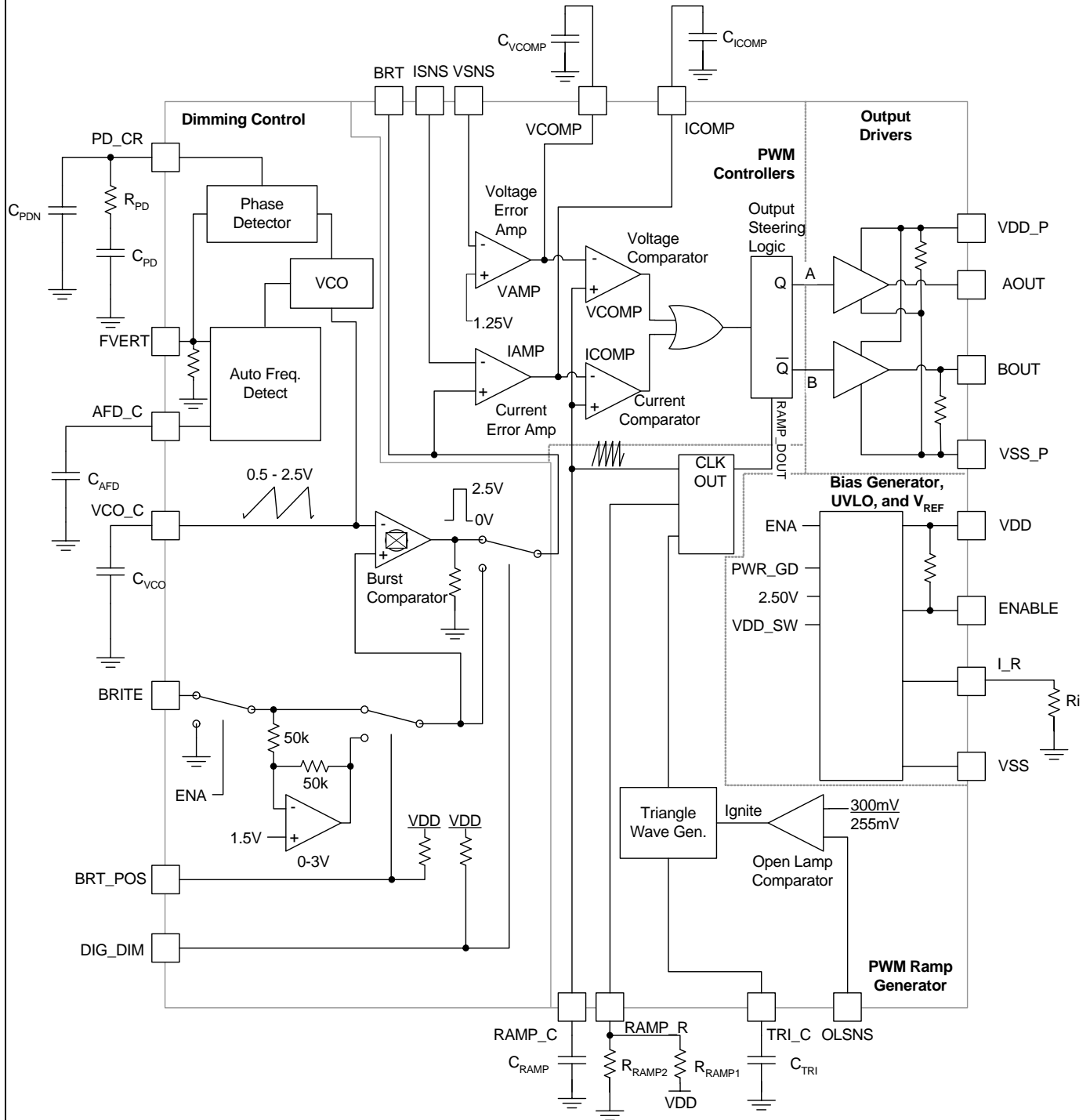
Unless otherwise specified, the following specifications apply over the operating ambient temperature  $-0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the LX1686E CPW and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the LX1686E IPW except where otherwise noted. Test conditions:  $V_{DD} = V_{DD\_P} = 3.0$  to  $5.5\text{V}$ ,  $R_i = 40\text{k}\Omega$ ,  $C_{VCO} = 0.01\mu\text{F}$ ,  $C_{AFD} = 0.22\mu\text{F}$ ,  $C_{TRI} = 0.83\mu\text{F}$ ,  $C_{RAMP} = 208\text{pF}$ ,  $R_{RAMP} = 15\text{k}\Omega$ ,  $C_{PD} = 0.22\mu\text{F}$ ,  $C_{PDB} = 0.047\mu\text{F}$ ,  $R_{PD} = 110\text{k}\Omega$

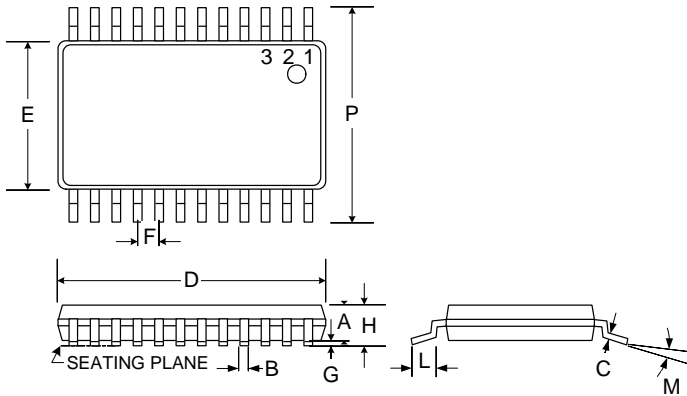
Parameter	Symbol	Test Conditions	LX1686E			Units
			Min	Typ	Max	
Power Supply Voltage	VDD	VDD = VDD_P	3		5.5	V
Operating Current	I <sub>DD</sub>	VDD = VDD_P = 5V		5	10	mA
Power Supply Voltage	VDD_P	VDD = VDD_P	3		5.5	V
Output Buffer Operating Current	I <sub>DD_P</sub>	Volsns = VDD = VDD_P = 5V, CA = CB = 1000pF		2	10	mA
UVLO Threshold	V <sub>TH_UVLO</sub>		2.7		2.9	V
UVLO Hysteresis	V <sub>H_UVLO</sub>			160		mV
<b>▶ DIRECT DRIVE RAMP BLOCK</b>						
Triangular Wave Generator Analog Output Peak Voltage	V <sub>P_TRI</sub>			2.25		V
Triangular Wave Generator Analog Output Valley Voltage	V <sub>V_TRI</sub>			0.75		V
Triangular Wave Generator Oscillation Frequency	F <sub>TRI</sub>			10		Hz
Triangular Wave Generator Oscillation Charge Current	I <sub>CHG_TRI</sub>	Tri_c = 0V	-2.3	-2.55	-2.9	μA
Triangular Wave Generator Oscillation Discharge Current	I <sub>DISCHG_TRI</sub>	Tri_c = 3V	2.3	2.65	2.9	μA
Ramp Generator Analog Output Peak Voltage	V <sub>P_RAMP</sub>			2.25		V
Ramp Generator Analog Output Valley Voltage	V <sub>V_RAMP</sub>			0.75		V
Ramp Frequency Change Threshold	V <sub>TH_RAMP_R</sub>	VDD = 3V	1.35	1.6	1.65	V
		VDD = 5.5V	1.35	1.6	1.85	V
Ramp Generator Oscillation Frequency – Nominal	F <sub>RAMP</sub>	$0 \leq V_{TRI\_C} < 1.35\text{V}$	84	100	116	KHz
Ramp Generator Oscillation Frequency – Maximum	F <sub>RAMP_HI</sub>	V <sub>TRI_C</sub> = 2.25V	170	200	256	KHz
OLSNS Threshold Voltage	V <sub>TH_OLSNS</sub>	VDD = 3V	200	300	400	mV
OLSNS Hysteresis	V <sub>H_OLSNS</sub>	VDD = 3V		45		mV
OLSNS-to-ICOMP Propagation Delay	T <sub>D_OLSNS</sub>	GBD		1		μS
<b>▶ DIGITAL DIMMER BLOCK</b>						
FVERT Input Frequency Capture Range	F <sub>R_FVERT</sub>		45		200	Hz
FVERT Logic Threshold	V <sub>TH_FVERT</sub>	Design Reference Only		VDD/2		V
FVERT Input Resistance	R <sub>FVERT</sub>	Design Reference Only		50		kΩ
VCO Analog Output Peak Voltage	V <sub>P_VCO</sub>			2.5		V
VCO Analog Output Valley Voltage	V <sub>V_VCO</sub>			0.65		V
VCO Forced Source Current	F <sub>R_VCO_I_SRC</sub>	V <sub>PD_CR</sub> = 3V, VDD = 3V	-6.4	-5.6	-5.1	μA
Forced VCO Oscillation Frequency	F <sub>X_VCO</sub>	AFC_C = 0V, CVCO = 0.01μF		250		Hz
Auto-Frequency Detection Response	T <sub>D_AFD</sub>	FVERT Frequency is 200Hz, VDD = 3V		1000		ms
BRITE Voltage Range	V <sub>R_BRITE</sub>		0		VDD	V
Full-Brightness Brite Input Voltage	V <sub>BRITE_FULL</sub>	V <sub>BRT_POS</sub> = VDD or float, BRITE = 2.5V	2.25	2.5	2.65	V
		V <sub>BRT_POS</sub> = 0V, BRITE = 0.5V	2.25	2.5	2.65	V
Full-Darkness Brite Input Voltage	V <sub>BRITE_DARK</sub>	V <sub>BRT_POS</sub> = VDD or float, BRITE = 0.5V	0.35	0.5	0.65	V
		V <sub>BRT_POS</sub> = 0V, BRITE = 2.5V	0.35	0.5	0.65	V

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, the following specifications apply over the operating ambient temperature  $-0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the LX1686E CPW and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the LX1686E IPW except where otherwise noted. Test conditions:  $V_{DD} = V_{DD\_P} = 3.0$  to  $5.5\text{V}$ ,  $R_i = 40\text{k}\Omega$ ,  $C_{VCO} = 0.01\mu\text{F}$ ,  $C_{AFD} = 0.22\mu\text{F}$ ,  $C_{TRI} = 0.83\mu\text{F}$ ,  $C_{RAMP} = 208\text{pF}$ ,  $R_{RAMP} = 15\text{k}\Omega$ ,  $C_{PD} = 0.22\mu\text{F}$ ,  $C_{PDB} = 0.047\mu\text{F}$ ,  $R_{PD} = 110\text{k}\Omega$

Parameter	Symbol	Test Conditions	LX1686E			Units
			Min	Typ	Max	
<b>DIGITAL DIMMING BLOCK (CONTINUED)</b>						
BRITE-to-ICOMP Propagation Delay	$T_{D\_BRITE}$			300		ns
BRITE_POS Logic Threshold				VDD/2		V
DIG-DIM Logic Threshold				VDD/2		V
<b>DIRECT DRIVE PWM BLOCK</b>						
ISNS Threshold Voltage Range	$V_{R\_ISNS}$	DIG_DIM = VDD	0		2.5	V
VAMP Transconductance	$G_{M\_VAMP}$	VCOMP = 1.25V		400		$\mu\text{mho}$
VAMP Output Source Current	$I_{S\_VAMP}$	VCOMP = 1.5V	10	50	110	$\mu\text{A}$
VAMP Output Sink Current	$I_{SK\_VAMP}$	VCOMP = 1.5V	15	70	120	$\mu\text{A}$
VAMP Output Voltage Range	$V_{R\_VAMP}$		0		VDD	V
VSNS Threshold Voltage	$V_{TH\_VSNS}$	VCOMP = VSNS	1.12	1.25	1.38	V
VCOMP Discharge Current	$I_{D\_VCOMP}$	VCOMP = 0.5V, VDD = 3V	0.8	1.5	10	mA
IAMP Transconductance	$G_{M\_IAMP}$	BRITE = 0.5 – 2.6V	70	200	700	$\mu\text{mho}$
IAMP Output Source Current	$I_{S\_IAMP}$	ICOMP = 1.5V, VDD = 3V	-15	-40	-80	$\mu\text{A}$
IAMP Output Sink Current	$I_{SK\_IAMP}$	ICOMP = 1.5V, VDD = 3V	20	60	100	$\mu\text{A}$
IAMP Output Voltage Range	$V_{R\_IAMP}$		0		VDD	V
VCMP Input Offset Voltage	$V_{OS\_VCMP}$	VCOMP = 1.25V, VDD = 3V	-10	3	10	mV
VCOMP-to-Output Propagation Delay	$T_{D\_VCOMP}$	VDD = 3V		250	500	ns
ICMP Input Offset Voltage	$V_{OS\_ICMP}$	ICOMP = 0.5 to 2.25V, VDD = 3V	-10	3	10	mV
ICOMP-to-Output Propagation Delay	$T_{D\_ICOMP}$	BRITE = 1.25V, RAMP_C = 2V, VDD = 3V		1100		ns
<b>OUTPUT BUFFER BLOCK</b>						
Output Sink Current	$I_{SK\_OUTBUF}$	AOUT, BOUT = 1V, VDD = 3V	20		200	mA
		AOUT, BOUT = VDD = 3V	25		300	mA
Output Source Current	$I_{SOUT\_BUF}$	AOUT, BOUT = 0V, VDD = 3V	-35		-300	mA
		AOUT, BOUT = 2V, VDD = 3V	-20		-200	mA
<b>BIAS CONTROL BLOCK</b>						
Voltage at Pin I_R	$V_{IR}$		.975		1.02	V
Pin I_R Maximum Source Current	$I_{MAX\_IR}$	Design Reference Only		50		$\mu\text{A}$
ENABLE Logic Threshold – 3V	$V_{EN3V}$	VDD = 3V	0.8	1.4	2.0	V
ENABLE Logic Threshold – 5.5V	$V_{EN5.5}$	VDD = 5.5V	0.8	1.4	2.0	V
ENABLE Threshold Hysteresis – 3V	$V_{H\_EN3}$			20		mV
ENABLE Threshold Hysteresis – 5.5V	$V_{H\_EN5.5}$			300		mV

**BLOCK DIAGRAM**


**PACKAGE DIMENSIONS**
**PW 24-Pin Thin Small Shrink Outline (TSSOP)**


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.10	—	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.55	0.246	0.256
*LC	—	0.10	—	0.004

\* Lead Coplanarity

**Note:**

- Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

**NOTES**

PRODUCTION DATA – Information contained in this document is proprietary to Microsemi and is current as of publication date. This document may not be modified in any way without the express written consent of Microsemi. Product processing does not necessarily include testing of all parameters. Microsemi reserves the right to change the configuration and performance of the product and to discontinue product at any time.