EPSON TOYOCOM

Application Manual

Real Time Clock Module

RTC-7301SF/DG

Model	Product Number
RTC-7301SF	QZ42730181000200
RTC-7301DG	QZ42730111000200

EPSON TOYOCOM CORPORATION

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CONTENTS

Multi-function 4 bit Parallel RTC Module

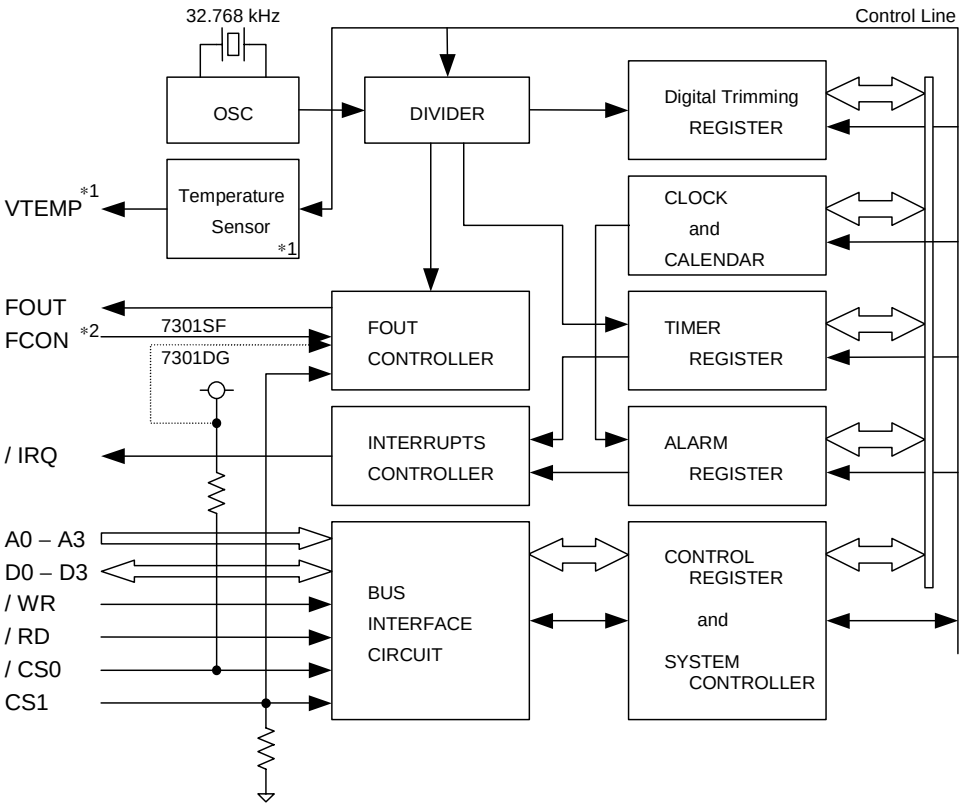
RTC - 7301 SF / DG

- Built-in crystal oscillator 32.768 kHz with frequency adjusted
- Frequency selectable clock output (32.768 kHz to 1/30 Hz)
- Built-in 30 second adjustment function, digital pace adjustment function (max. adjustment: $\pm 192 \times 10^{-6}$)
- Built-in alarm and timer interrupt functions
- Built-in semiconductor temperature sensor (Voltage output: -7.8 mV / °C , RTC-7301SF)
- Operating voltage range: 2.4 V to 5.5 V, timekeeper (retained) voltage range: 1.6 V to 5.5 V
- Low current consumption (0.6 μA / 3V Typ.)
- High speed parallel interface compatible with S-RAM

1. Overview

This is a real-time clock module using a parallel interface method with a built-in crystal oscillator.
It has a variety of built-in functions such as the leap year Clock & Calendar circuit that automatically adjust from seconds to years, the alarm and timer interrupt functions, and the time update detector. It is also equipped with a frequency selectable clock output pin.
Furthermore, it has a digital pace adjustment function for adjusting the accuracy of the clock and a semiconductor temperature sensor (analog voltage output) to enable a more accurate clock system.
Also, the interface employed is a parallel interface that is compatible with S-RAM thereby making connections easier and high speed data communication possible.
We have both SSOP and DIP package types enabling this to be used on a wide range of electronic equipment such as computers, word processors, facsimiles, multi-function telephones, sequencers and various types of control equipment.

2. Block diagram

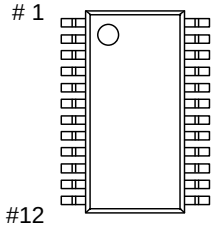


* This is a block diagram for RTC-7301SF.
Be aware that RTC-7301DG differs according to the following 2 points.
*1) The VTEMP output is not connected to an external pin.
*2) The FCON input pin is not connected to an external pin, but is fixed at “H” internally.

3. Terminal connections

RTC - 7301 SF

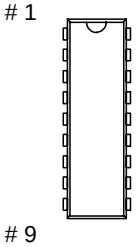
1.	/ CS0	24.	VDD
2.	FCON	23.	(VDD)
3.	FOUT	22.	(VDD)
4.	VTEP	21.	(VDD)
5.	(VDD)	20.	(VDD)
6.	/ IRQ	19.	(VDD)
7.	A0	18.	CS1
8.	A1	17.	D0
9.	A2	16.	D1
10.	A3	15.	D2
11.	/ RD	14.	D3
12.	GND	13.	/ WR



SSOP - 24 pin

RTC - 7301 DG

1.	/ CS0	18.	VDD
2.	FOUT	17.	(VDD)
3.	/ IRQ	16.	(VDD)
4.	A0	15.	CS1
5.	A1	14.	D0
6.	A2	13.	D1
7.	A3	12.	D2
8.	/ RD	11.	D3
9.	GND	10.	/ WR



DIP - 18 pin

4. Terminal functions

Pin name	Pin number 7301SF 24pin	Pin number 7301DG 18pin	I/O	Functions
/CS0	1	1	Input	This is a chip select 0 input pin and has a built-in pull-up resistor. When /CS0="L",CS1="H," access of this device is possible. Note: At the time of initial power-on, keep a level of CS 0 in High. Please use this device after making CS0 a High level once after power-on when you cannot but start CS0 with a Low level.
FCON	2	-	Input	This pin is only on the RTC7301SF. It selects the frequency to output to the FOUT pin. This pin is fixed at 32.768 kHz output when FCON="L" and frequencies are selectable by the FD bit when FCON="H." Note: This pin is not found on RTC-7301DG. It is fixed at "H" internally. Therefore, because FDOUT output frequencies are selected by the FD bit, set the FD bit and FE bit to the appropriate setting when the frequency is output to the FOUT pin.
FOUT	3	2	Output	This outputs the clock signal at the frequency set by the FD bit (CMOS output). Furthermore, output is 32.768 kHz when FCON="L." When there is no FOUT output, this pin is set to high impedance.
VTEMP	4	-	Output	This is a temperature sensor output pin found only on RTC7301SF. (Analog voltage output) When there is no VTEMP output, this pin is set to high impedance.
/IRQ	6	3	Output	This is an N-ch open-drain interrupt output pin.
A0 to A3	7 to 10	4 to 7	Input	These are address input pins. When accessing this device, this pin inputs the register address to select.
/RD	11	8	Input	This is a read strobe input pin. Data can be read from RTC when /RD="L."
GND	12	9	-	This pin is connected to the ground.
/WR	13	10	Input	This is a write strobe input pin. This pin writes data to the RTC at edge of the rise.
D0 to D3	14 to 17	11 to 14	I/O	These are data I/O pins.
CS1	18	15	Input	This is a chip select 1 input pin and has a built-in pull-down resistor. It is possible for the FOUT pin to output when CS1="H," regardless of the status of the /CS0 pin. The FOUT pin is set to high impedance when CS1="L."
(VDD)	5, 19 - 23	16,17	-	These pins have the same electrical potential as VDD, but, do not connect them to any external equipment.
VDD	24	18	-	Connect this to a + power supply.

Note 1) Be sure to connect a filter capacity of at least 0.1µF close to VDD - GND.
Note 2) When the /RD and /WR pins are both in the "L" state, mis-operations can occur. Avoid this state.

- Relationship of FOUT output and RTC access by the /CS0, CS1 and FCON pins and the FE bit

/ CS0	CS1	FCON	FE	FOUT output	RTC access
L	L	X	X	High impedance	Not possible
H	H	L	X	32.768 kHz output	Not possible
H	H	H	0	High impedance	Not possible
H	H	H	1	FD bit selectable frequency output	Not possible
L	H	L	X	32.768 kHz output	Possible
L	H	H	0	High impedance	Possible
L	H	H	1	FD bit selectable frequency output	Possible

5. Characteristics

5-1. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}	-	–0.3 to +7.0	V
Input voltage	V_{IN}	Input terminal, D0 to D3 pins	GND–0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	/ IRQ pin	GND–0.3 to +8.0	V
Output voltage (2)	V_{OUT2}	FOUT, D0-D3 pins, VTEMP pin	GND–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	Stored bare product after unpacking	–55 to +125	°C

5-2. Recommended operating conditions

GND=0 V

Item	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	-	2.4 to 5.5	V
Clock power supply voltage	V_{CLK}	-	1.6 to 5.5	V
Operating temperature	T_{OPR}	No condensation	–40 to +85	°C

5-3. Oscillating characteristics

Item	Symbol	Condition	Rating	Unit
Frequency precision	Δ f / fo	Ta= +25 °C, V_{DD}=3.0 V	5 ± 23 (*1)	$\times 10^{-6}$
Frequency voltage characteristics	f / V	Ta= +25 °C, V_{DD}=1.6 V to 5.5 V	$\pm$ 2 Max.	$\times 10^{-6}$ / V
Frequency temperature characteristics	Top	Ta= –10 °C to +70 °C, V_{DD}=3.0 V Ta=+25°C is standard (=0).	+10 / –120	$\times 10^{-6}$
Oscillating starting time	t_{STA}	Ta= +25 °C, V_{DD}=2.4 V	3 (Max.)	s
Aging amount	fa	Ta= +25 °C, V_{DD}=3.0 V ; first year	$\pm$ 5 Max.	$\times 10^{-6}$ / year

*1) Equivalent to 1 minute of monthly deviation (excluding offset).

5-4. DC characteristics

5-4-1. DC characteristics (1) * Unless specified otherwise : GND=0 V , V_{DD}=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

Item	Symbol		Condition	Min.	Typ.	Max.	Unit
Current consumption (When non-accessed) FOUT =Output OFF VTEMP =Output OFF	I_{DD1}	V_{DD}=5 V	/CS0,/RD,/WR=V_{DD}, A0-A3, CS1=GND D0-D3,/IRQ=Hi-z, FOUT=Hi-z(OFF) VTEMP=Hi-z(OFF)	-	1.0	2.0	µA
	I_{DD2}	V_{DD}=3 V		-	0.6	1.0	µA
Current consumption (When non-accessed) FOUT = 32 kHz Output VTEMP = Output OFF	I_{DD3}	V_{DD}=5 V	/CS0,/RD,/WR,CS1=V_{DD} A0-A3=GND, D0-D3, /IRQ=Hi-z FOUT=32 kHz Output, When CL= 0pF VTEMP=Hi-z(OFF)	-	3.0	7.5	µA
	I_{DD4}	V_{DD}=3 V		-	1.7	4.5	µA
	I_{DD5}	V_{DD}=5 V	/CS0,/RD,/WR,CS1=V_{DD} A0-A3=GND D0-D3,/IRQ=Hi-z FOUT=32 kHz Output, When CL=30 pF VTEMP=Hi-z(OFF)	-	8.0	20	µA
	I_{DD6}	V_{DD}=3 V		-	5.0	12	µA
Current consumption (When non-accessed) FOUT = Output OFF	I_{DD7}	V_{DD}=5 V	/CS0,/RD,/WR=V_{DD}, Ta= +25 °C A0-A3,CS1=GND D0-D3,/IRQ=Hi-z FOUT=Hi-z(OFF) VTEMP=ON	-	50	75	µA
	I_{DD8}	V_{DD}=3 V		-	40	60	µA

Note) There is no VTEMP pin on the RTC-7301DG so be aware of the following.
*1) Does not apply for I_{DD7}, I_{DD8}.
*2) Specifications for the VTEMP pin within the conditions described above do not apply for I_{DD1}–I_{DD6}.

-4-2. DC characteristics (2) * Unless specified otherwise : GND=0 V , V_{DD}=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input voltage (1)	V_{IH1}	V_{DD}=4.5 V to 5.5 V	/CS0, FCON, /RD, /WR A0-A3, D0-D3 pins	2.2		V_{DD}+0.3	V
	V_{IL1}			GND–0.3		0.8	V
Input voltage (2)	V_{IH2}	V_{DD}=2.4 V to 3.6 V	/CS0, FCON, /RD, /WR A0-A3, D0-D3 pins	0.8V_{DD}		V_{DD}+0.3	V
	V_{IL2}			GND–0.3		0.2V_{DD}	V
Input voltage (3)	V_{IH3}	V_{DD}=1.6 V to 5.5 V	CS1 pin	0.8V_{DD}		V_{DD}+0.3	V
	V_{IL3}			GND–0.3		0.2V_{DD}	V
Input leakage current	I_{LEK}	/CS0:V_{IN}=V_{DD}, CS1:V_{IN}=GND FCON, /RD, /WR, A0-A3 : V_{IN}=V_{DD} or GND		–0.5		0.5	µA

Note) There is no FCON pin on the RTC-7301DG so standards for the FCON pin within the conditions described above do not apply.

-4-3. DC characteristics (3) * Unless specified otherwise : GND=0 V , V_{DD}=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Pull-up resistor (1)	R_{UP1}	V_{DD}=5 V	/CS0 pin V_{IN}=GND	75	150	300	kΩ
Pull-up resistor (2)	R_{UP2}	V_{DD}=3 V		150	300	600	kΩ
Pull-down resistor (1)	R_{DWN1}	V_{DD}=5 V	CS1 pin, V_{IN}=V_{DD}	20	40	80	MΩ
Pull-down resistor (2)	R_{DWN2}	V_{DD}=3 V		42.5	85	170	MΩ
Pull-down resistor (3)	R_{DWN3}	V_{DD}=5 V	CS1 pin, V_{IN}=0.5 V	30	60	120	kΩ
Pull-down resistor (4)	R_{DWN4}	V_{DD}=3 V	CS1 pin, V_{IN}=0.5 V	55	110	220	kΩ
"H" Output voltage (1)	V_{OH1}	V_{DD}=5 V	I_{OH}= –1 mA	4.5		5.0	V
"H" Output voltage (2)	V_{OH2}	V_{DD}=3 V	D0-D3, FOUT pin	2.0		3.0	V
"H" Output voltage (3)	V_{OH3}	V_{DD}=3 V	I_{OH}= –100 µA D0-D3, FOUT pin	2.9		3.0	V
"L" Output voltage (1)	V_{OL1}	V_{DD}=5 V	I_{OL}= 1 mA	0		0.5	V
"L" Output voltage (2)	V_{OL2}	V_{DD}=3 V	D0-D3, FOUT pin	0		0.8	V
"L" Output voltage (3)	V_{OL3}	V_{DD}=3 V	I_{OL}= 100 µA D0-D3, FOUT pin	0		0.1	V
"L" Output voltage (4)	V_{OL4}	V_{DD}=5 V	I_{OL}= 1 mA	0		0.25	V
"L" Output voltage (5)	V_{OL5}	V_{DD}=3 V	/IRQ pin	0		0.4	V
Output leakage current	I_{OZ}	D0-D3, /IRQ, FOUT pin V_{OUT}=V_{DD} or GND		- 0.5		0.5	µA

-5. Pin capacity characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Address input capacity	C_{ADD}	A0 to A3 pins			8	pF
Data input capacity	C_{DATA}	D0 to D3 pins			15	pF

-6. Temperature sensor characteristics

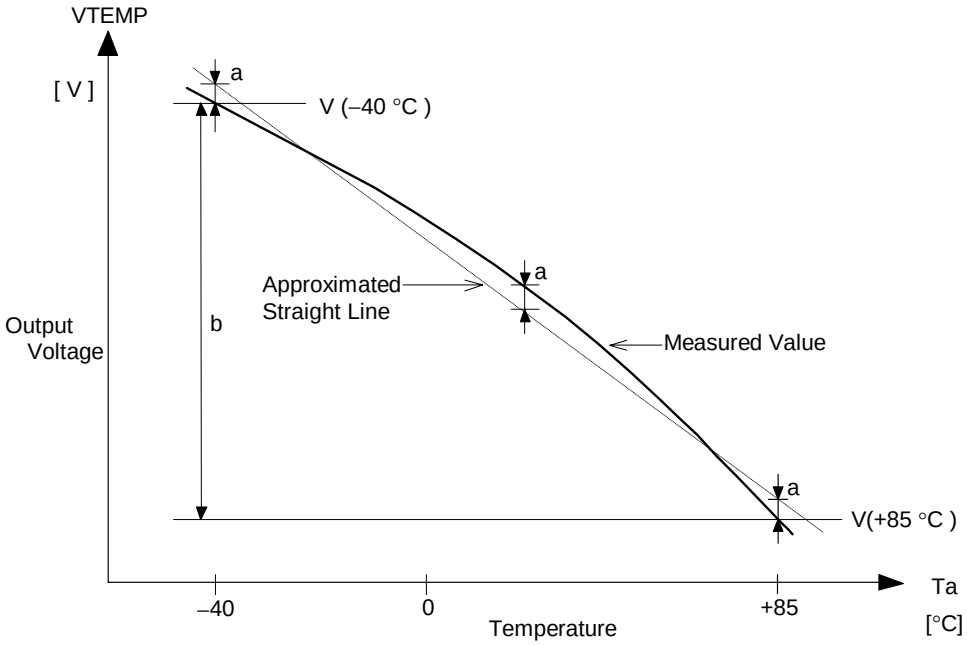
* Unless specified otherwise :
GND=0 V , V_{DD}=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature output voltage	V_{TEMP}	Ta= +25 °C , GND based output voltage VTEMP pins, V_{DD}=2.7 V to 5.5 V		1.470		V
Output precision	T_{ACR}	Ta =+25 °C , V_{DD}=2.7 V to 5.5 V			± 5.0	°C
Temperature sensitivity	V_{SE}	–40 °C ≤ Ta ≤ +85 °C , V_{DD}=2.7 V to 5.5V	–7.3	–7.8	–8.3	mV/°C
Linearity	ΔNL	–40 °C ≤ Ta ≤ +85 °C , V_{DD}=2.7 V to 5.5V			± 2.0	%
Temperature detection range	T_{SOP}	ΔNL ≤ ± 2.0 % , V_{DD}=2.7 V to 5.5V	–40		+ 85	°C
Output resistance	R_O	Ta= +25 °C, VTEMP pins, V_{DD}=2.7 V to 5.5V GND standard and V_{DD} standard		1.0	3.0	kΩ
Load condition	C_L	V_{DD}=2.7 V to 5.5V			100	pF
	R_L	V_{DD}=2.7 V to 5.5V	500			kΩ
Response time	t_{RSP}	V_{DD}=3.3 V C_L=50 pF , R_L=500 kΩ , Max. ± 1°C			200	µs

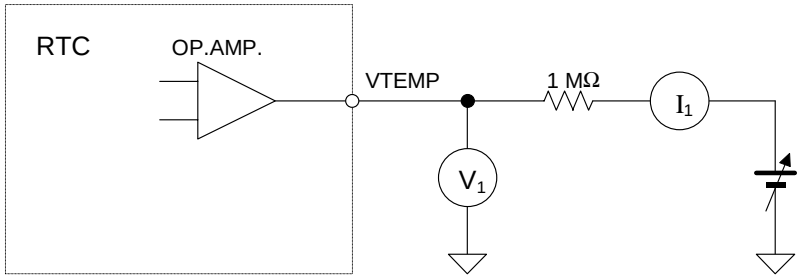
Note1) Temperature sensitivity V_{SE} = (V (+85 °C) – V (–40 °C)) / 125 [mV/°C]

Note 2) Linearity $\Delta NL = \frac{a}{b} \times 100$ [%]

a: Maximum deviation between the measure value of VTEMP and the approximated straight line.
b: Difference between measured values at -40 °C and +85 °C



Note 3) Output resistance (Ro) $Ro = \Delta V_1 / \Delta I_1$



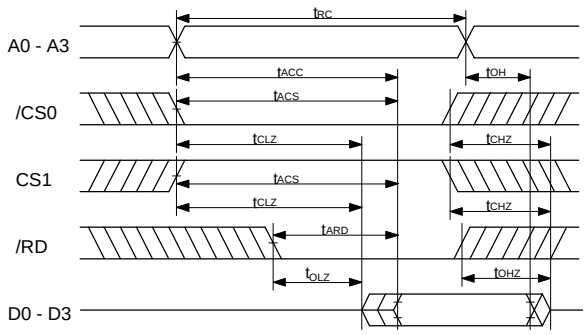
Note) There is no temperature sensor function on the RTC-7301DG.

6-7. AC characteristics

* If not specifically indicated:
- GND=0 V , Ta= –40 °C to +85 °C
- Input conditions: V_I=0.5 × V_{DD}, V_O=0.5 × V_{DD}
- Output load: C_L=100 pF (t_{ACC},t_{ACS},t_{ARD})

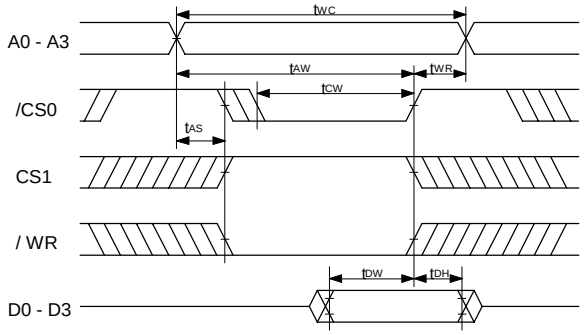
Item	Symbol	Condition	V_{DD}=2.4 to 3.6V		V_{DD}=4.5 to 5.5V		Unit
			Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	-	150	-	85	-	Ns
Address access time	t_{ACC}	-	-	150	-	85	Ns
CE access time	t_{ACS}	-	-	150	-	85	Ns
RD access time	t_{ARD}	-	-	100	-	45	Ns
CE output set time	t_{CLZ}	-	5	-	3	-	ns
CE output floating	t_{CHZ}	-	-	60	-	30	ns
RD output set time	t_{OLZ}	-	5	-	3	-	ns
RD output floating	t_{OHZ}	-	-	60	-	30	ns
Output hold time	t_{OH}	-	10	-	5	-	ns
Write cycle time	t_{WC}	-	150	-	85	-	ns
Chip select time	t_{CW}	-	140	-	70	-	ns
Address valid to end of write	t_{AW}	-	140	-	70	-	ns
Address setup time	t_{AS}	-	0	-	0	-	ns
Address hold time	t_{WR}	-	0	-	0	-	ns
Write pulse width	t_{WP}	-	130	-	65	-	ns
Input data set time	t_{DW}	-	80	-	35	-	ns
Input data hold time	t_{DH}	-	0	-	0	-	ns
FOUT output frequency duty	DUTY	FOUT = 32.768 kHz	40	60	40	60	%

(1) Reading data

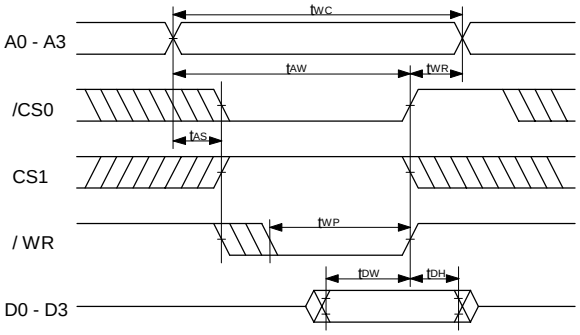


(2) Writing data

i) CS Control



ii) WR Control



Note: At the time of initial power-on, keep a level of CS 0 in High. Please use this device after making CS0 a High level once after power-on when you cannot but start CS0 with a Low level.

6. Registers

6-1. Register table

Bank 0 Clock and calendar registers

Address	Register	bit 3	bit 2	bit 1	bit 0
0	1 second	8	4	2	1
1	10 second	Fos	40	20	10
2	1 minute	8	4	2	1
3	10 minute	○	40	20	10
4	1 hour	8	4	2	1
5	10 hour	○	○	20	10
6	Day	○	4	2	1
7	1 day	8	4	2	1
8	10 day	○	○	20	10
9	1 month	8	4	2	1
A	10 month	○	○	○	10
B	1 year	8	4	2	1
C	10 year	80	40	20	10
D	100 year	800	400	200	100
E	1000 year	*1,*2 TEST	*1,*2 TEMP	2000	1000
F *1	Control register *1	Bank Sel 1 *1	Bank Sel 0 *1	STOP *1	BUSY / ADJ *1

Bank 1 Alarms and FOUT registers

Address	Register	bit 3	bit 2	bit 1	bit 0
0	1 second	8	4	2	1
1	10 second	AE	40	20	10
2	1 minute	8	4	2	1
3	10 minute	AE	40	20	10
4	1 hour	8	4	2	1
5	10 hour	AE	•	20	10
6	Day	AE	4	2	1
7	1 day	8	4	2	1
8	10 day	AE	•	20	10
9	-	•	•	•	•
A	-	•	•	•	•
B	CS1 Controller	CTEMP	CDT_ON	•	•
C	FOUT divider ratio setting register	○	FD2	FD1	FD0
D	FOUT divider ratio setting register	FE	○	FD4	FD3
E	Alarm control	*1,*2 TEST	*1,*2 TEMP	AF	AIE
F *1	Control register *1	Bank Sel 1 *1	Bank Sel 0 *1	STOP *1	BUSY / ADJ *1

Bank 2 Digital offset and timer registers

Address	Registers	bit 3	Bit 2	bit 1	bit 0
0	Digital offset	DT3	DT2	DT1	DT0
1		DT_ON	DT6	DT5	DT4
2	–	○	○	○	○
3	–	○	○	○	○
4	Timer counter preset value	8	4	2	1
5		128	64	32	16
6	Timer counter data	8	4	2	1
7		128	64	32	16
8	Timer settings	TE	TI / TP	TD1	TD0
9	–	○	○	○	○
A	–	○	○	○	○
B	–	○	○	○	○
C	–	○	○	○	○
D	–	○	○	○	○
E	Timer control	*1,*2 TEST	*1,*2 TEMP	TF	TIE
F *1	Control register *1	Bank Sel 1 *1	Bank Sel 0 *1	STOP *1	BUSY / ADJ *1

1) [*1] bits (all bits of the control registers and the TEST bits and TEMP bits) are common for all BANKs.
2) When the power is turned on initially, the [*2] TEST and TEMP bits are cleared to 0. Also, Fos is set to 1, but because other the register values of other bits are unknown, always make their initial settings. When doing so, do not make settings for date and time that are impossible. We do not guarantee proper operation of the clock for such settings. When digital pace adjustment function is not used , please clear a DT_ON bit to 0 at the time of initial setting, by all means.
3) The TEST bit is our internal test bit.
   Always use with this set to "0."
   Note) When using the RTC-7301DG, always use with the [*2] TEST and TEMP bits set to "0."
4) Write is possible for the AF and TF bits only when set to "0."
5) " ○ " bits should be used when set to "0" after the initial settings.
6) " • " bits can be used as RAM.
7) When not using the alarm interrupt, it is possible to use BANK 1 registers 0 to 8 as RAM. (Total 36 bits)
8) When not using the timer interrupt, it is possible to use BANK 2 registers 4 to 5 as RAM. (Total 8 bits)
9) When not using digital pace adjustment, Bank 2 registers 0 to 1 can be used as RAM except DT_ON. (Total 7 bits)
10) The BUSY/ADJ bit is busy when reading and is a 30 second ADJ bit when writing. Also, a BUSY flag is set 122 μs before and after the time update timing. The ADJ bit is cleared to 0 automatically at a maximum of 244 μs after being set.

- FOUT setting registers (Bank 1 Registers C and D)
- Timer setting registers (Bank 2 Register 8)

FD4	FD3	Source clock
0	0	32768 Hz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

FD2	FD1	FD0	Divider ratio
0	0	0	1 / 1
0	0	1	1 / 2
0	1	0	1 / 3
0	1	1	1 / 6
1	0	0	1 / 5
1	0	1	1 / 10
1	1	0	1 / 15
1	1	1	1 / 30

TD1	TD0	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	Update in seconds
1	1	Update in minutes

6-2. Register description

6-2-1. Clock and calendar registers (Bank0, Reg-0 to Reg-E)

- Data is in BCD format. For example, if the 10 second register is “0101” and the 1 second register is “1001” it has the meaning of 59 seconds.
- The clock keeps time using a 24 hour format.
- Leap years are automatically determined between the years of 1901 and 2099.
- Days are in Bank 0 Reg-6.
  Day registers are in 3 bits from bit 0 to 2 and are allocated as shown in the following table.

Bit 2	bit 1	bit 0	Day
0	0	0	Sun.
0	0	1	Mon.
0	1	0	Tues.
0	1	1	Wed.
1	0	0	Thurs.
1	0	1	Fri.
1	1	0	Sat.

- **Fos (Oscillation voltage decrease detection bit)**
  This flag is a bit for recording the decrease in voltage on the crystal oscillator. It detects the decrease in the voltage of the crystal oscillator that is in use and is a flag bit for notifying the decrease in the reliability of the time data.
  “1” indicates a decrease in the voltage and it is retained until a “0” is written.
  This is not affected by the function of other bits.

6-2-2. Alarm register (Bank1 Reg-0 to Reg-8 and Reg-E)

- **AE bit:** (Alarm Enable)
  This bit enables the setting of the alarms for date, day, hour, minute and second.
  An AE bit accompanies the alarm register, so using this bit makes it easy to set the alarm for each second, each minute, each hour, each day or each date.
  It is not possible to set a multiple of days at one time.
  When the AE bit is 0, the appropriate register and the clock register are compared; when the bit is 1, this means "don't care" and the data is ignored and the two are regarded as the same.

- Example of setting day alarm bits for each day (Bank1 Reg-6)

bit 2	bit 1	bit 0	Day
0	0	0	Sun.
0	0	1	Mon.
0	1	0	Tues.
0	1	1	Wed.
1	0	0	Thurs.
1	0	1	Fri.
1	1	0	Sat.

- **AF bit:** (Alarm Flag)
  The AF bit is “1” when an alarm occurs.
  This data is retained until a “0” is written. It is not possible to write “1.”

- **AIE bit:** (Alarm Interrupt Enable)
  This bit sets whether or not to output the alarm interrupt signal to the /IRQ pin.
  The /IRQ pin is Low active when the AF bit is set to 1 at the time of an alarm interrupt, if the AIE bit is “1.”
  An alarm interrupt output is prohibited from the /IRQ pin when the AIE bit is “0.”
  It is necessary to set the AIE bit to “1” in order to have an alarm interrupt.

6-2-3. CS1 control registers (Bank1, Reg-B)

Address	Register	bit 3	bit 2	bit 1	bit 0
B	CS1 control	CTEMP	CDT_ON	•	•

The CS 1 control register CTEMP bit selects whether or not to link the temperature sensor operation with the logic status of each CS1 pin. The CDT_ON bit selects whether or not to link the digital pace adjustment function (called digital offset below) with the logic status of each CS1 pin.

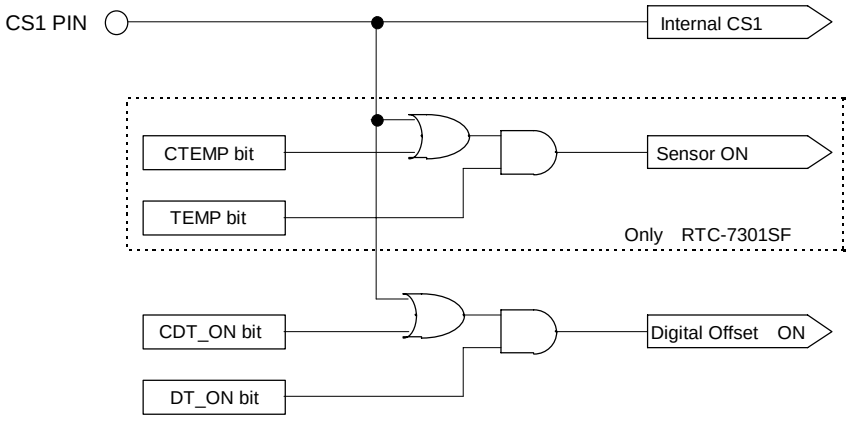
•**CTEMP** bit

Setting CTEMP to "0" will operate the temperature sensor only when the CS1 pin is “H.”
Setting CTEMP to "1" will operate the temperature sensor regardless of the CS1 pin.
(A separate TEMP bit setting is necessary for the operation of the temperature sensor.)

Note) Set to [CTEMP bit = “0”] because there is no temperature sensor output for the RTC-7301DG.

•**CDT_ON** bit

Setting CDT_ON to “0” will operate the digital offset only when the CS1 pin is “H.”
Setting CDT_ON to “1” will operate the digital offset regardless of the CS1 pin.
(A separate DT_ON bit setting is necessary for the operation of the digital offset.)



•Function operating tables

1) Temperature sensor

CS1 Pin	CTEMP bit	TEMP bit	Temperature sensor
X	X	0	Stops
L	0	1	Stops
H	0	1	Runs
L	1	1	Runs
H	1	1	Runs

Note) This function does not operate because there is no temperature sensor function on the RTC-7301DG.

2) Digital offset

CS1 Pin	CDT_ON bit	DT_ON bit	Digital offset
X	X	0	Stops
L	0	1	Stops
H	0	1	Runs
L	1	1	Runs
H	1	1	Runs

6-2-4. FOUT frequency setting registers (Bank1, Reg-C and D)

Address	Registers	bit 3	bit 2	Bit 1	bit 0
C	FOUT divider ratio setting	○	FD2	FD1	FD0
D	FOUT frequency setting	FE	○	FD4	FD3

- **FE bit**: (Fout Enable)
  When the FCON bit is "H," the specified frequency (source clock) is output from the FOUT pin at the specified divider ratio when the FE bit is "1."
  When the FE bit is "0," output enters a prohibitive state (high impedance).
  When the FCON pin is "L," 32.768 kHz is output from the FOUT pin regardless of the content of the Reg-C and D.
  Note) Internally, [FCON pin = "H"] on the RTC-7301DG.

- **FD bit**

FD4	FD3	Source clock
0	0	32768 Hz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

FD2	FD1	FD0	Divider ratio	FOUT duty
0	0	0	1 / 1	1 / 2
0	0	1	1 / 2	1 / 2
0	1	0	1 / 3	1 / 3
0	1	1	1 / 6	1 / 2
1	0	0	1 / 5	1 / 5
1	0	1	1 /10	1 / 2
1	1	0	1 /15	1 / 3
1	1	1	1 /30	1 / 2

6-2-5. Timer register (Bank2, Reg-4 to Reg-8 and Reg-E)

These registers control the 8 bit pre-settable down-counter used in the timer interrupt.
The down-counter counting cycle (source clock) is specified by Reg-8 TD0 and TD1. Reg-4 and 5 specify the pre-set (divider) value of the down-counter.

The down-counter continues counting down using the specified source clock period. When it reaches zero, the TF (Timer Flag) is set to "1."

At this time, when the Reg-E TIE (Timer Interrupt Enable) bit is "1," the /IRQ pin becomes a Low level and an interrupt occurs. When the TIE bit is "0," output from the /IRQ pin is prohibited.
Also, when the TI / TP bits are "1," the timer counter register data is re-loaded and another count-down is started. (Repeat operation)

- Timer interrupt source clock selections

TD1	TD0	Source clock	IRQ automatic return time
0	0	4096 Hz	0.122 ms
0	1	64 Hz	7.81 ms
1	0	Update in seconds	7.81 ms
1	1	Update in minutes	7.81 ms

- Timer interrupt intervals

Timer counter setting values	Source clock			
	4096 Hz	64 Hz	Update in seconds	Update in minutes
0	-	-	-	-
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.250 ms	2 s	2 min
3	732.42 μs	46.875 ms	3 s	3 min
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
255	62.26 ms	3.984 s	255 s	255 min

- **TF bit**: (Timer Flag)
  The TF bit set to 1 when the timer reaches zero. The data is maintained until 0 is written. It is not possible to write 1.

- **TE bit**: (Timer Enable)
  When TE is set to 1 , timer is running. When TE is cleared to 0, Timer stops.

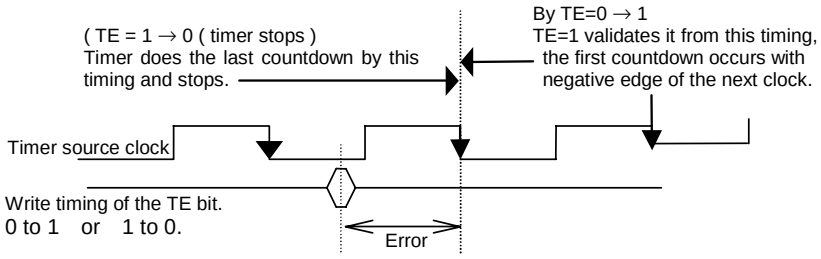
- **TIE** bit: (Timer Interrupt Enable)
  This bit determines whether or not to drive the /IRQ pin when there has been a timer interrupt.
  When the TIE bit is "0," the timer interrupt is not output to the /IRQ pin.

- **TI/TP** bits: (Interrupt Signal Output Mode Select. Interrupt / Periodic)
  These bits set the output mode of the timer interrupt signal.

TI/TP	0	1
Function	• **Level interrupt mode** The /IRQ pin is "L" immediately upon the occurrence of the timer interrupt (however, when TIE = 1) and the TF bit is "1" and the /IRQ is maintained at "L" until "0" is written to the TF bit.	• **Repeat interrupt mode (interval)** The /IRQ pin is "L" immediately upon the occurrence of the timer interrupt (however, when TIE = 1) and the TF bit is "1." Subsequently, the /IRQ pin enters high impedance and the TF bit is "1" is retained until "0" is written.

- Alarm-interrupt and a both signal of a timer-interrupt output it from /IRQ terminal.
- Even if the output of one interrupt is prohibition state, another interrupt occur and /IRQ terminal becomes LOW active if it is a state of the output permission.
- If the hardware interrupt is not being used, clear both the TIE and AIE bits to "0" and monitor both flag bits of AF and TF with the software, if necessary.
- Timer operation when the TI/TP bit is "0" is that the timer count register counts down and when the data reaches zero, the TE bit is cleared and the counter automatically stops. The value of the timer count register when the timer automatically stops is zero.
- Timer operation when the TI/TP bit is "1" is that the timer counter register counts down and when the data reaches zero, the timer counter register data is reloaded and count down begins again. This can be used as the interval timer (repeat mode).
- Reg-6 and 7 are read only, and can read the current value of the 8 bit pre-settable down counter. It cannot write the data.
- The pre-settable binary down-counter is updated when data is written to the Reg-4 and 5 registers. Data written to the Reg-4 and 5 registers is retained until it is written again.

- A timer interrupt does not occur from the /IRQ pin even if the data when the timer counter (Reg-4 and 5) reaches zero is set when the TE bit is "1."
- There is an error in time of 0 to –1 cycles of the selected source clock with 1 timer operation.
- Also, if the timer operation time is less than 1 cycle of the source clock, the count will may not be performed normally.
- Particularly, be aware that, when using minute update clock from clock register, for the source clock, there will be an error of a maximum of 60 seconds depending on the timing.
- The timer starts counting down from the edge of the rise of /WR corresponding to the TE bit in the time chart below, in the data write mode.
- When the TE bit is "0," the counter stops. When the TE bit is "1", the count starts.
- Using this function enables you to stop the counter part-way through timer operations, but when the timer starts, be aware that an error will occur at the maximum of the source clock period.
- For example, when source clock set to 1 minute.Timer does countdown and stops from TE=0 after 1 minute (maximum), and there is the case that interrupt occurs.
- When interrupt is unnecessary, set TIE bits adequately, and prohibit unprepared interrupt.



6-2-6. Digital offset registers (Bank2 Reg-0,1)

Address	Registers	bit 3	bit 2	bit 1	bit 0
0	Digital Offset	DT3	DT2	DT1	DT0
1		DT_ON	DT6	DT5	DT4

- When DT_ON="1", the digital pace adjustment function is enabled. When pace adjustment is enabled, the digital offset register digitally offsets the timekeeper according to the values set for the digital offset register by changing one second of the clock count every 10 seconds.
  Linking the digital pace adjustment operation with the status of the CS 1 pin will set the CDT_ON bit (Bank1,RegB)= "1".
  When disabled digital pace adjustment, set to DT_ON= "0."

[When a digital pace adjustment function is not used.]

At the time of initial setting, please clear a DT_ON bit to 0 by all means.

[When used a digital pace adjustment function.]

When it is used a digital pace adjustment function, please perform an initialization in a specified procedure in initial power on by all means.
Please set it according to a procedure of 7-1-2 "When used a digital pace adjustment function." of "7-1 Procedures for initially turning ON the power"

- The relationship between offset range and resolution

Offset range	Offset resolution	Offset timing
-195.20×10^{-6} to $+192.15 \times 10^{-6}$	3.05×10^{-6}	Every 10 seconds

The offset range is prescribed using frequency.

- The relationship of the DT bit and the digital offset value
  When the DT6 bit = "0", it is a positive offset, when the DT6 bit = "1", it is a negative offset.

Digital offset bits							Offset value
DT6	DT5	DT4	DT3	DT2	DT1	DT0	($\times 10^{-6}$)
0	1	1	1	1	1	1	+192.15
0	1	1	1	1	1	0	+189.10
			• • •				• • •
0	0	0	0	0	1	0	+6.10
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	0	-6.10
			• • •				• • •
1	0	0	0	0	0	1	-192.15
1	0	0	0	0	0	0	-195.20

The offset value is shift value for internal real crystal frequency.

- How to calculate the offset value

1) When the offset value is positive:

DT [6 to 0] = [Offset Value] / 3.05

However, decimals are discarded.

Example Calculation: When the offset value is +192.15 x 10^{-6}
DT[6 to 0] = 192.15 / 3.05 = 63 (dec)
= 0111111(bin) is set.

2) When the offset value is negative:

DT[6 to 0] = 128 - [Offset Value]/ 3.05
However, decimals are discarded.

Example Calculation: When the offset value is -158.6 $\times$ 10^{-6}
DT[6 to 0] = 128 - (158.6 / 3.05) = 76(dec)
= 1001100(bin) is set.

6-2-7. Control registers (Common to each Bank Reg-E and Reg-F)

Address	bit 3	Bit 2	bit 1	bit 0
E	TEST	TEMP		
F	Bank Sel 1	Bank Sel 0	STOP	BUSY/ADJ

- **TEST bit**: This bit is for our internal testing.

Note) The TEST bit is for our internal testing, so always set to **[TEST bit –"0"].**
Be careful not to mistakenly write a "1" when writing data to other bits of the same register.

- **TEMP** bit

When this bit is set to "1", the VTEMP pin outputs the temperature sensor voltage (analog).
When it is set to "0," the VTEMP pin is set to a high impedance. This bit is reset to "0" when the power is turned ON.

Note) Because the VTEMP pin is not set on the RTC-7301DG, always set to **[TEMP bit = "0"].**
When using with [TEMP bit = "1"], power current consumption will increase.

- **Bank Sel bit**

This bit specifies the Bank to access (read/write)

Bank Sel 1	Bank Sel 0	Access bank name
0	0	Bank0
0	1	Bank1
1	0	Bank2
1	1	Bank1

- **STOP** bit

When this bit is set to "1", the timekeeper is set to STOP and RESET from the 32 Hz divider counter.
This is used when setting the clock data.
The timekeeper starts when it is "0."
When setting the date and time data, wait a minimum of 122 μs after writing "1" to this bit, then set the date and time data.

- **BUSY/ADJ bit**

This bit is in BUSY mode when reading and in ADJ mode when writing. The data"1" can't set to this bit.
When "1" is written to this bit, the following operations will be performed between a minimum of 61 μs to a maximum of 183 μs.

- When the seconds display is 00 to 29 ——– Resets the counter up to 32 Hz for the seconds and sets the second digits to 00 seconds.
- When the seconds display is 30 to 59 ——–Resets the counter up to 32 Hz for the seconds and sets the second digits to 00 seconds and adds one minute to the minute digit. Later, this bit is automatically reset to "0" after 244 μs (Max.)

Because when BUSY = 1, the counter is updated, read out to the clock and calendar when BUSY = 1. If BUSY=0, it reads out stable data without updating the time at a maximum of 122 μs.
There is a possibility that unstable data will be read out while updating the clock if reading out when BUSY=1.
The following will occur when BUSY=1.

1) Normal 1 second digit raise is processed.
2) Processing of the ±30 second adjust (When writing 1 to the ADJ bit.)

- Function operation table

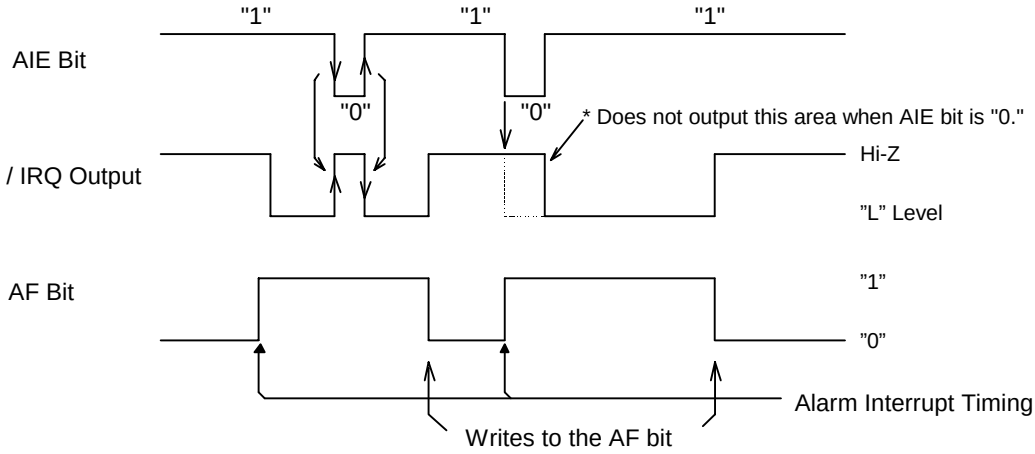
Bit		Function			
STOP	ADJ	Clock	Timer	Alarm	FOUT
0	0	Runs	Runs *1	Runs	Runs *1
0	1	30 adjust.	Runs *1	Runs	Runs *1
1	0	Stops	*1	Stops	*2
1	1	Stops&30 adjust.	*1	Stops	*2

∗1 : When source clock set to 1Hz or 1 minute, in a timing of digital adjustment or 30ADJ, a period of a timer and a period of FOUT change a little. When STOP-Bit is "1", operation is stops.

∗2 : When source clock is 1Hz,The output is halt.

6-2-8. Alarm interrupt

- The /IRQ pin becomes “L” output when AIE = 1 when the alarm is matched, and it becomes high impedance when AIE = 0.
- An alarm interrupt is output when a carry occurs in the seconds digit.



6-2-8-1. How to use the alarm

Alarms can be set for dates, days, hours, minutes and seconds. It is not possible to set a multiple of days at one time.
In order to avoid careless hardware interrupts while setting the alarms, we recommend setting both the AF and AIE bits to “0” first. Then, set the alarm data and clear the AF flag to zero once to ensure its initialization. When finished, set the AIE bit to “1”. If you do not wish to use the hardware interrupt, set the AIE bit to “0” and monitor the AF bit with the software as is necessary.

6-2-8-2. Example of use

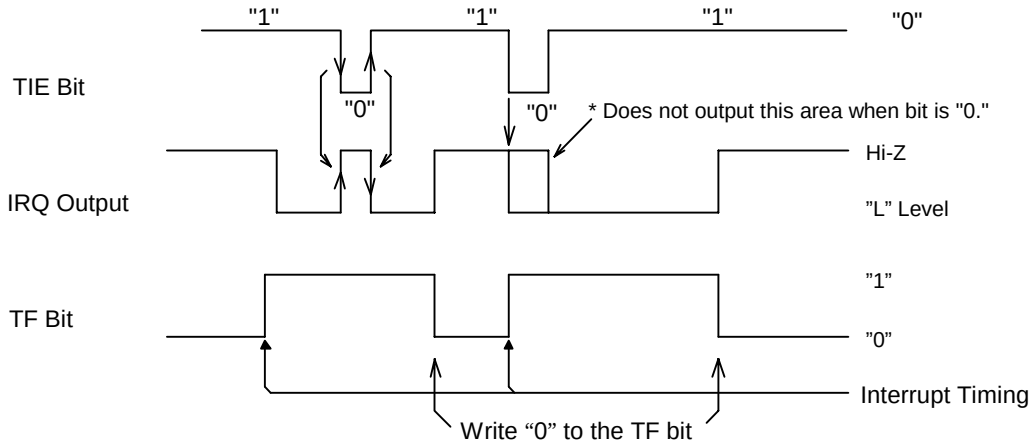
1) Issuing an alarm at 6:00 PM the next day:
- Write “0” to the AIE bit, and “0” to the AF bit.
- Write “1” to the AE bit of the date alarm.
- Acquire the current date in the Bank 0 register 6 to the day alarm register and write the next day’s data in the day setting table. (If the acquired data is 6/H (Saturday), write 0/H (Sunday).)
- Write “18h” to the hour alarm register.
- Write “00h” to the minute alarm register.
- Write “00h” to the second alarm register.
- Clear the AF bit to zero.
- Write “1” to the AIE bit.

2) Issuing an alarm at 6:00 AM every Sunday morning:
- Write “0” to the AIE bit, and “0” to the AF bit.
- Write “1” to the AE bit of the date alarm.
- Write “0h” to the day alarm register.
- Write “06h” to the hour alarm register.
- Write “00h” to the minute alarm register.
- Write “00h” to the second alarm register.
- Clear the AF bit to zero.
- Write “1” to the AIE bit.

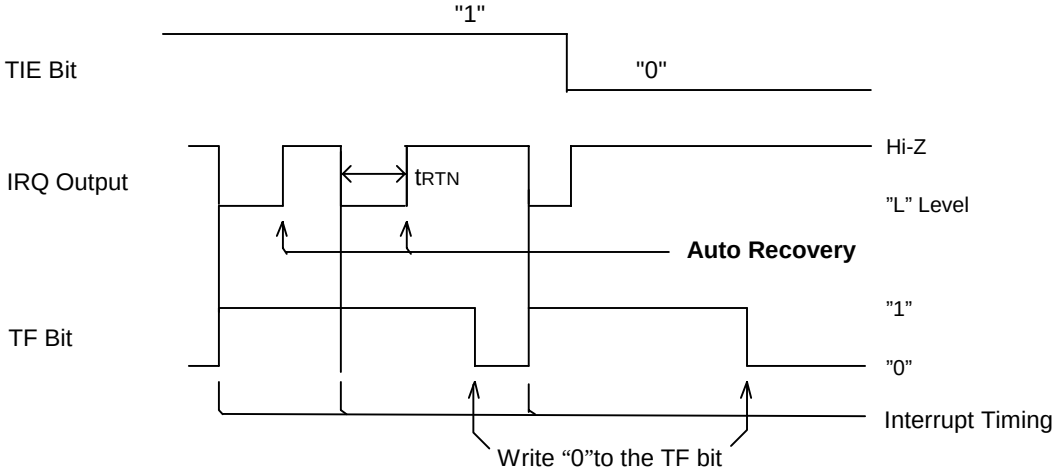
6-2-9. Timer interrupt

- Setting the TI / TP bit enables selection of the level interrupt or the repeat interrupt modes.

(1) Level interrupt mode (TI / TP = "0")
When an interrupt occurs, and TIE =1, the /IRQ pin outputs “L” and if TIE = 0, the /IRQ pin becomes high impedance.



(2) Repeat mode (TI/TP = "1")
When an interrupt occurs, and TIE = 1, the /IRQ pin outputs “L.”
When an interrupt occurs and TIE = 0, only the TF bit is “1” while the /IRQ pin stays at high impedance. This state is retained.



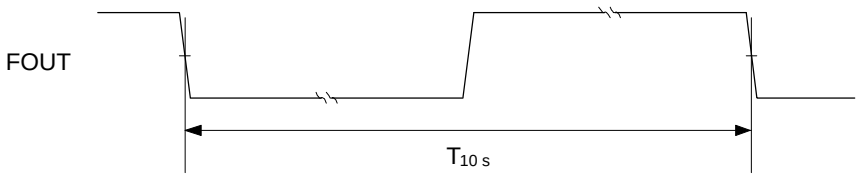
*Auto recovery time of the interrupt output in the repeat mode
The auto recovery time (tRTN) is different by the source clock specified by Bank1 Reg-D (FD3 and FD4 bits).

Relationship of each source clock and auto recovery times

Source clock	Auto recovery times (tRTN)
4069 Hz	0.122 ms
64 Hz	7.81 ms
Update in seconds	7.81 ms
Update in minutes	7.81 ms

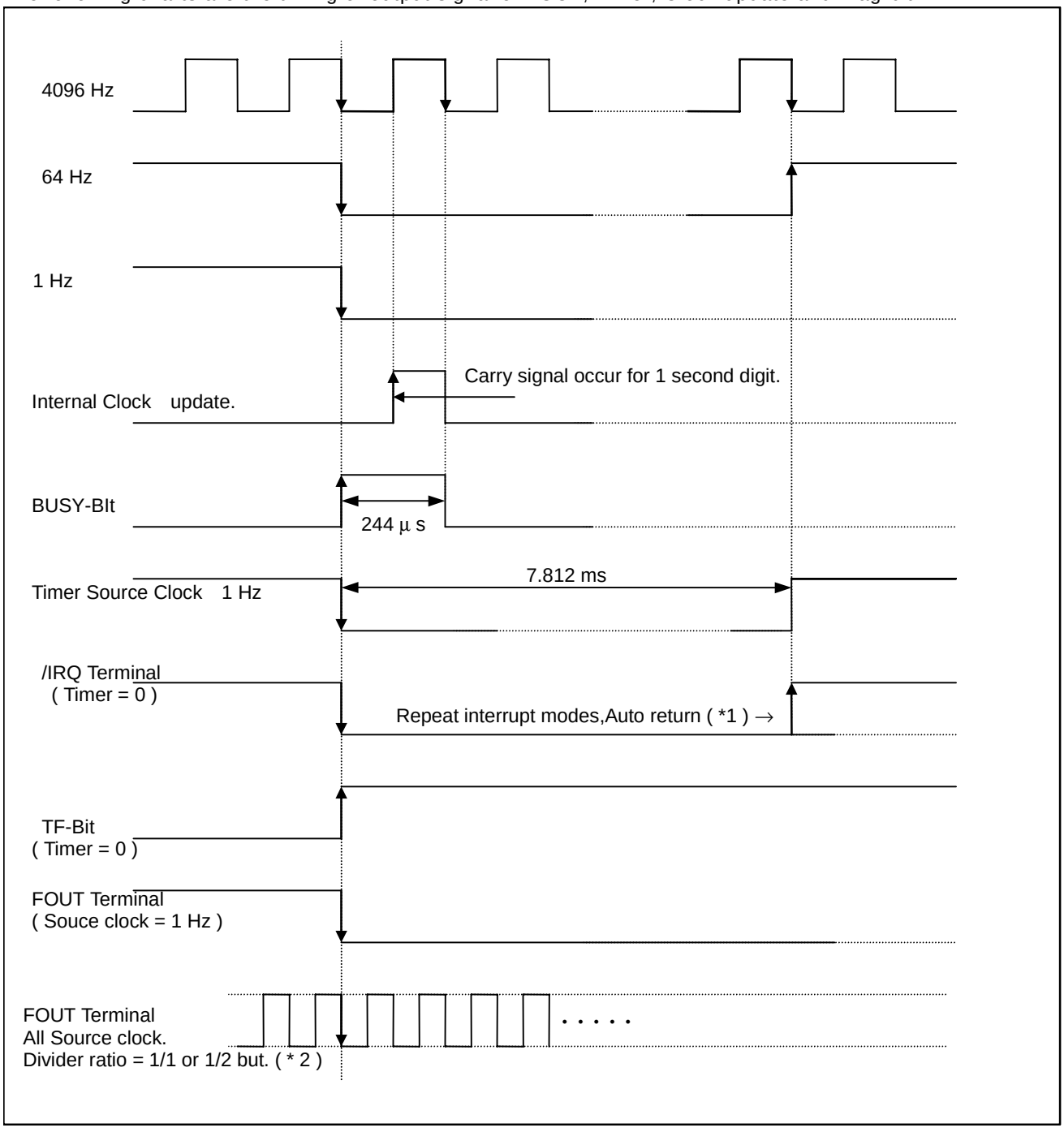
6-2-10. How to verify the digital offset

Because the digital offset is performed every 10 seconds, the results of the digital offset outputs a 10 s signal from the FOUT pin and this allows monitoring.



6-2-11. Timing of output signal.

The following charts are the timing of output signal of FOUT, Timer, Clock update and Flag-bit.



*1 When source clock is 4096 Hz, automatic return with 122 μs.

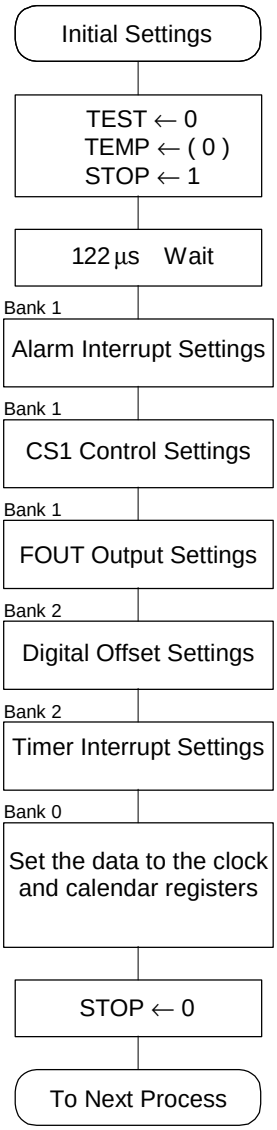
*2 FOUT is asynchronous to edge of 1Hz,
when source-clock is 32768 Hz, 1024 Hz, 32 Hz (excludes 1 Hz),
and Divider ratio set 1/3 or 1/5 only.

7. How to use

7-1. Procedures for initially turning ON the power[*1] (initial settings)

7-1-1. When a digital pace adjustment function is not used.

*1 : It is necessary to turn on the power to the RTC first. Once the initial settings for the RTC are completed, the contents are retained in a backup. Therefore when the system power is turned ON again later, perform the “Procedures for recovery from the backup” in the next section.



- Approximately 1 s is required from the start of the oscillator until the clock and calendar register is set.
- Mask the interrupt on the system side so that the CPU does not respond to careless interrupts from RTC when making the initial settings.
- Register table Bank switching is performed by writing to the Address F (common to all Banks) Bank Sel bit.
- Clear the TEST bit, stop the clock, and turn the temperature sensor OFF(your option).

- Set the alarm interrupt.
- When not using the alarm interrupt, set the AIE bit to "0."

- Set the CS1 link functions.
- When not using the CS1 link functions, set the CTEMP and CDT_ON bits to "0."

- Set the FOUT output. When set for 32.768 kHz output when the FCON pin is Low, setting of the register is unnecessary.
- When not using the FOUT output, set the FE bit to "0."

- Set the digital offset functions.
- When not using the digital offset functions, set the DT_ON bit to "0."

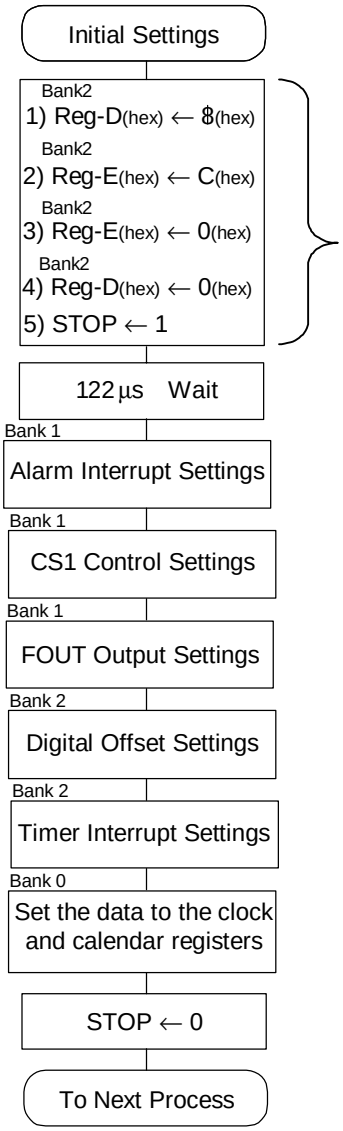
- Set the Timer interrupt.
- When not using the Timer interrupt, set the TE bit to "0."

- Set the current time.

- Start the clock.

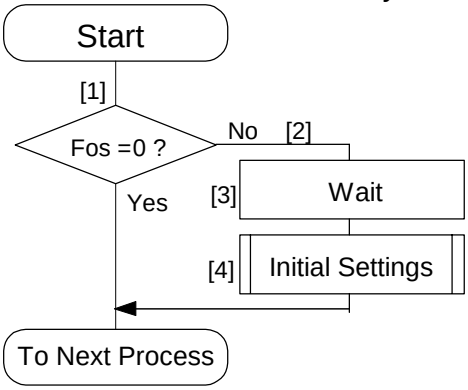
7-1-2. When used a digital pace adjustment function.

*1 : It is necessary to turn on the power to the RTC first. Once the initial settings for the RTC are completed, the contents are retained in a backup. Therefore when the system power is turned ON again later, perform the “Procedures for recovery from the backup” in the next section.



- Approximately 1 s is required from the start of the oscillator until the clock and calendar register is set.
- Mask the interrupt on the system side so that the CPU does not respond to careless interrupts from RTC when making the initial settings.
- Register table Bank switching is performed by writing to the Address F (common to all Banks) Bank Sel bit.
- Please obey faithfully this procedure for initialization of a circuit of digital pace adjustment function and must write data by all means.
- Set the alarm interrupt.
- When not using the alarm interrupt, set the AIE bit to "0."
- Set the CS1 link functions.
- When not using the CS1 link functions, set the CTEMP and CDT_ON bits to "0."
- Set the FOUT output. When set for 32.768 kHz output when the FCON pin is Low, setting of the register is unnecessary.
- When not using the FOUT output, set the FE bit to "0."
- Set the digital offset functions.
- When not using the digital offset functions, set the DT_ON bit to "0."
- Set the Timer interrupt.
- When not using the Timer interrupt, set the TE bit to "0."
- Set the current time.
- Start the clock.

7-2. Procedures for recovery from the backup



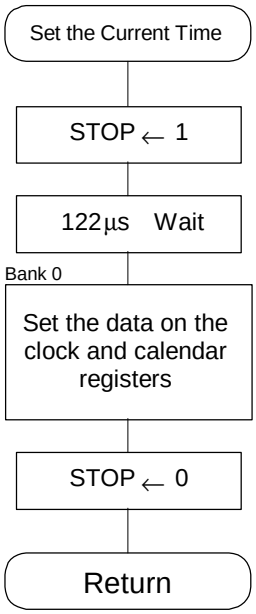
1)Check the Fos Flag.

2)If Fos is "1," the backup power voltage is reduced so the RTC data and contents of the register might have been lost, so it is necessary to redo the initial settings.

3)Please wait oscillation start up time.
In this waiting time, it is approximately 1 second.
See also specification of oscillation start up time(tSTA).

4)When the initial power-on occurs or if the Fos flag is 1, you must do initial settings to all registers.

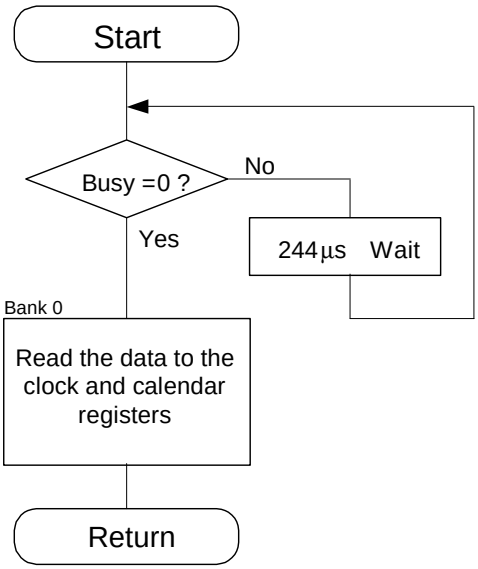
7-3. Writing to the clock and calendar (setting the current time)



- Stop the clock counter and reset the seconds digit by the STOP bit.
- Set the data on the clock and calendar registers.
- Start the clock.

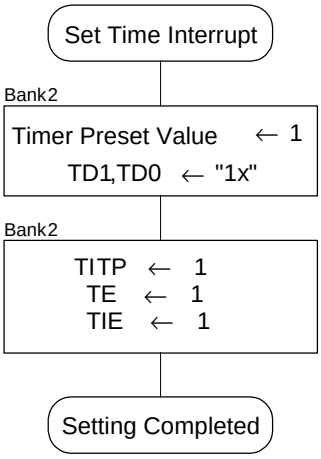
7-4. Reading out the clock and calendar

7-4-1. Reading out using the Busy bit check

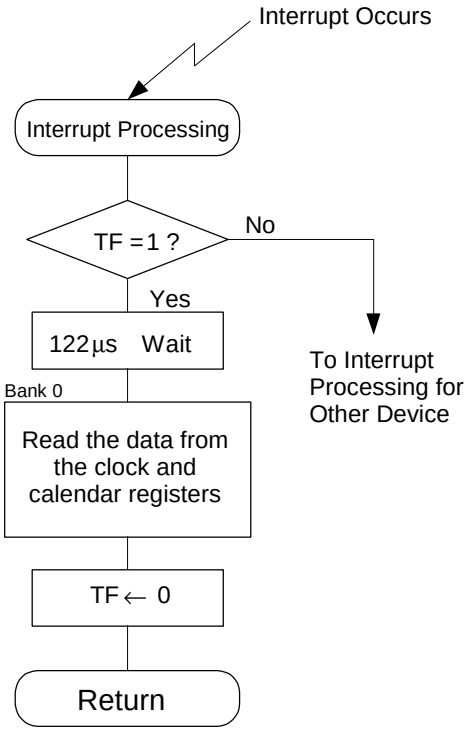


- Perform the Busy bit check.
- When the Busy bit is "1," the internal clock is being updating, so wait for the update to finish before reading out the data of the register.
- When the Busy bit is "0," the clock register update does not occur for 122 μs, so write the data of the register within 122 μs.

7-4-2. Read-out using an interrupt

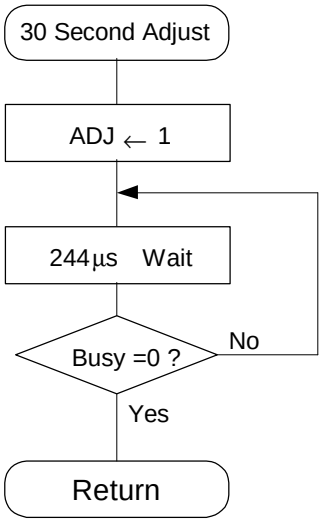


- Set 1 to the Timer preset value.
- Set "10" or "11" to TD1 and TD0.
  ("10": Update in seconds; "11": Update in minutes)
- Enable the Timer interrupt using the repeat mode.



- Check the TF flag, and verify that it is a Timer interrupt.
- Read the data from the clock and calendar registers.
- Clear the TF flag.

7-5. 30 second adjust *2



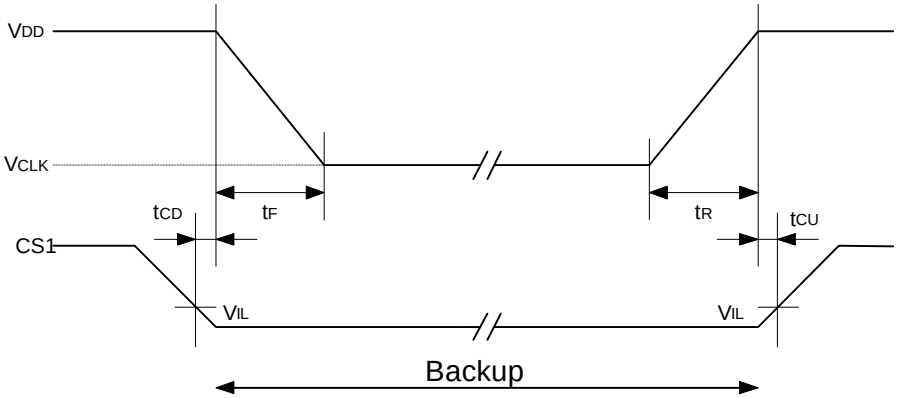
- Set the ADJ bit.
- Wait for the 30 second adjust processing to be completed.
- If the Busy flag is "0," the 30 second adjust process is completed.

*2 : When using the 30 second adjust function, if the second digits are 00 to 29 seconds, adjust the second digits to 00 seconds
and when the second digits are 30 to 59 seconds, plus 1 minute to minute digit, and adjust the second digits to 00 seconds.
Clock data can adjust to the just exact time by this function with the time signal.

Precautions
The crystal oscillator can be damaged by excessive shocks.
If, the crystal oscillator stops oscillating, the clock function will stop.
If the crystal oscillator is oscillating, the Busy bit will automatically recover in 244 µs,
but if oscillation stops, automatic recovery will not occur.
Therefore, in this state, there is the possibility that the Busy bit will not be able to escape the check loop and the system will hang-up.

As a fail-safe,
when it does not escape from the loop, as between 0.5 ms to 1 ms, we recommend jump to timeout procedure, to escape from the eternal loop to enable the processing of any errors.

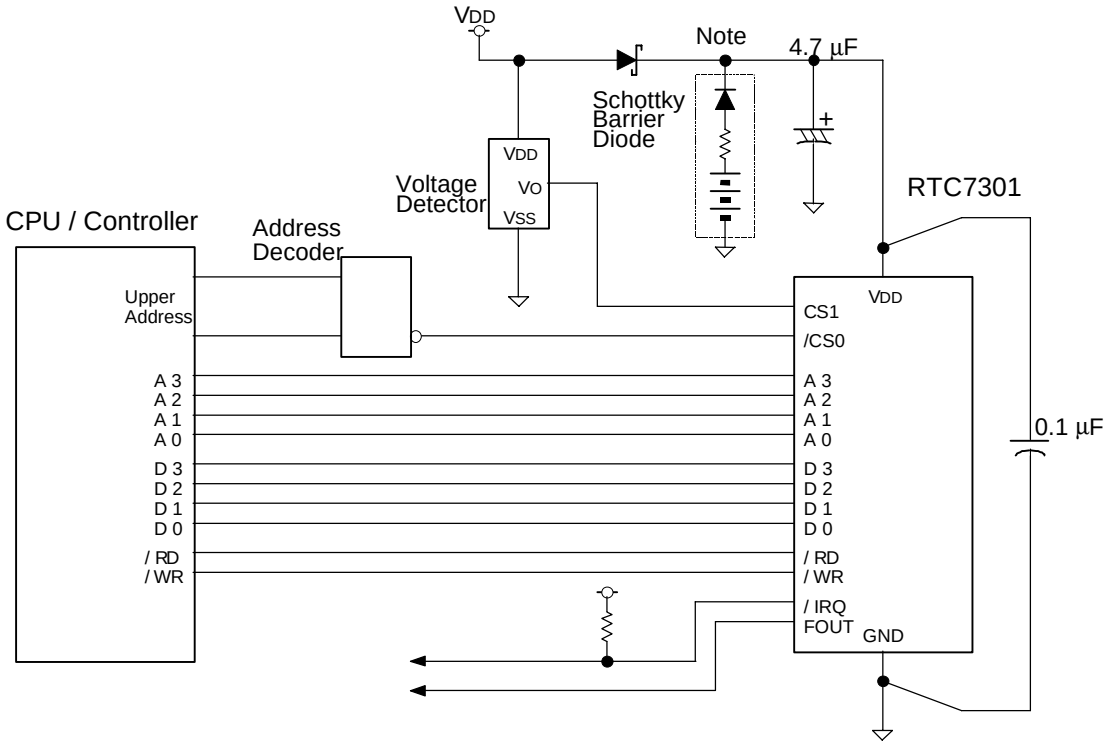
8. Shifting to backup and recovering



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CS1 time before power fall	tCD	-	0			µs
Power fall time	tF	-	2			µs / V
Power rise time	tR	-	1			µs / V
CS1 time after power rise	tCU	-	0			µs

*When shifting to backup, the CS1 should be at Low level and RTC should be in a non-selectable state before switching the power supply.
Note: At the time of initial power-on, keep a level of CS 0 in High. Please use this device after making CS0 a High level once after power-on when you cannot but start CS0 with a Low level.

9. External connection example

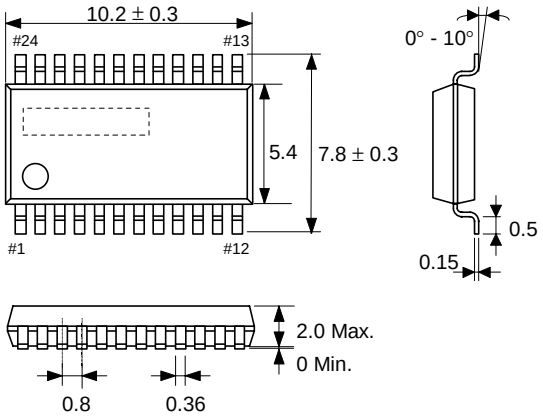


Note : Use a secondary battery or a lithium battery. If using a secondary battery, a diode is unnecessary. If using a lithium battery, a diode is necessary. Talk with your battery dealer regarding the details of the values of resistors.

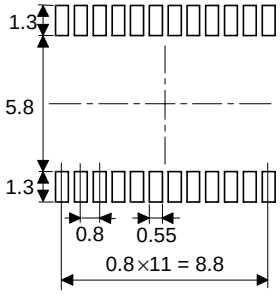
10. External diagram

RTC - 7301 SF (SSOP-24pin)

- External dimensions



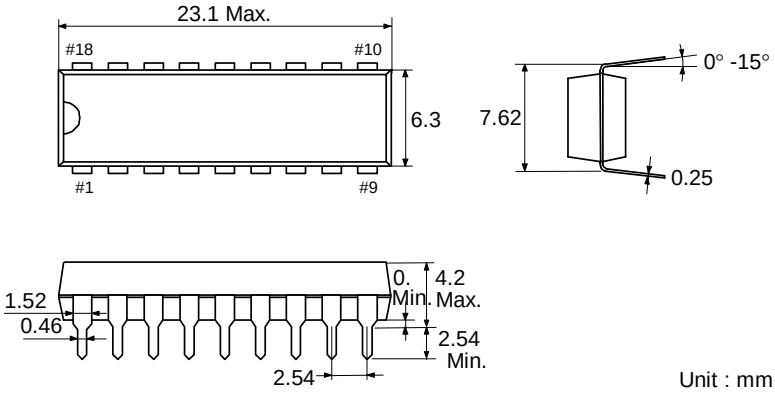
- Recommended soldering pattern



Unit : mm

* The cylinder of the crystal oscillator can be seen in this area (back and front), but it has no effect on the performance of the device.

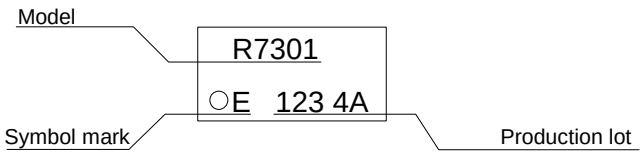
RTC - 7301 DG (DIP-18pin)



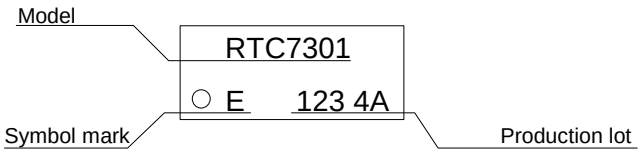
Unit : mm

11. Marking layout

RTC - 7301 SF (SSOP-24pin)



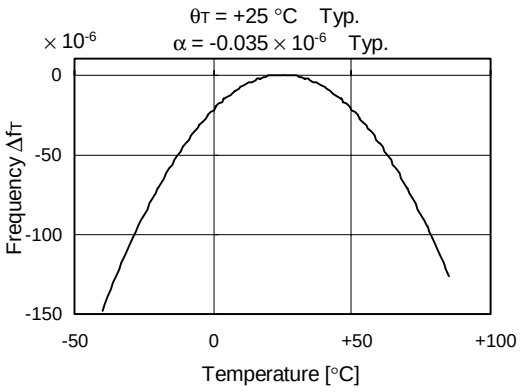
RTC - 7301 DG (DIP-18pin)



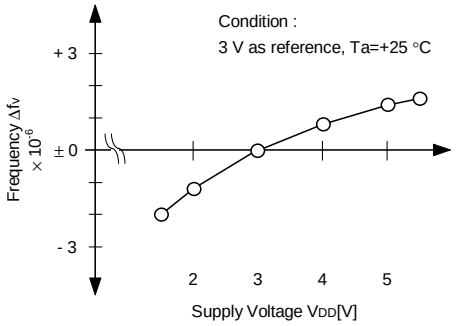
* Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

12. Reference data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha (\theta_T - \theta_X)^2$

Δf_T		: Frequency deviation in any temperature
α	$1 / °C^2$)	: Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6} / °C^2$
θ_T	°C)	: Ultimate temperature (+25±5 °C)
θ_X	°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage.
$\Delta f/fo$	: Frequency precision
Δf_T	: Frequency deviation in any temperature.
Δfv	: Frequency deviation in any voltage.

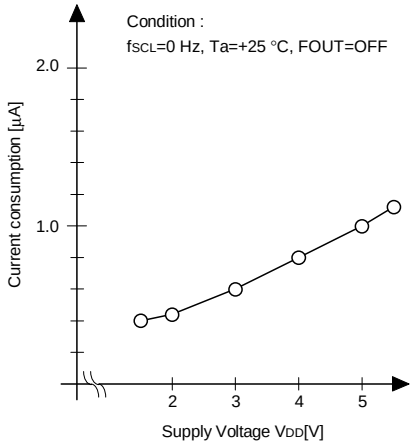
3. How to find the date difference

Date Difference = $\Delta f/f \times 86400$(s)

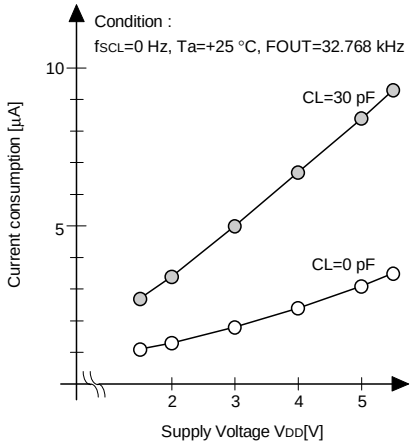
* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) Current consumption when non-accessed (i) when FOUT=OFF



(3-2) Current consumption when non-accessed (ii) when FOUT=32.768 kHz



13. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 µF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

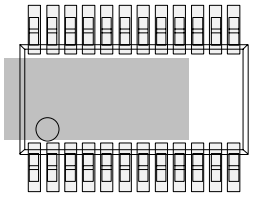
(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example GND Pattern	Fig. 2: Soldering Conditions of SMD Products Air Reflow Profile

Fig. 1 : Example GND Pattern

RTC - 7301 SF (SSOP-24pin)



RTC - 7301 DG (DIP-18pin)

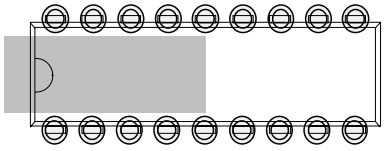
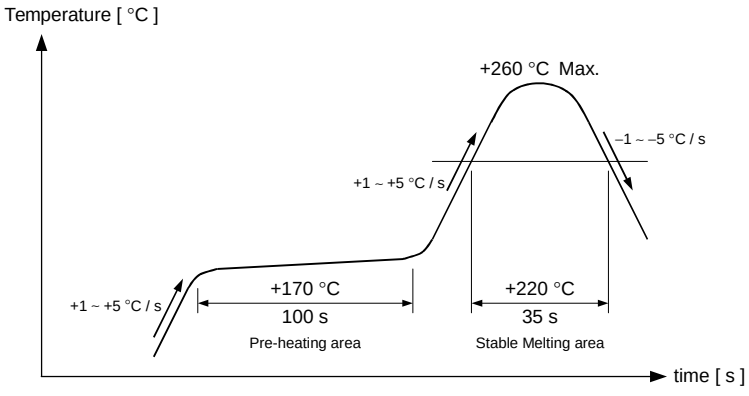


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.
(SMD Products)



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