MJB5742T4G

NPN Silicon Power Darlington Transistors

The Darlington transistors are designed for high−voltage power switching in inductive circuits.

Features

- These Devices are Pb−Free and are RoHS Compliant

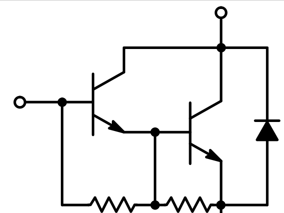
Applications

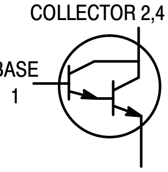
- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

ON Semiconductor®

http://onsemi.com

POWER DARLINGTON TRANSISTORS
8 AMPERES, 400 VOLTS
100 WATTS





MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage		$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage		V_{CEV}	800	Vdc
Emitter−Base Voltage		V_{EB}	8	Vdc
Collector Current	– Continuous – Peak (Note 1)	I_C I_{CM}	8 16	Adc
Base Current	– Continuous – Peak (Note 1)	I_B I_{BM}	2.5 5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	W W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	100 0.8	W W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	°C

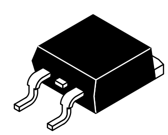
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

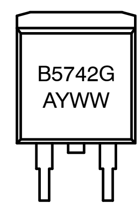
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MARKING DIAGRAM



D²PAK
CASE 418B
STYLE 1



B5742	=	Specific Device Code
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJB5742T4G	D²PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector−Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)	I_{EBO}	–	–	75	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 7			
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 4 Adc, V_{CE} = 5 Vdc)	h_{FE}	50 200	100 400	– –	–
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)	$V_{CE(sat)}$	– – –	– – –	2 3 2.2	Vdc
Base−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)	$V_{BE(sat)}$	– – –	– – –	2.5 3.5 2.4	Vdc
Diode Forward Voltage (Note 3) (I_F = 5 Adc)	V_f	–	–	2.5	Vdc

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6 A I_{B1} = I_{B2} = 0.25 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.04	–	μs
Rise Time		t_r	–	0.5	–	μs
Storage Time		t_s	–	8	–	μs
Fall Time		t_f	–	2	–	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(pk)}$ = 6 A, $V_{CE(pk)}$ = 250 Vdc I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	4	–	μs
Crossover Time		t_c	–	2	–	μs

2. Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.
3. The internal Collector−to−Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

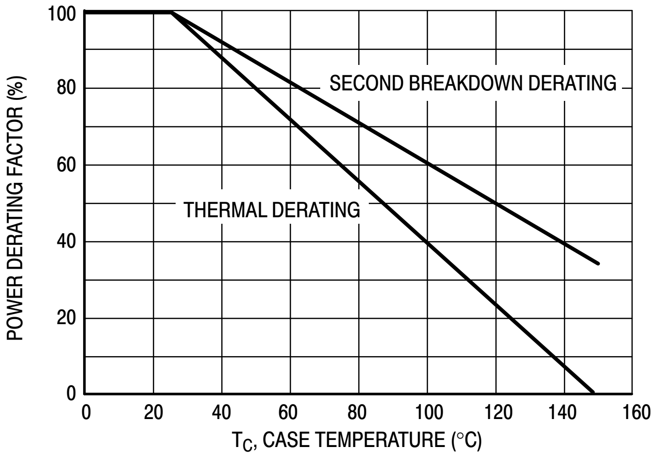


Figure 1. Power Derating

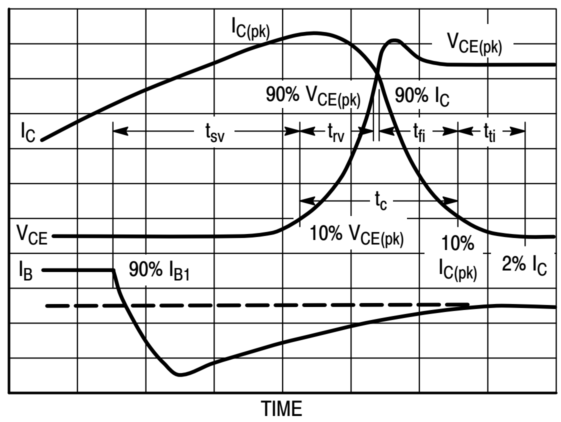


Figure 2. Inductive Switching Measurements

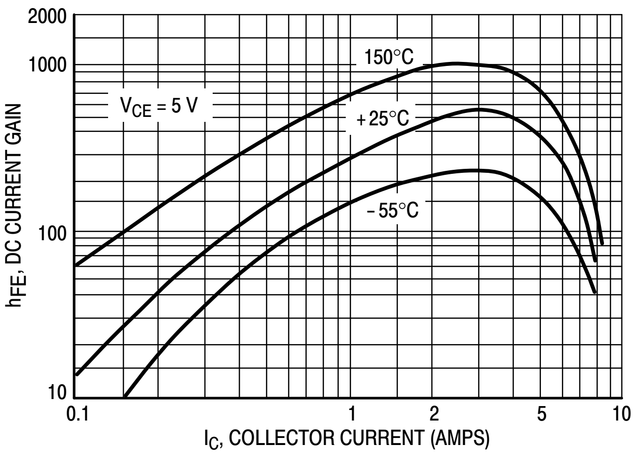


Figure 3. DC Current Gain

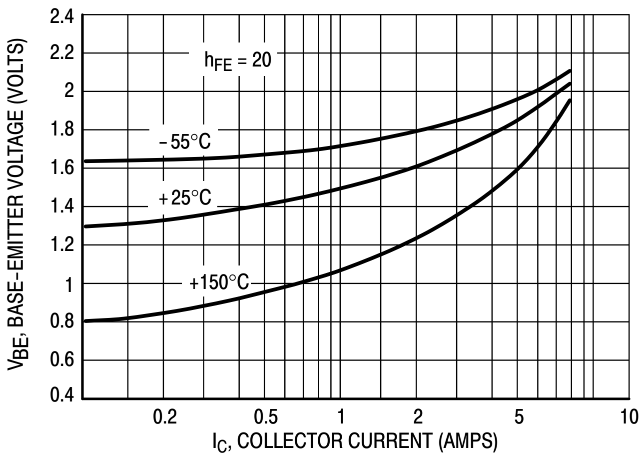


Figure 4. Base−Emitter Voltage

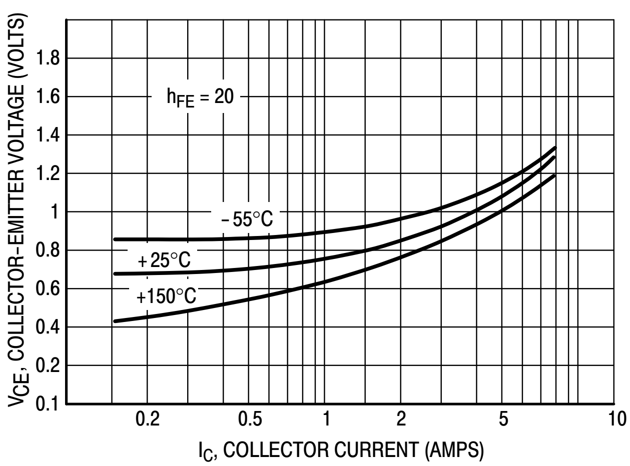
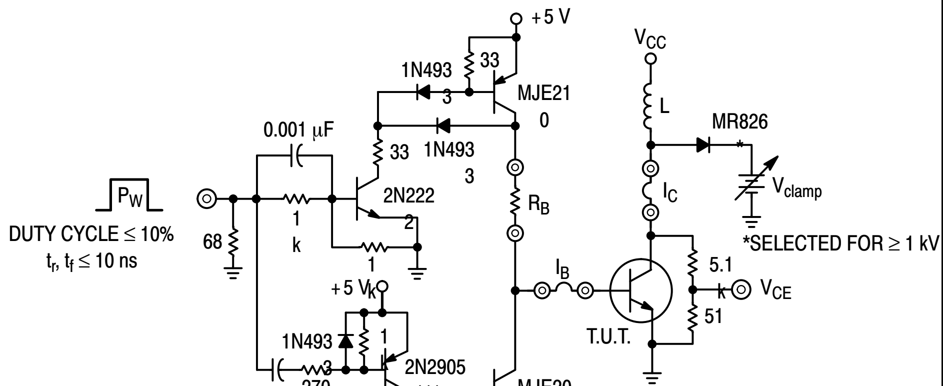
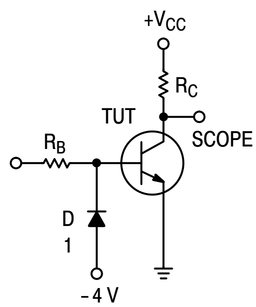
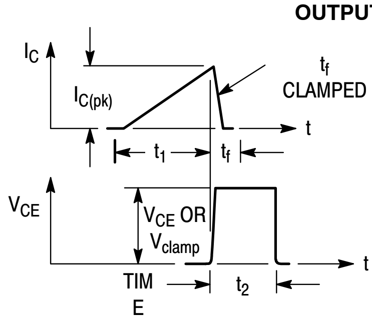


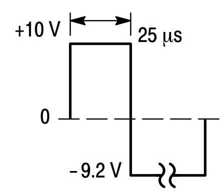
Figure 5. Collector−Emitter Saturation Voltage

Table 1. Test Conditions for Dynamic Performance

<table>
<tr><th></th><th>REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>TEST CIRCUITS</td><td>


NOTE:
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}
</td><td>


</td></tr>
<tr><td>CIRCUIT VALUES</td><td>
COIL DATA:
FERROXCUBE CORE #6656
FULL BOBBIN (~16 TURNS) #16
GAP FOR 200 μH/20 A
L_{coil} = 200 μH
V_{CC} = 30 V
$V_{CE(pk)}$ = 250 Vdc
$I_{C(pk)}$ = 6 A
</td><td>
V_{CC} = 250 V
D1 = 1N5820 OR EQUIV.
</td></tr>
<tr><td>TEST WAVEFORMS</td><td>
OUTPUT WAVEFORMS


t_1 ADJUSTED TO OBTAIN I_C
$t_1 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{clamp}}$
TEST EQUIPMENT
SCOPE-TEKTRONICS
475 OR EQUIVALENT
</td><td>


t_r, t_f < 10 ns
DUTY CYCLE = 1%
R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C
</td></tr>
</table>

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

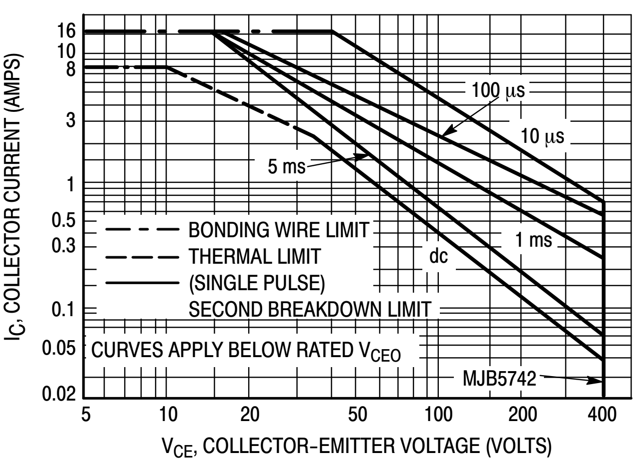


Figure 6. Forward Bias Safe Operating Area

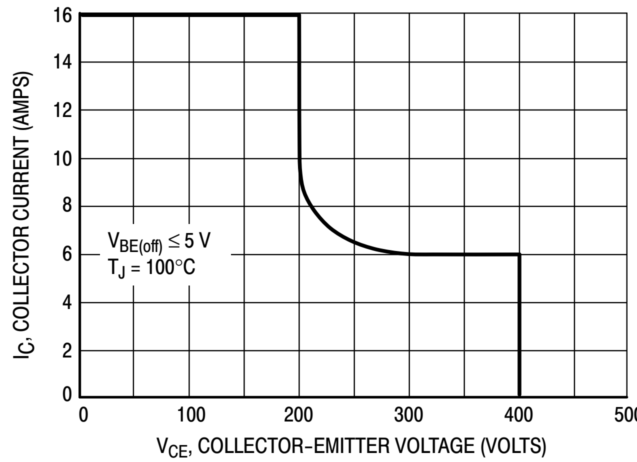


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

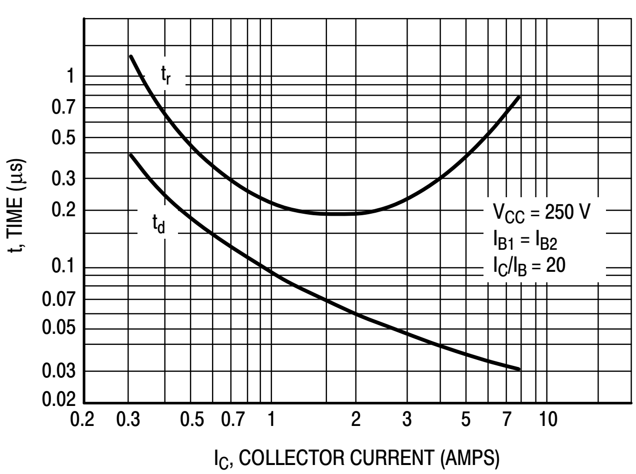


Figure 8. Turn−On Time

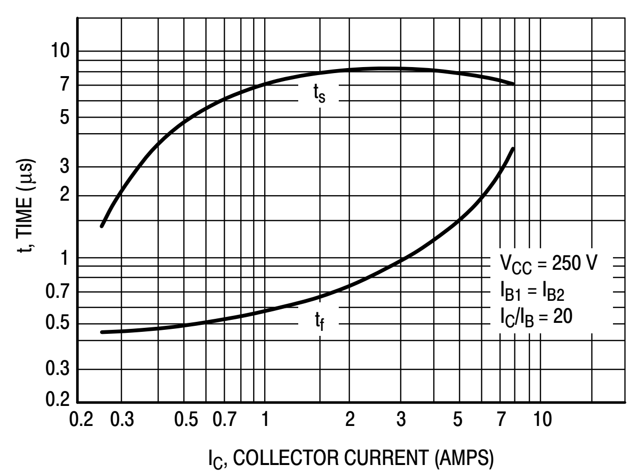
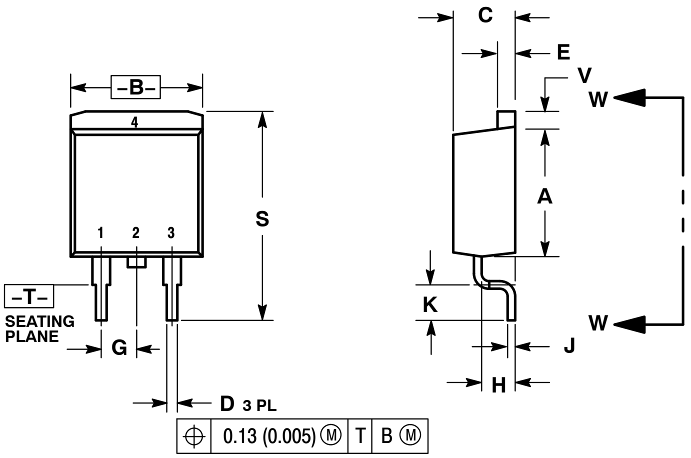


Figure 9. Turn−Off Time

PACKAGE DIMENSIONS

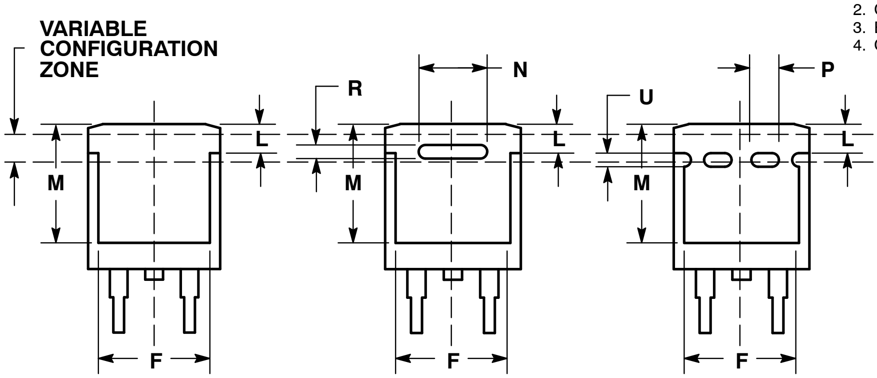
D²PAK 3
CASE 418B−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

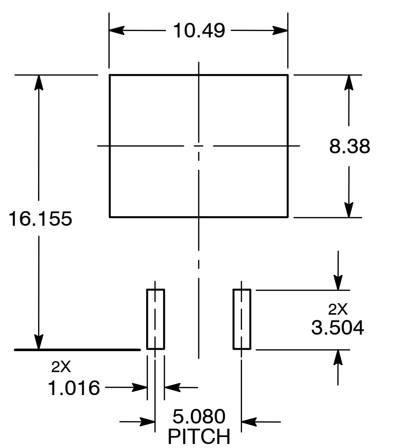
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



VIEW W−W 1 **VIEW W−W 2** **VIEW W−W 3**

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative