



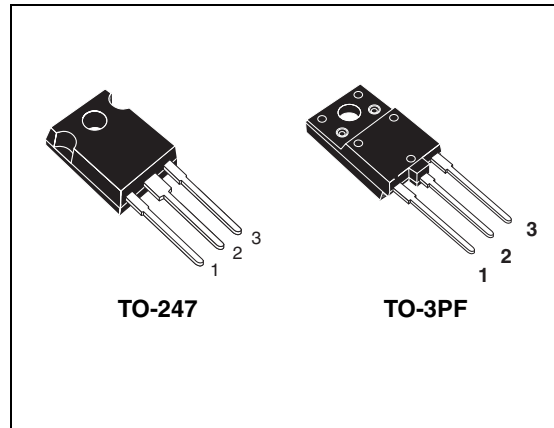
STW60N65M5 STFW60N65M5

N-channel 650 V, 0.049 Ω , 46 A MDmesh™ V Power MOSFET
in TO-247, TO-3PF

Features

Order codes	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STFW60N65M5 STW60N65M5	710 V	< 0.059 Ω	46 A

- Worldwide best $R_{DS(on)}$ * area amongst the silicon based devices
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



Application

Switching applications

Description

The devices are N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

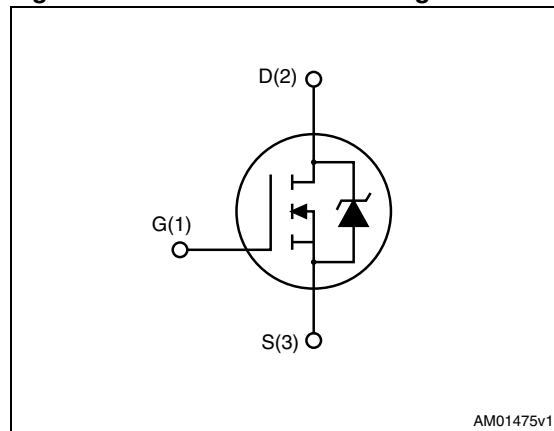


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFW60N65M5 STW60N65M5	60N65M5	TO-3PF TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-247	TO-3PF	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	46		A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	29		A
$I_{DM}^{(1)}$	Drain current (pulsed)	184		A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	255	79	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	12		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1400		mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C=25\text{ °C}$)		3500	V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 46\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 400\text{ V}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-247	TO-3PF	
$R_{thj-case}$	Thermal resistance junction-case max	0.49	1.58	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 23\text{ A}$		0.049	0.059	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	6810	-	pF
C_{oss}	Output capacitance			141		pF
C_{rss}	Reverse transfer capacitance			6.2		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$	-	480	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			140		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 23\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 17)	-	139	-	nC
Q_{gs}	Gate-source charge			34		nC
Q_{gd}	Gate-drain charge			52		nC

- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_d (V)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 30$ A,		90		ns
t_r (V)	Voltage rise time	$R_G = 4.7$ Ω , $V_{GS} = 10$ V	-	11	-	ns
t_f (I)	Current fall time	(see Figure 18)		13		ns
t_c (off)	Crossing time	(see Figure 21)		16		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		46	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				184	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 46$ A, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 46$ A, $di/dt = 100$ A/ μ s		448		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V (see Figure 21)	-	10		μ C
I_{RRM}	Reverse recovery current			45		A
t_{rr}	Reverse recovery time	$I_{SD} = 46$ A, $di/dt = 100$ A/ μ s		534		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C	-	14		μ C
I_{RRM}	Reverse recovery current	(see Figure 21)		52		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-3FP

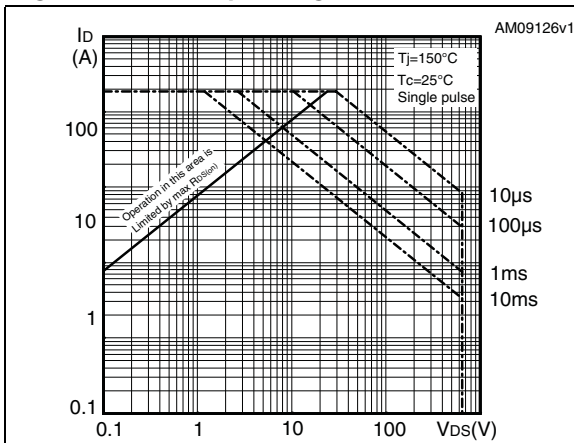


Figure 3. Thermal impedance for TO-3FP

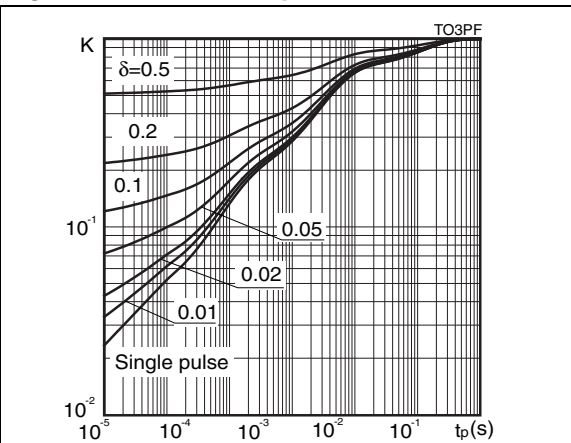


Figure 4. Safe operating area for TO-247

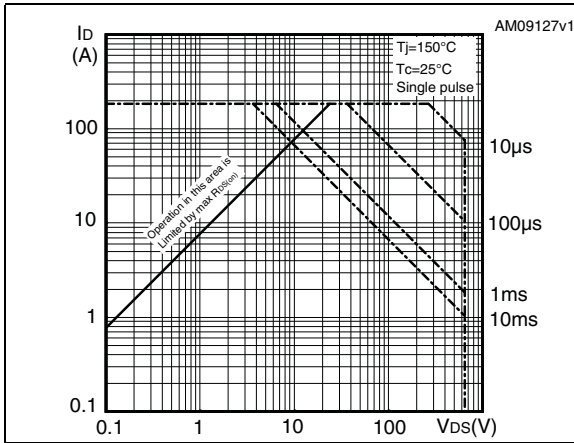


Figure 5. Thermal impedance for TO-247

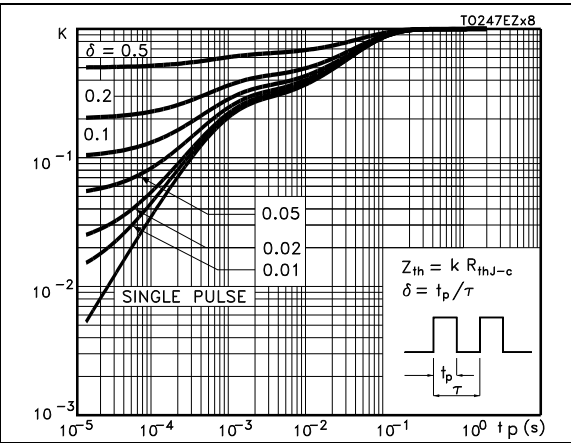


Figure 6. Output characteristics

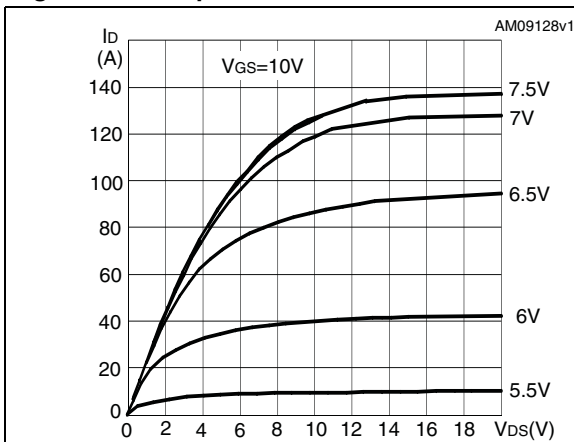


Figure 7. Transfer characteristics

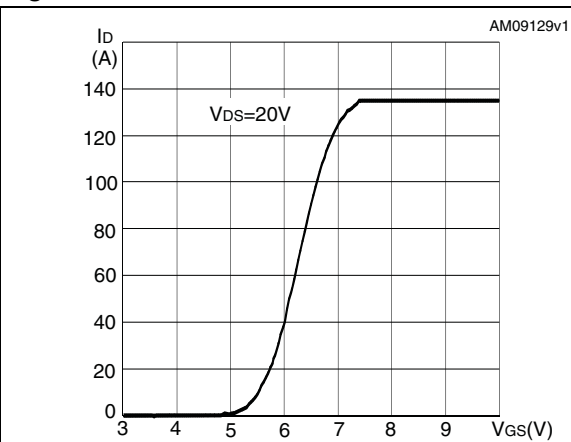


Figure 8. Gate charge vs gate-source voltage **Figure 9. Static drain-source on resistance**

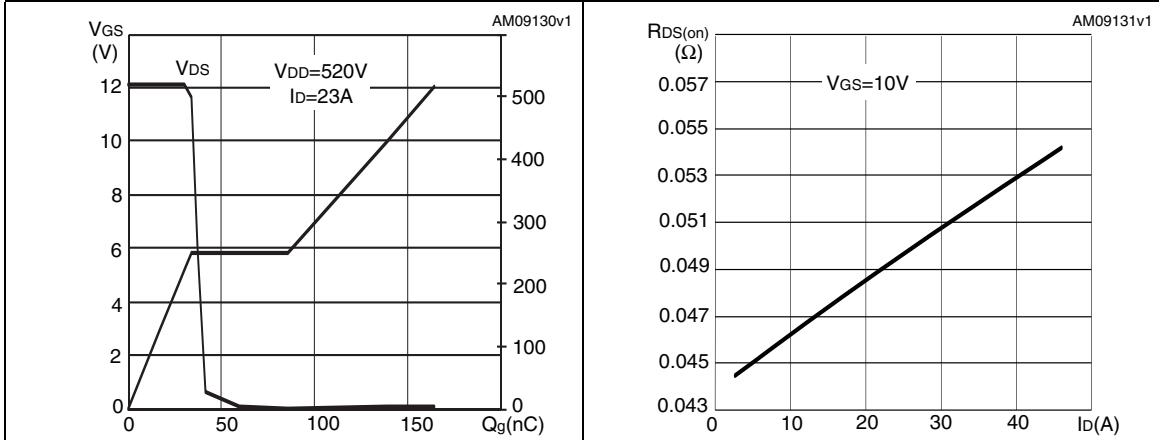


Figure 10. Capacitance variations **Figure 11. Output capacitance stored energy**

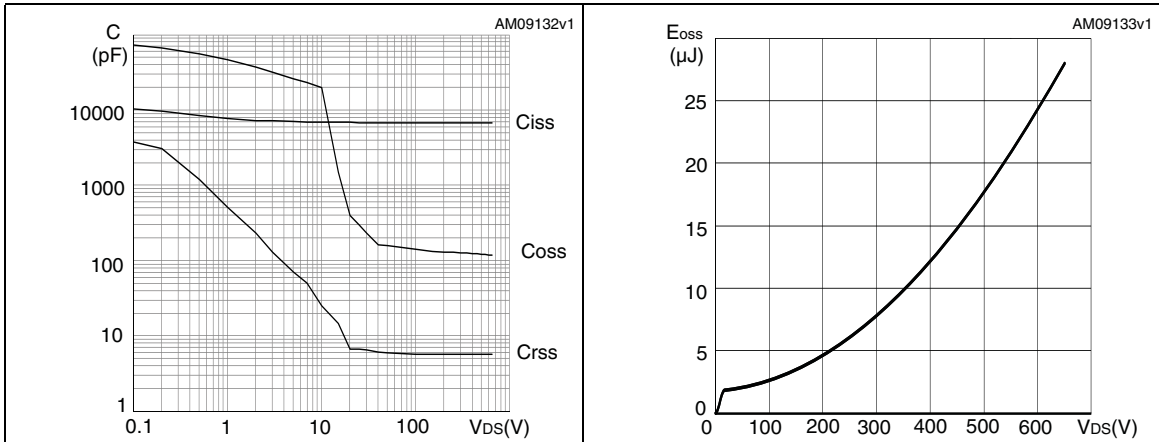


Figure 12. Normalized gate threshold voltage vs temperature **Figure 13. Normalized on resistance vs temperature**

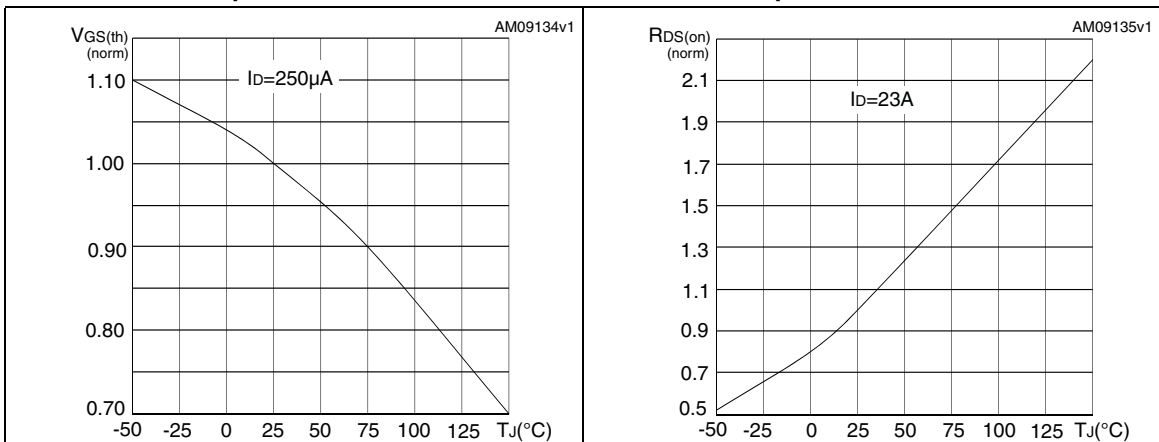
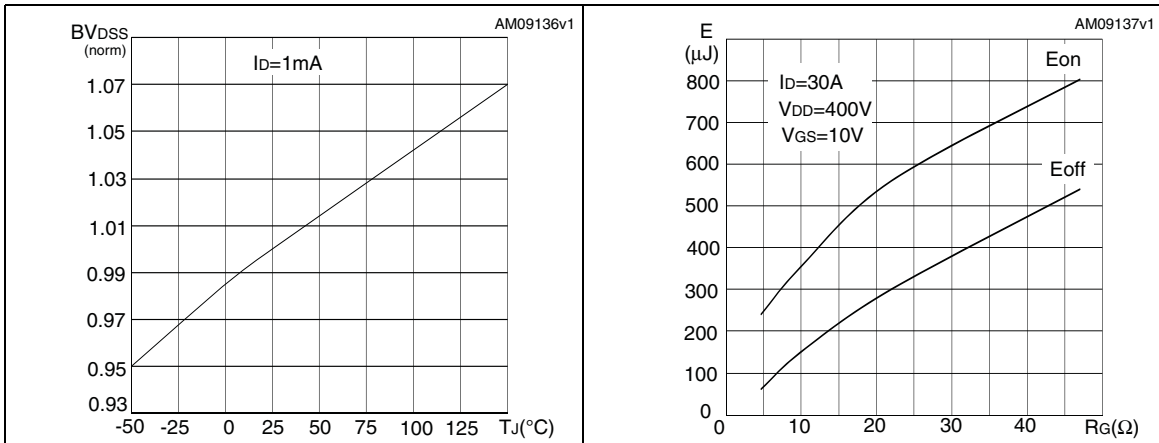


Figure 14. Normalized B_{VDSS} vs temperature Figure 15. Switching losses vs gate resistance (1)



1. E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 16. Switching times test circuit for resistive load

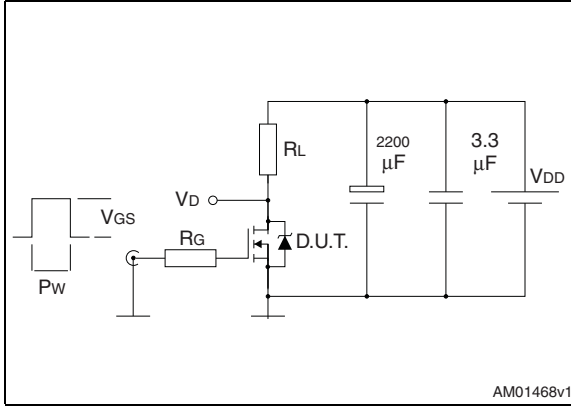


Figure 17. Gate charge test circuit

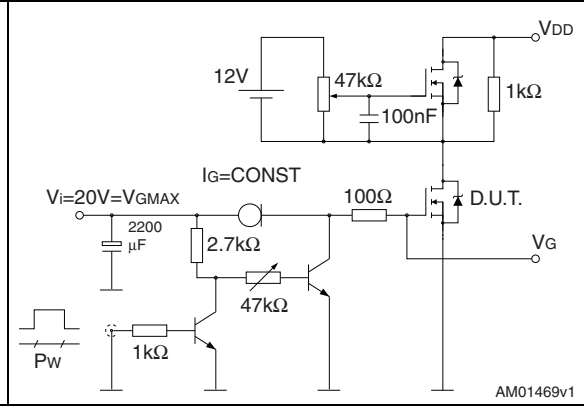


Figure 18. Test circuit for inductive load switching and diode recovery times

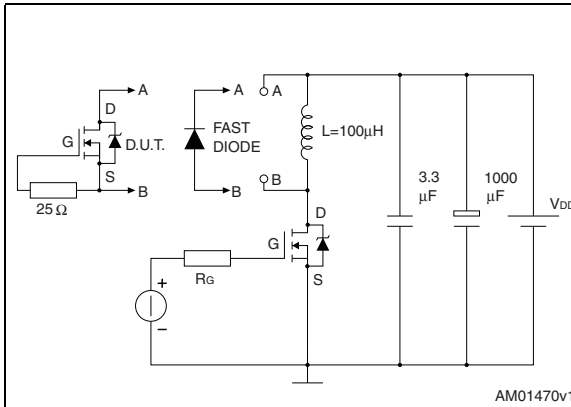


Figure 19. Unclamped inductive load test circuit

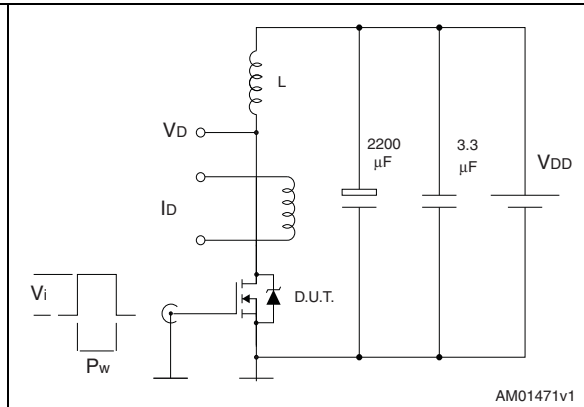


Figure 20. Unclamped inductive waveform

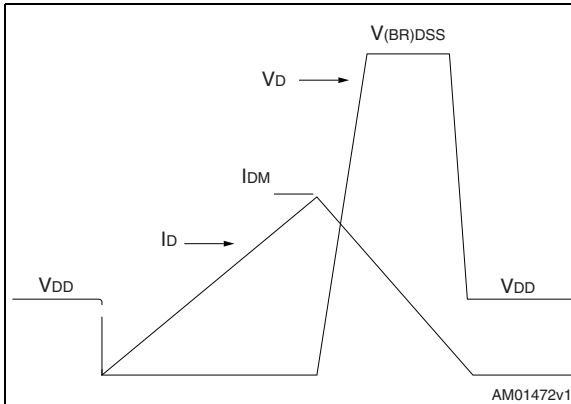
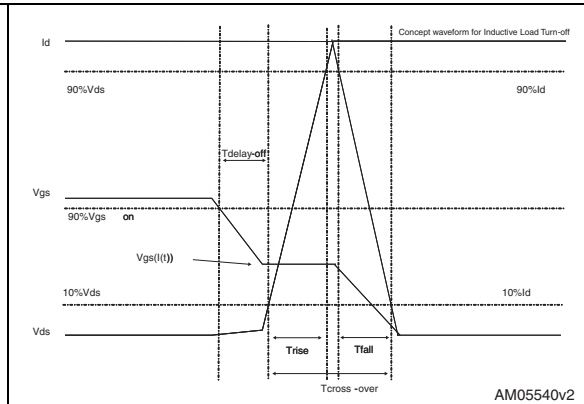


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

Figure 22. TO-3PF drawing

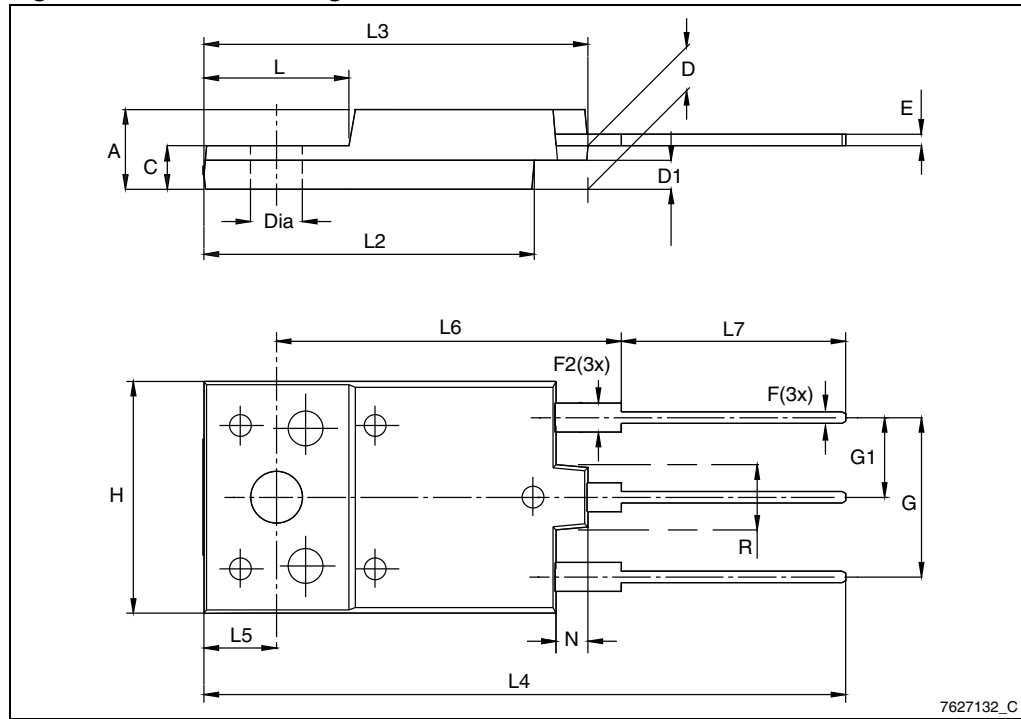
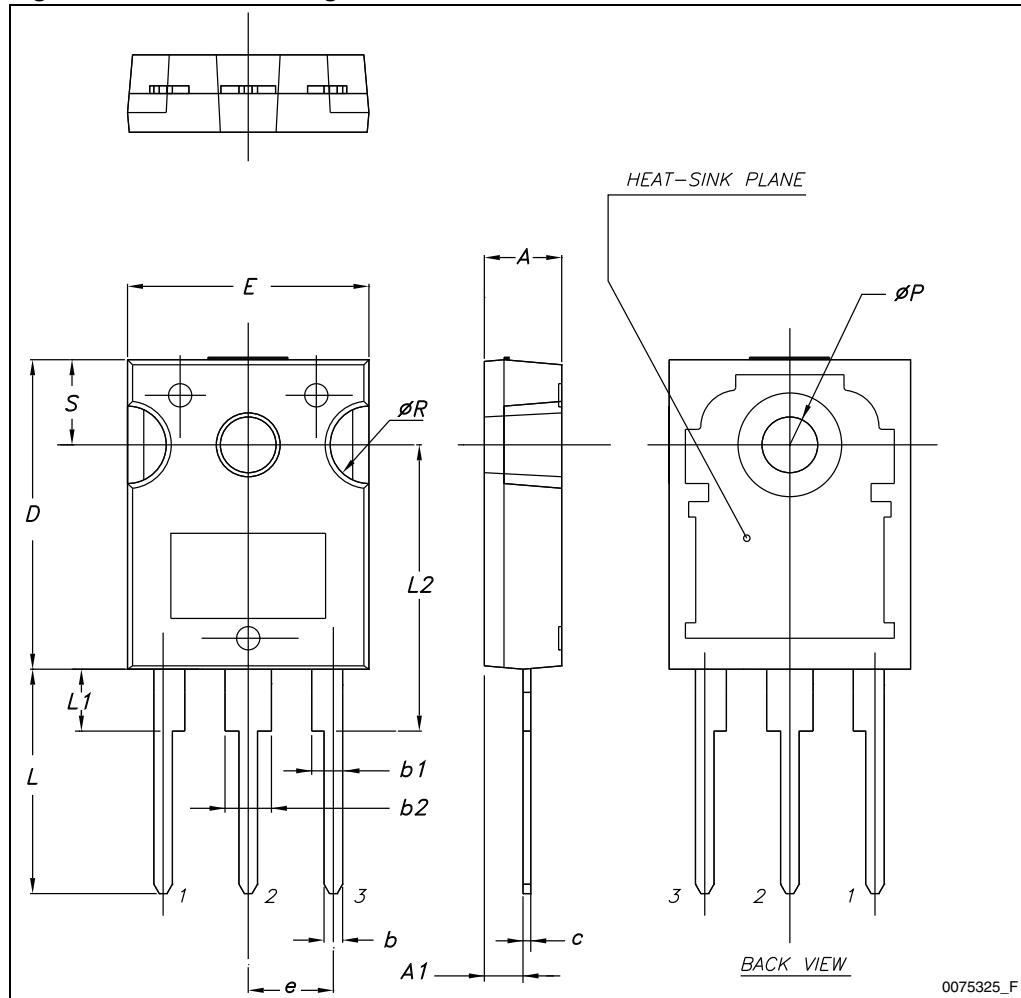


Table 9. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 23. TO-247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Nov-2010	1	First release.
05-May-2011	2	Document status promoted from preliminary data to datasheet.

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