



STH210N75F6-2

N-channel 75 V, 0.0022 Ω , 180 A H²PAK-2
STripFET™ VI DeepGATE™ Power MOSFET

Preliminary data

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STH210N75F6-2	75 V	< 0.0028 Ω	180 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Application

Switching applications

Description

This product is a 75 V N-channel STripFET™ VI Power MOSFET based on the ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

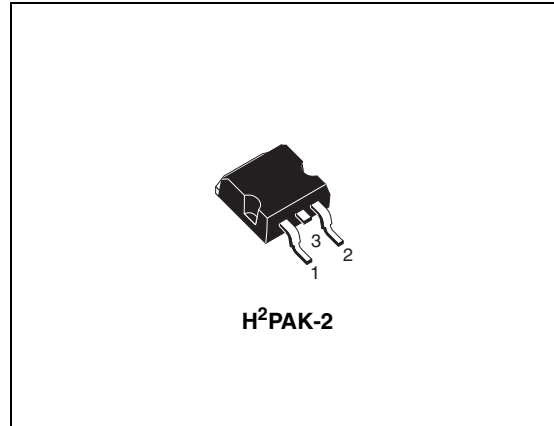


Figure 1. Internal schematic diagram

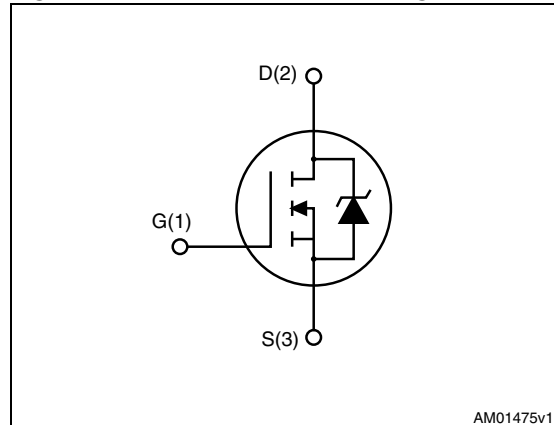


Table 1. Device summary

Order code	Marking	Package	Packaging
STH210N75F6-2	210N75F6	H ² PAK-2	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	150	A
$I_{DM}^{(1)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Current limited by package.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	75			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	For H ² PAK-2 $V_{GS} = 10\text{ V}$, $I_D = 90\text{ A}$		2.2	2.8	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	11800	-	pF
C_{oss}	Output capacitance			1060		pF
C_{rss}	Reverse transfer capacitance			394		pF
Q_g	Total gate charge	$V_{DD} = 37.5\text{ V}$, $I_D = 120\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)	-	171	-	nC
Q_{gs}	Gate-source charge			50		nC
Q_{gd}	Gate-drain charge			36		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{ V}$, $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)	-	34	-	ns
t_r	Rise time			70		ns
$t_{d(off)}$	Turn-off-delay time			154		ns
t_f	Fall time			71		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 180 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 4)	-	60 144 4.8		ns nC A

1. Current limited by package.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

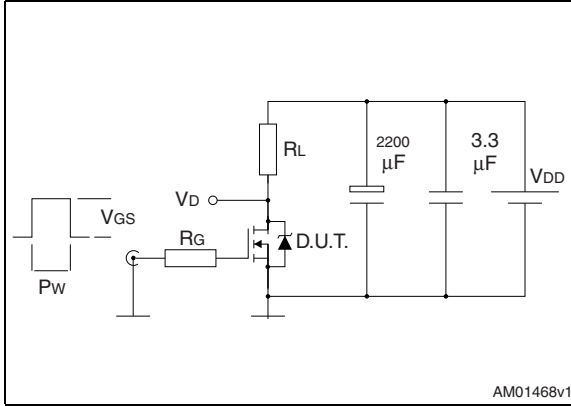


Figure 3. Gate charge test circuit

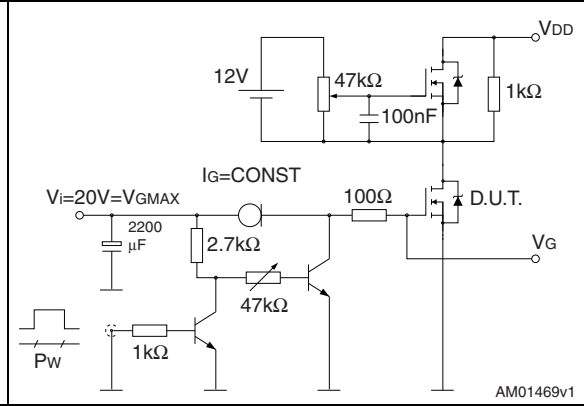


Figure 4. Test circuit for inductive load switching and diode recovery times

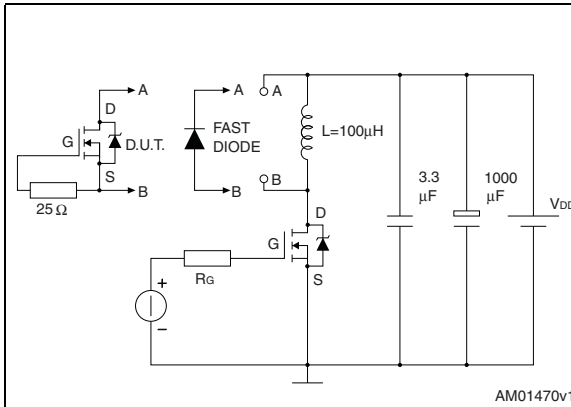


Figure 5. Unclamped inductive load test circuit

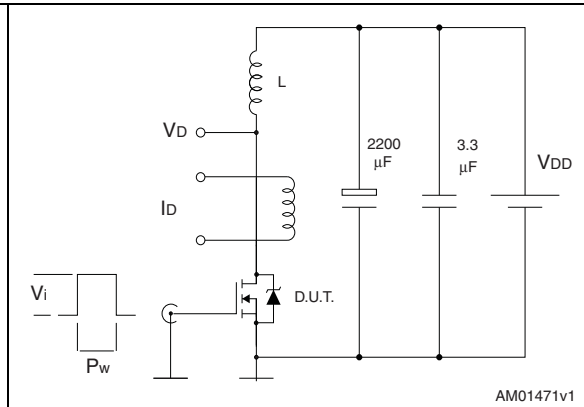


Figure 6. Unclamped inductive waveform

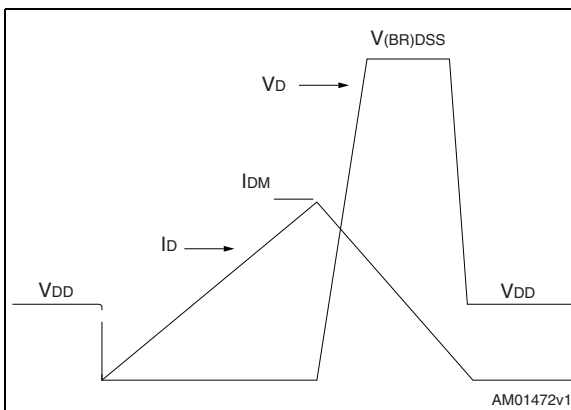
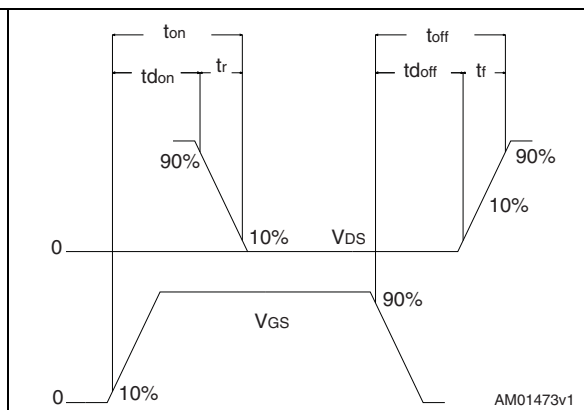


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H²PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 8. H²PAK 2 leads drawing

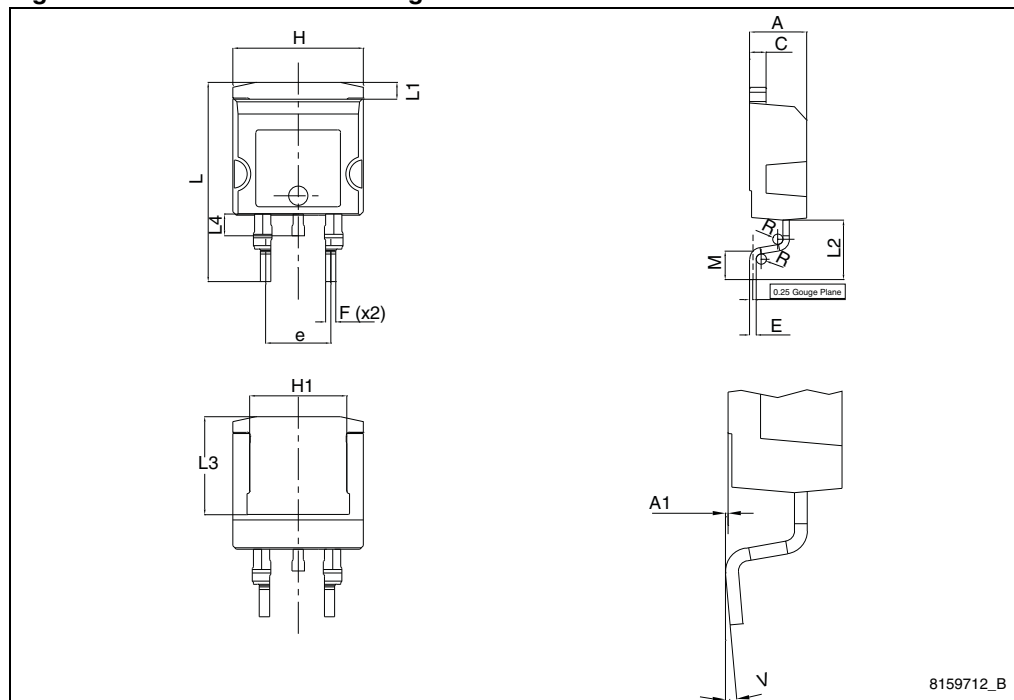
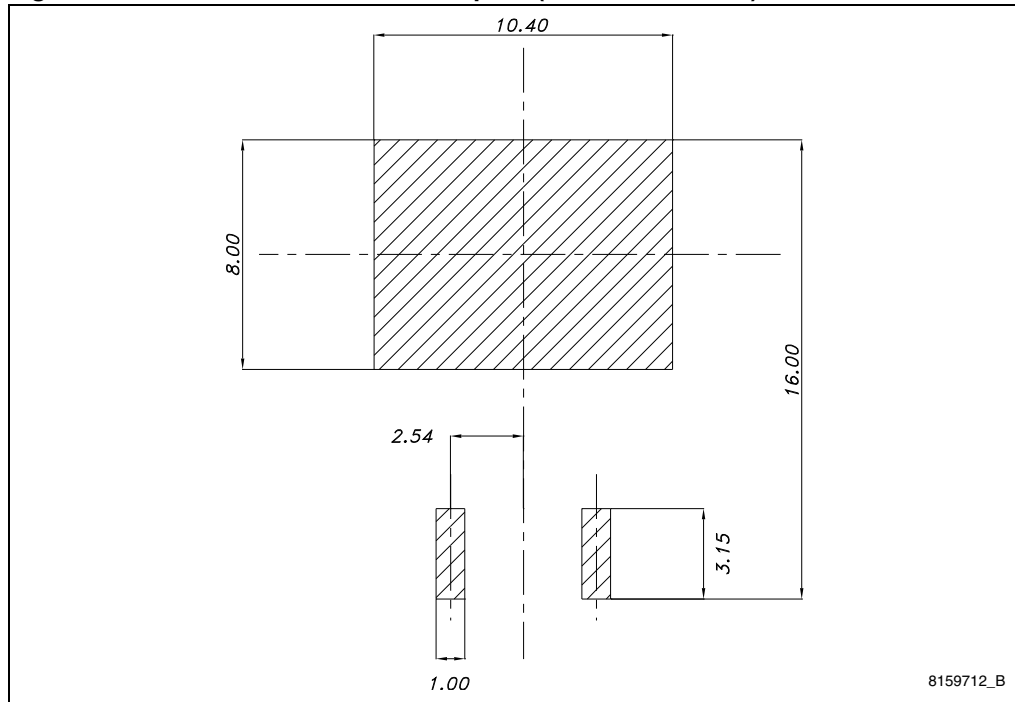


Figure 9. H²PAK2 recommended footprint (dimension in mm)



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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-May-2011	1	First release.

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