

# 4V Drive Pch MOSFET

## RRR015P03

### ● Structure

Silicon P-channel MOSFET

### ● Features

- 1) Low On-resistance.
- 2) High power package.
- 3) 4V drive.

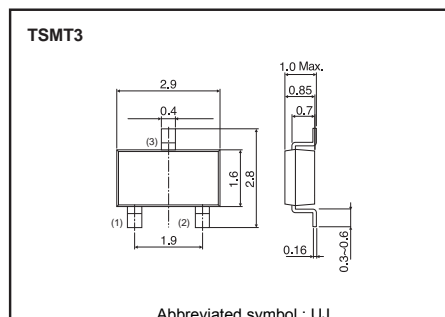
### ● Application

Switching

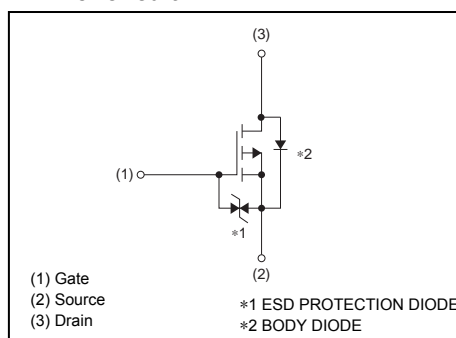
### ● Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RRR015P03		○

### ● Dimensions (Unit : mm)



### ● Inner circuit



### ● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	$V_{DSS}$	-30	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	Continuous	$I_D$	$\pm 1.5$ A
	Pulsed	$I_{DP}^{*1}$	$\pm 6$ A
Source current (Body Diode)	Continuous	$I_S$	-0.8 A
	Pulsed	$I_{SP}^{*1}$	-6 A
Power dissipation	$P_D^{*2}$	1.0	W
Channel temperature	Tch	150	°C
Range of storage temperature	Tstg	-55 to +150	°C

\*1  $P_w \leq 10 \mu s$ , Duty cycle  $\leq 1\%$

\*2 Mounted on a ceramic board.

### ● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	125	°C / W

\*Mounted on a ceramic board.

## ● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	-	-	$\pm 10$	$\mu A$	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	-	-	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	$I_{DSS}$	-	-	-1	$\mu A$	$V_{DS} = -30V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	115	160	m $\Omega$	$I_D = -1.5A, V_{GS} = -10V$
		-	170	240		$I_D = -0.7A, V_{GS} = -4.5V$
		-	190	270		$I_D = -0.7A, V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	1.2	-	-	S	$V_{DS} = -10V, I_D = -1.5A$
Input capacitance	$C_{iss}$	-	230	-	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	-	40	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	$C_{rss}$	-	33	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	12	-	ns	$I_D = -0.7A, V_{DD} = -15V$
Rise time	$t_r^*$	-	8	-	ns	$V_{GS} = -10V$
Turn-off delay time	$t_{d(off)}^*$	-	40	-	ns	$R_L = 21.4\Omega$
Fall time	$t_f^*$	-	13	-	ns	$R_G = 10\Omega$
Total gate charge	$Q_g^*$	-	3.2	-	nC	$I_D = -1.5A, V_{DD} = -15V$
Gate-source charge	$Q_{gs}^*$	-	1.2	-	nC	$V_{GS} = -5V, R_L = 10\Omega$
Gate-drain charge	$Q_{gd}^*$	-	0.7	-	nC	$R_G = 10\Omega$

\*Pulsed

## ● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	$V_{SD}^*$	-	-	-1.2	V	$I_s = -1.5A, V_{GS} = 0V$

\*Pulsed

● Electrical characteristic curves

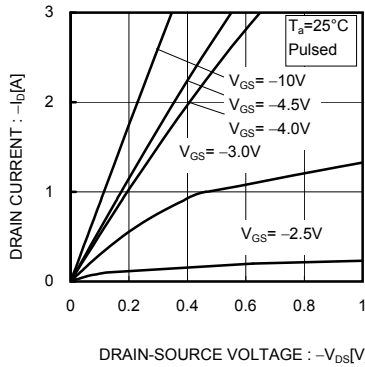


Fig.1 Typical Output Characteristics( I )

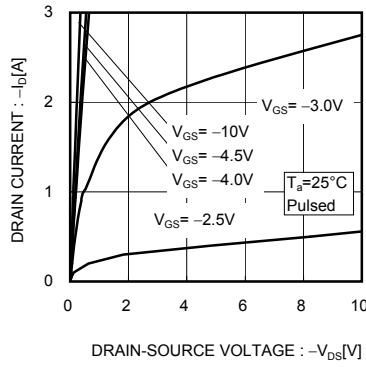


Fig.2 Typical Output Characteristics( II )

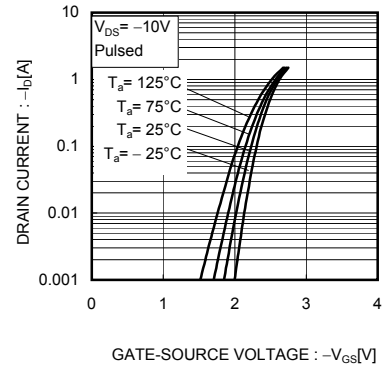


Fig.3 Typical Transfer Characteristics

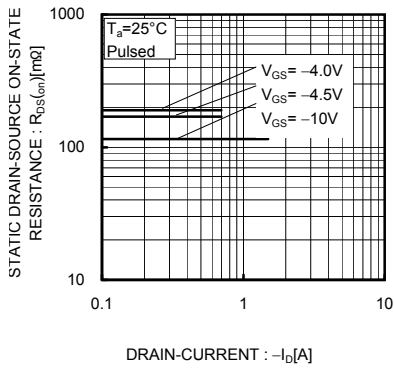


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current( I )

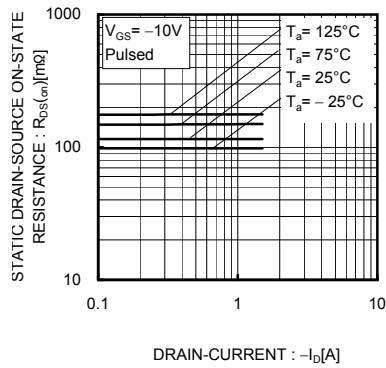


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )

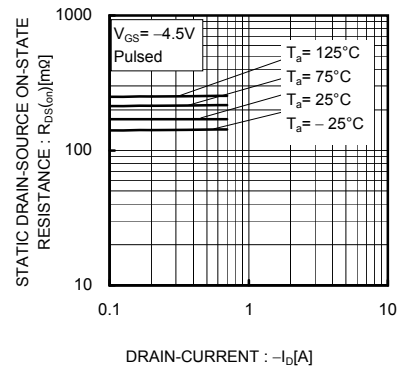


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current( III )

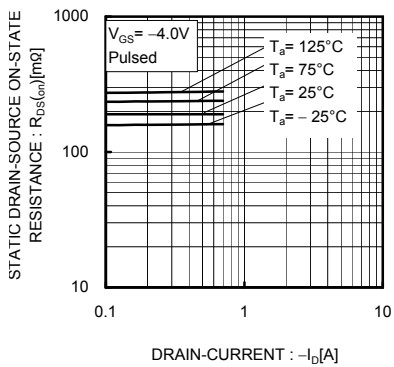


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

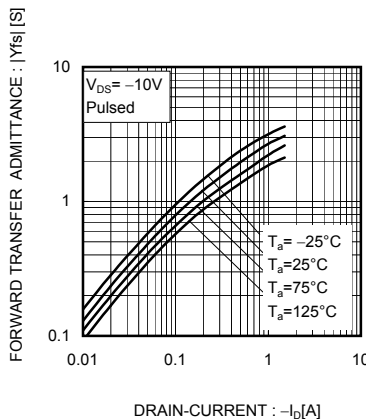


Fig.8 Forward Transfer Admittance vs. Drain Current

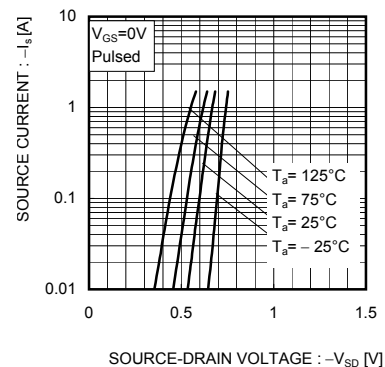


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

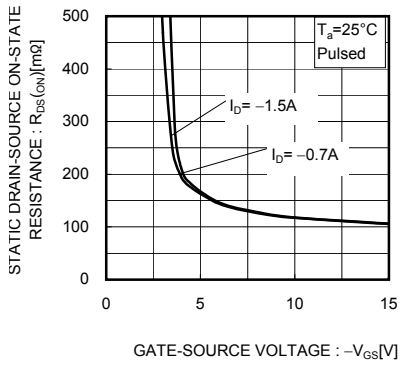


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

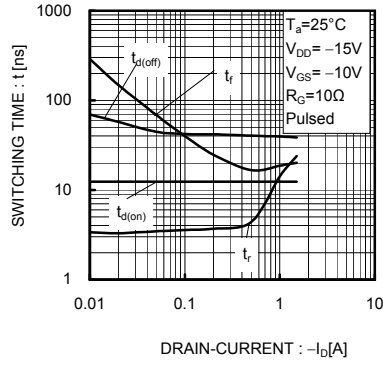


Fig.11 Switching Characteristics

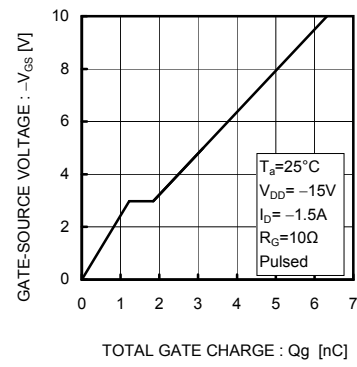


Fig.12 Dynamic Input Characteristics

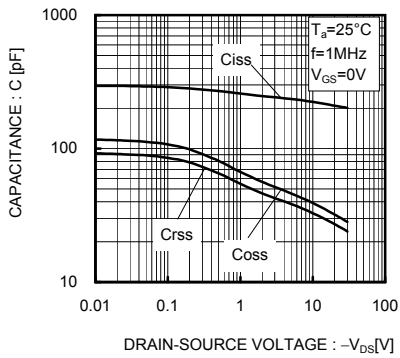


Fig.13 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

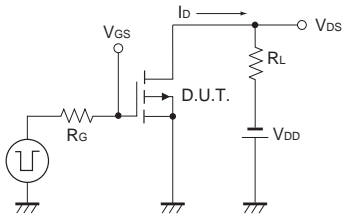


Fig.1-1 Switching time measurement circuit

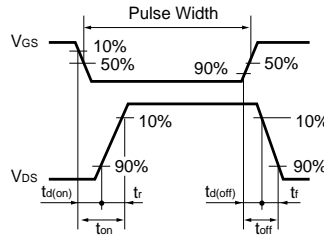


Fig.1-2 Switching Waveforms

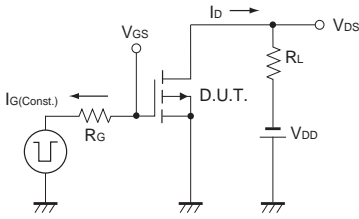


Fig.2-1 Gate charge measurement circuit

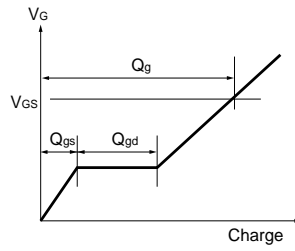


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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