

TONE CONTROL DIGITALLY CONTROLLED AUDIO PROCESSOR

1 FEATURES

- INPUT MULTIPLEXER
 - 2 STEREO INPUTS
 - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE, AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
 - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

2 DESCRIPTION

The TDA7449 is a volume tone (bass and treble) balance (Left/Right) processor for quality audio

Figure 1. Package

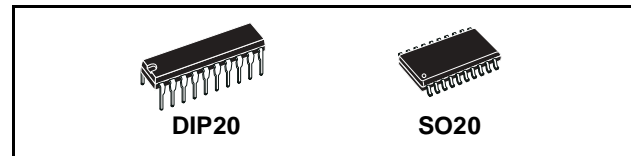


Table 1. Order Codes

Part Number	Package
TDA7449	DIP20
TDA7449D	SO20

applications in TV systems. Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Block Diagram

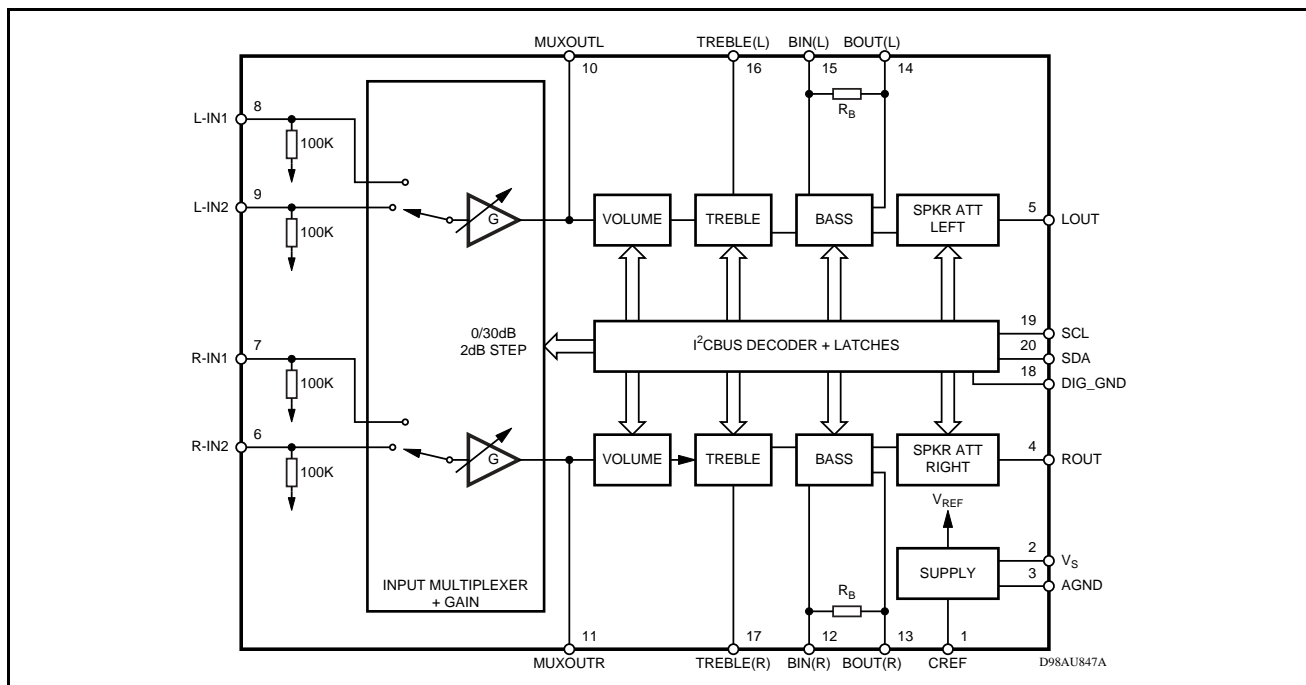


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _S	Operating Supply Voltage	10.5	V
T _{amb}	Operating Ambient Temperature	0 to 70	°C
T _{stg}	Storage Temperature Range	-55 to 150	°C

Figure 3. Pin Connection

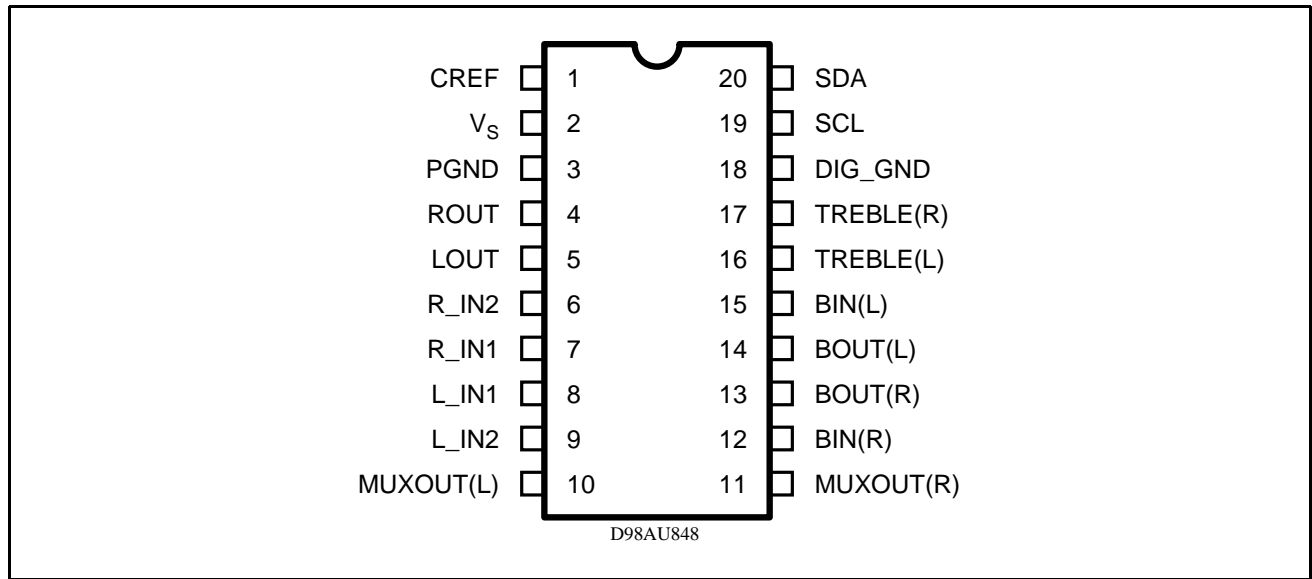


Table 3. Thermal Data

Symbol	Parameter	Value	Unit
R _{th j-pin}	Thermal Resistance Junction- pins	85	°C/W

Table 4. Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _S	Supply Voltage	6	9	10.2	V
V _{CL}	Max Input Signal Handling	2			V _{RMS}
THD	Total Harmonic Distortion V = 0.1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V _{out} = 1Vrms (mode = OFF)		106		dB
S _C	Channel Separation f = 1KHz		90		dB
	Input Gain (2dB step)	0		30	dB
	Volume Control (1dB step)	-47		0	dB
	Treble Control (2dB step)	-14		14	dB
	Bass Control (2dB step)	-14		14	dB
	Balance Control 1dB step	-79		0	dB
	Mute Attenuation		100		dB

Table 5. Electrical Characteristics (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{k}\Omega$, $R_G = 600\Omega$, all controls flat ($G = 0\text{dB}$), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10.2	V
I_S	Supply Current			7		mA
SVR	Ripple Rejection		60	90		dB
INPUT STAGE						
R_{IN}	Input Resistance			100		$\text{k}\Omega$
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V _{rms}
S_{IN}	Input Separation	The selected input is grounded through a 2.2μ capacitor	80	100		dB
G_{inmin}	Minimum Input Gain		-1	0	1	dB
G_{inmax}	Maximum Input Gain			30		dB
G_{step}	Step Resolution			2		dB
VOLUME CONTROL						
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Max. Attenuation		45	47	49	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	$A_V = 0$ to -24dB	-1.0	0	1.0	dB
		$A_V = -24$ to -47dB	-1.5	0	1.5	dB
E_T	Tracking Error	$A_V = 0$ to -24dB		0	1	dB
		$A_V = -24$ to -47dB		0	2	dB
V_{DC}	DC Step	adjacent attenuation steps		0	3	mV
		from 0dB to A_V max		0.5		mV
A_{mute}	Mute Attenuation		80	100		dB
BASS CONTROL (1)						
G_b	Control Range	Max. Boost/cut	+12.0	+14.0	+16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_b	Internal Feedback Resistance		18.75	25	31.25	$\text{k}\Omega$
TREBLE CONTROL (1)						
G_t	Control Range	Max. Boost/cut	+13.0	+14.0	+15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB

Table 5. Electrical Characteristics (continued)

SPEAKER ATTENUATORS						
C_{RANGE}	Control Range			76		dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	$A_V = 0$ to -20 dB	-1.5	0	1.5	dB
		$A_V = -20$ to -56 dB	-2	0	2	dB
V_{DC}	DC Step	adjacent attenuation steps		0	3	mV
A_{mute}	Mute Attenuation		80	100		dB
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	$d = 0.3\%$	2.1	2.6		V_{RMS}
R_L	Output Load Resistance		2			$K\Omega$
R_O	Output Impedance		10	40	70	W
V_{DC}	DC Voltage Level			3.8		V
GENERAL						
E_{NO}	Output Noise	All gains = 0dB; BW = 20Hz to 20KHz flat		5	15	μV
E_t	Total Tracking Error	$A_V = 0$ to -24 dB		0	1	dB
		$A_V = -24$ to -47 dB		0	2	dB
S/N	Signal to Noise Ratio	All gains 0dB; $V_O = 1V_{RMS}$;		106		dB
S_C	Channel Separation Left/Right		80	100		dB
d	Distortion	$A_V = 0$; $V_I = 1V_{RMS}$;		0.01	0.08	%
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current	$V_{IN} = 0.4V$	-5		5	μA
V_O	Output Voltage SDA Acknowledge	$I_O = 1.6mA$		0.4	0.8	V

Note: 1. The device is functionally good at $V_S = 5V$. a step down, on V_S , to 4V does't reset the device.

2. BASS and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

Figure 4. P.C.Board (Referred to DIP20 package only)

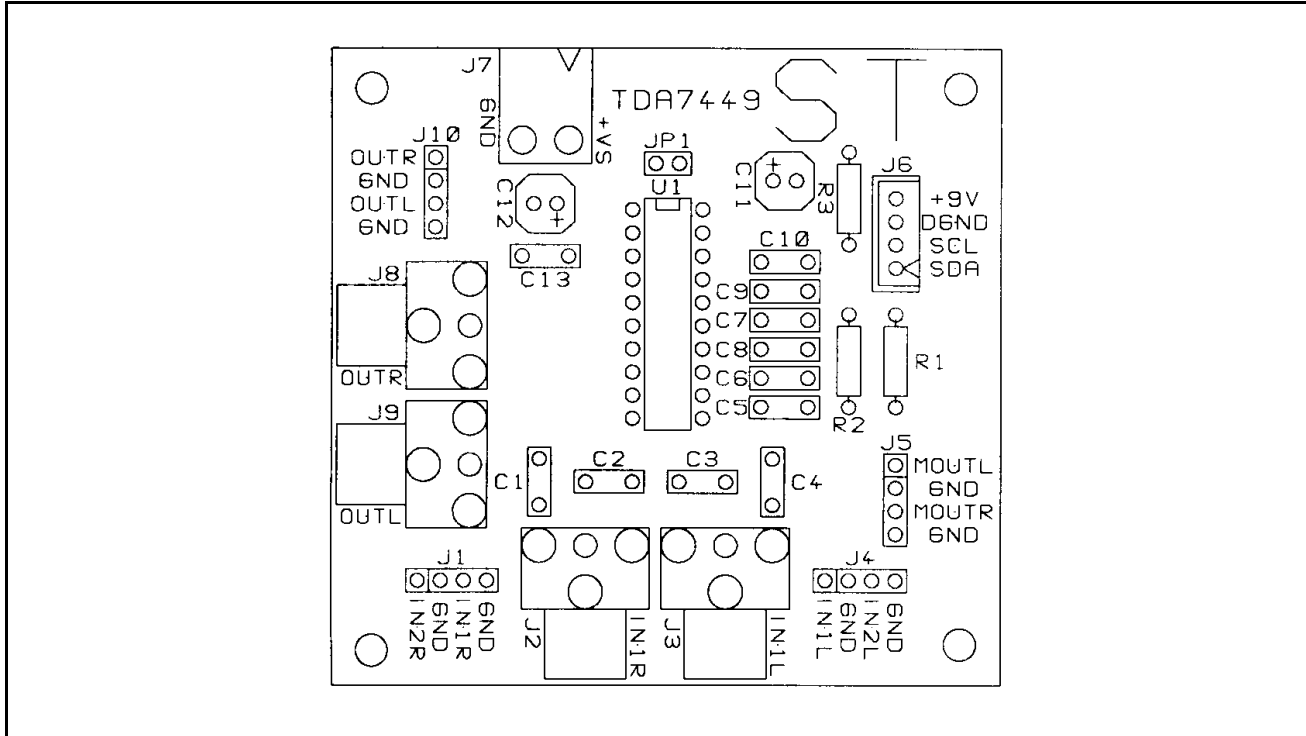
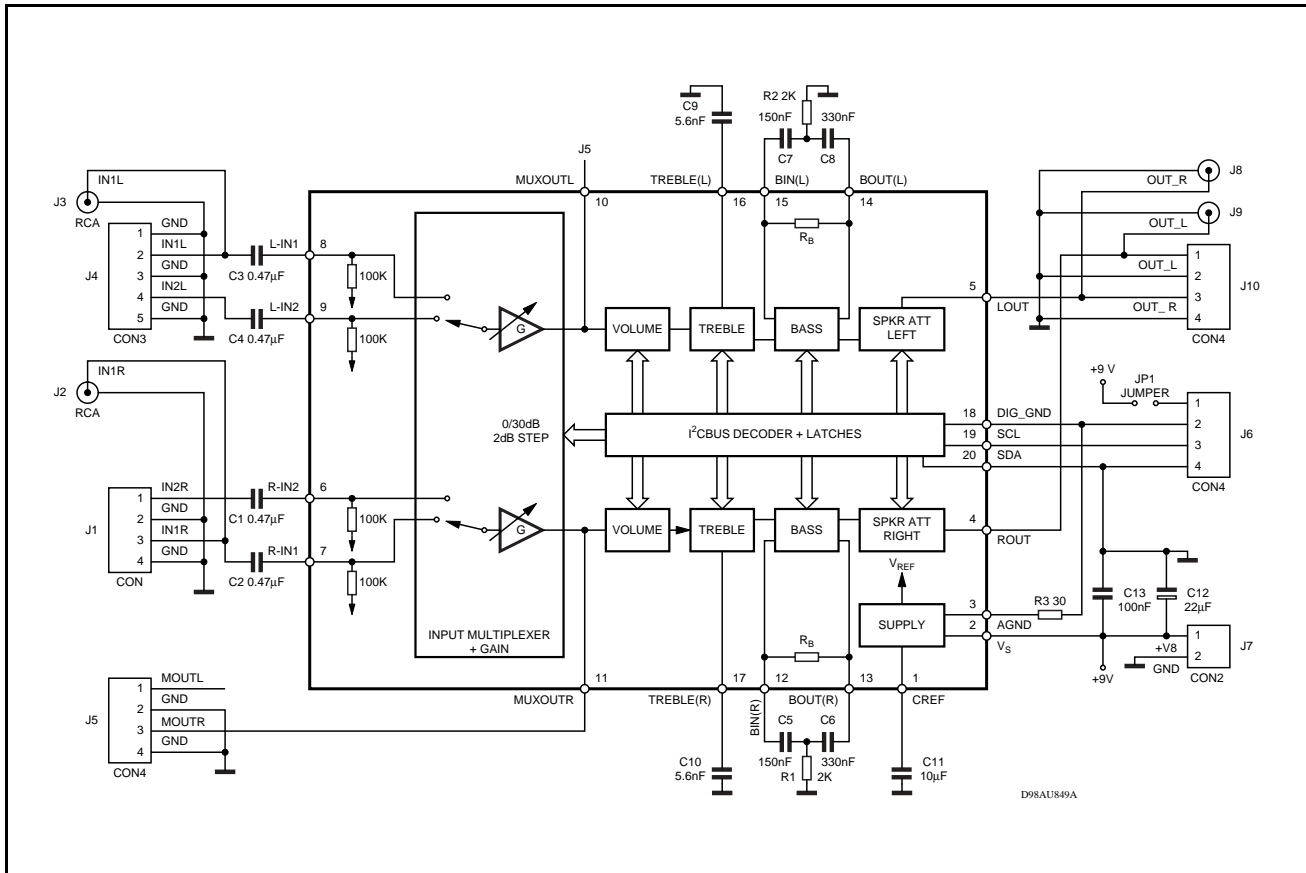


Figure 5. Test Circuit



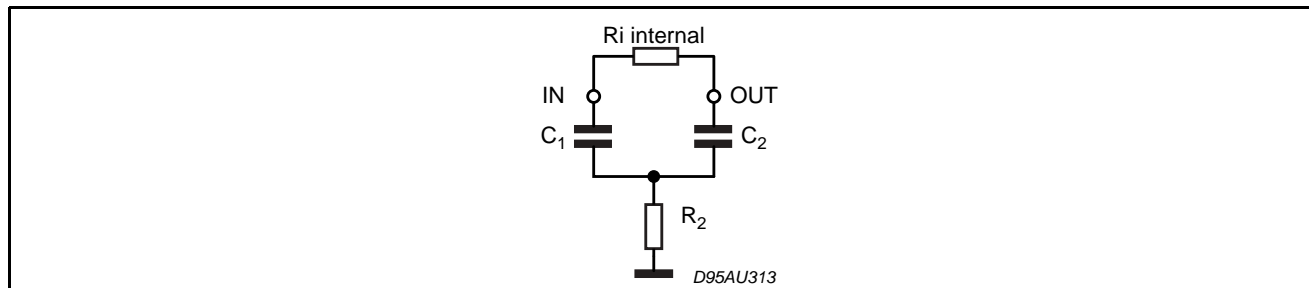
3 APPLICATION SUGGESTIONS

The first and the last stages are volume control blocks. The control range is 0 to -47dB (mute) for the first one, 0 to -79dB (mute) for the last one. Both of them have 1dB step resolution. The very high resolution allows the implementation of systems free from any noisy acoustical effect. The TDA7449 audioprocessor provides 2 bands tones control.

3.1 Bass, Stages

The Bass cell has an internal resistor $R_i = 25K\Omega$ typical. Several filter types can be implemented, connecting external components to the Bass IN and OUT pins. The fig.6 refers to basic T Type Bandpass Filter starting from the filter component values (R_1 internal F_c , the gain A_v at max. boost and the filter Q factor are computed as follows:

Figure 6.



$$F_c = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}$$

$$A_v = \frac{R_2 C_2 + R_2 C_1 + R_i C_1}{R_2 C_1 + R_2 C_2}$$

$$Q = \frac{\sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}{R_2 C_1 + R_2 C_2}$$

Viceversa, once F_c , A_v , and R_i internal value are fixed, the external components values will be:

$$C_1 = \frac{A_v - 1}{2 \cdot \pi \cdot F_c \cdot R_i \cdot Q} \quad C_2 = \frac{Q^2 \cdot C_1}{A_v - 1 - Q^2}$$

$$R_2 = \frac{A_v - 1 - Q^2}{2 \cdot \pi \cdot C_1 \cdot F_c \cdot (A_v - 1) \cdot Q}$$

3.2 Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25K Ω typical) and an external capacitor connected between treble pins and ground. Typical responses are reported in Fig. 10 to 13.

3.3 CREF

The suggested 10 μ F reference capacitor (CREF) value can be reduced to 4.7 μ F if the application requires faster power ON.

Figure 7. THD vs. frequency

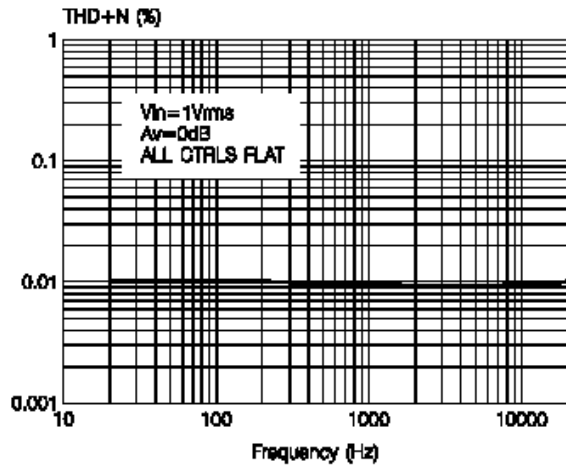


Figure 10. Bass response

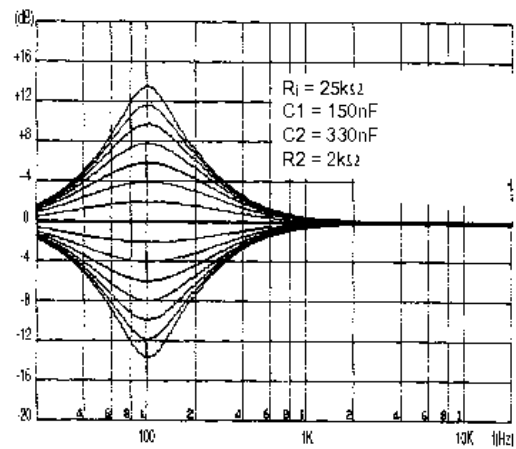


Figure 8. THD vs. RLOAD

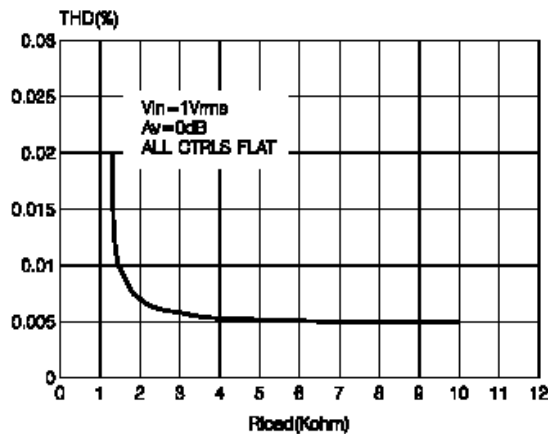


Figure 11. Treble response

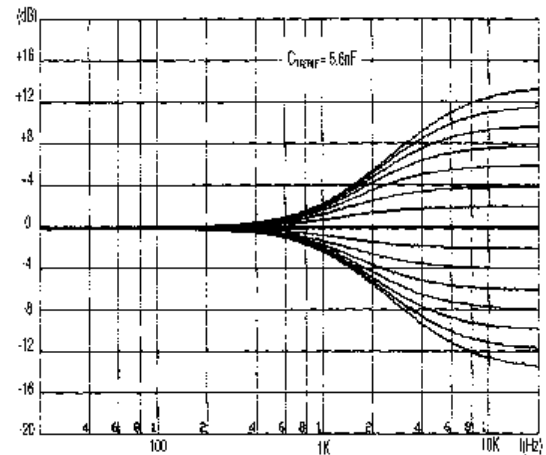
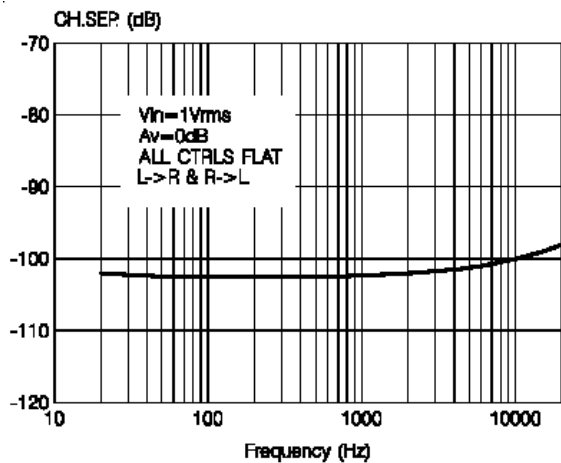


Figure 9. Channel separation vs. frequency



4 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7449 and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

4.1 Data Validity

As shown in fig. 12, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

4.2 Start and Stop Conditions

As shown in fig.13 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

4.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

4.4 Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 14). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

4.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 12. Data Validity on the I²C BUS

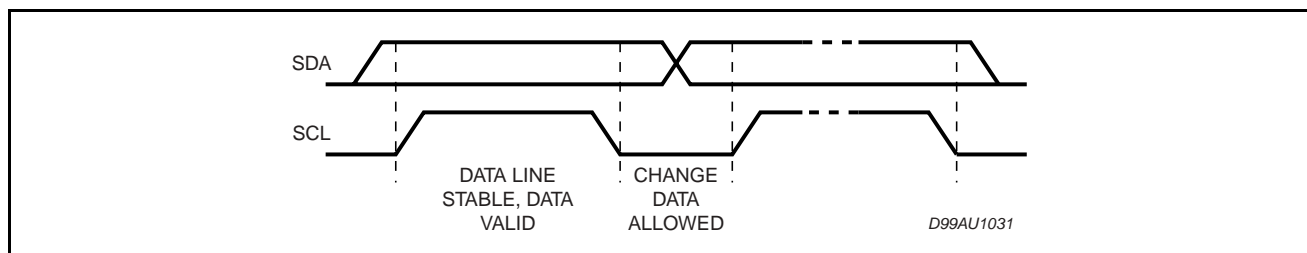


Figure 13. Timing Diagram of I²C BUS

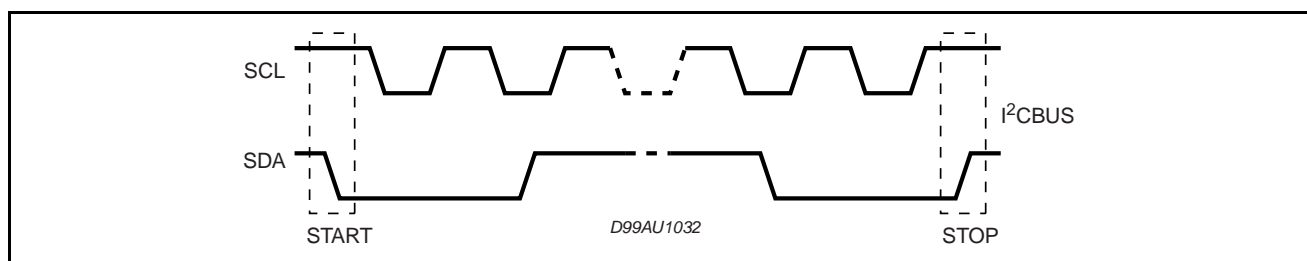
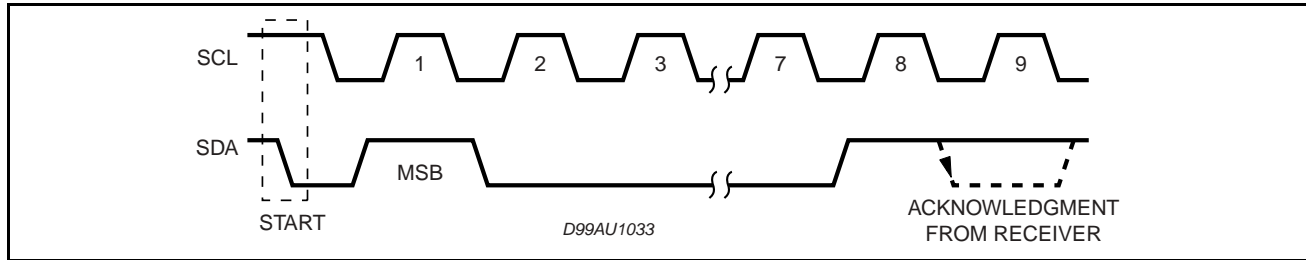


Figure 14. Acknowledge on the I²C BUS



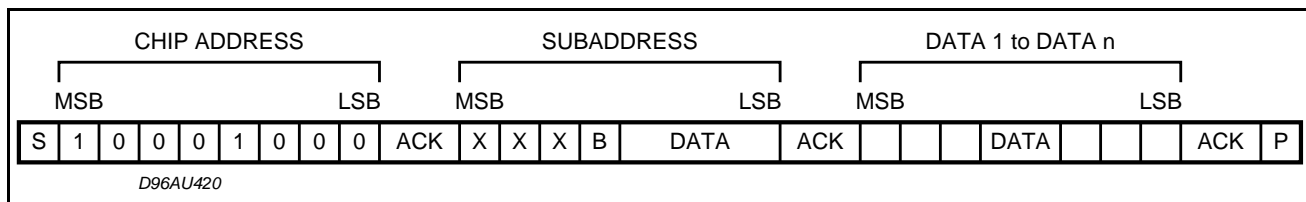
5 SOFTWARE SPECIFICATION

5.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7449 address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

Figure 15.



ACK = Acknowledge

S = Start

P = Stop

A = Address

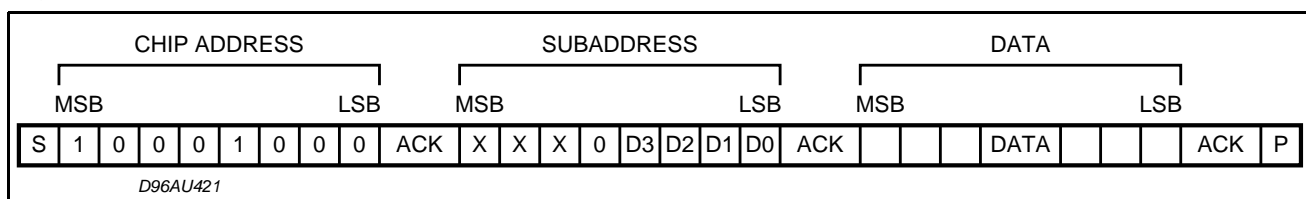
B = Auto Increment

6 EXAMPLES

6.1 No Incremental Bus

The TDA7449 receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

Figure 16.



6.2 Incremental Bus

The TDA7449 receive a start conditions, the correct chip address, a subaddress with the B = 1 incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.

Figure 17.

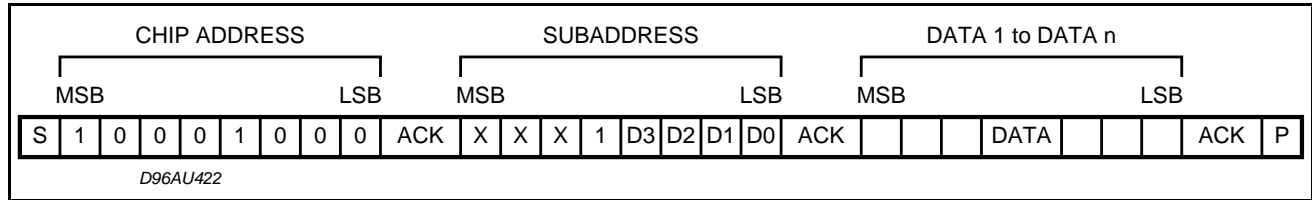


Table 6. POWER ON RESET CONDITION

INPUT SELECTION	IN2
INPUT GAIN	28dB
VOLUME	MUTE
BASS	0dB
TREBLE	2dB
SPEAKER	MUTE

7 DATA BYTES

Address = 88 HEX (ADDR:OPEN).

Table 7. FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	VOLUME
X	X	X	B	0	0	1	1	NOT ALLOWED
X	X	X	B	0	1	0	0	BASS
X	X	X	B	0	1	0	1	TREBLE
X	X	X	B	0	1	1	0	SPEAKER ATTENUATE "R"
X	X	X	B	0	1	1	1	SPEAKER ATTENUATE "L"

B = 1: INCREMENTAL BUS ACTIVE
 B = 0: NO INCREMENTAL BUS
 X = DON'T CARE

Table 8. INPUT SELECTION

MSB							LSB		INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0		
X	X	X	X	X	X	0	0	NOT ALLOWED	
X	X	X	X	X	X	0	1	NOT ALLOWED	
X	X	X	X	X	X	1	0	IN2	
X	X	X	X	X	X	1	1	IN1	

Table 9. INPUT GAIN SELECTION

MSB							LSB		INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS	
				0	0	0	0	0dB	
				0	0	0	1	2dB	
				0	0	1	0	4dB	
				0	0	1	1	6dB	
				0	1	0	0	8dB	
				0	1	0	1	10dB	
				0	1	1	0	12dB	
				0	1	1	1	14dB	
				1	0	0	0	16dB	
				1	0	0	1	18dB	
				1	0	1	0	20dB	
				1	0	1	1	22dB	
				1	1	0	0	24dB	
				1	1	0	1	26dB	
				1	1	1	0	28dB	
				1	1	1	1	30dB	

GAIN = 0 to 30dB

Table 10. VOLUME SELECTION

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	X	1	1	1	X	X	X	MUTE

VOLUME = 0 to 47dB/MUTE

Table 11. BASS SELECTION

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 12. TREBLE SELECTION

MSB							LSB	TREBLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 13. SPEAKER ATTENUATE SELECTION

MSB					LSB			SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	MUTE

SPEAKER ATTENUATION = 0 to -79dB/MUTE

Figure 18. PIN :1

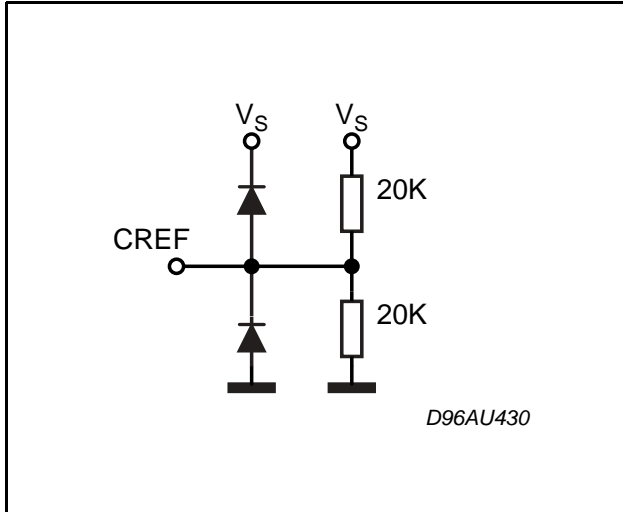


Figure 21. PINS: 10, 11

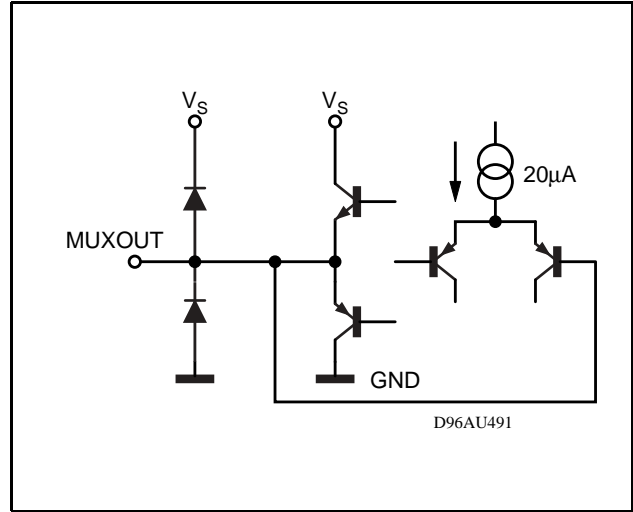


Figure 19. PINS: 4, 5

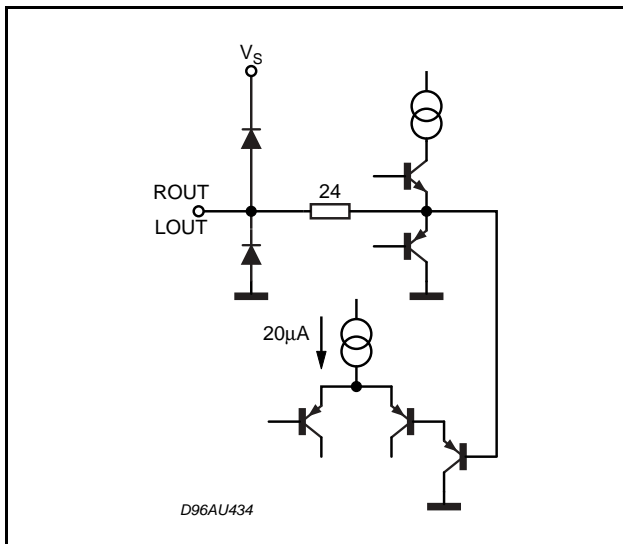


Figure 22. PINS: 12, 15

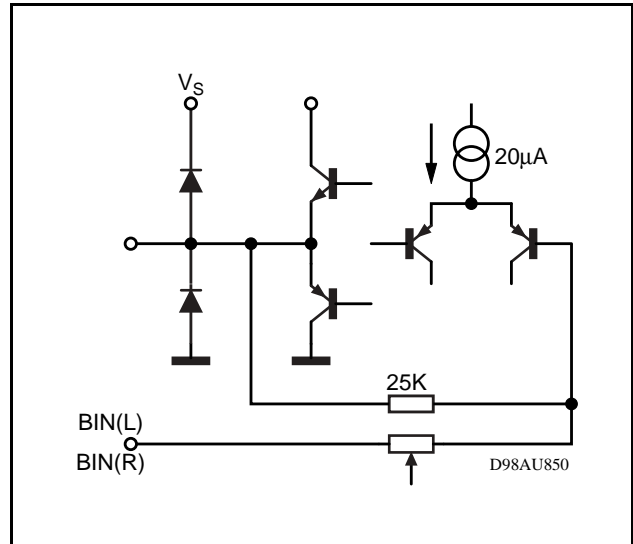


Figure 20. PINS: 6, 7, 8, 9

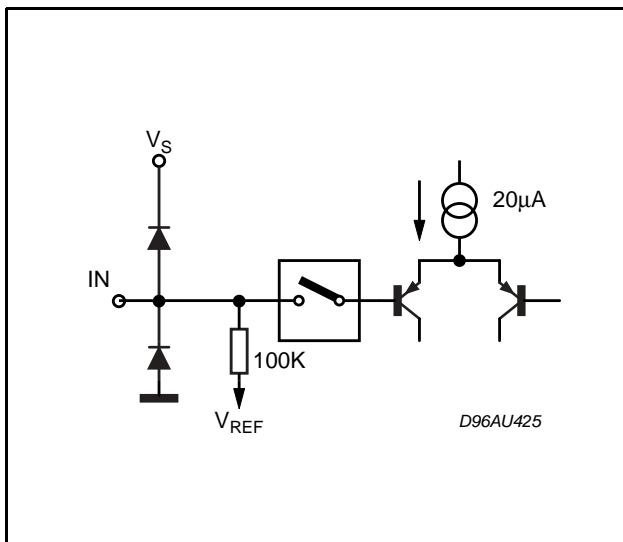


Figure 23. PINS: 13, 14,

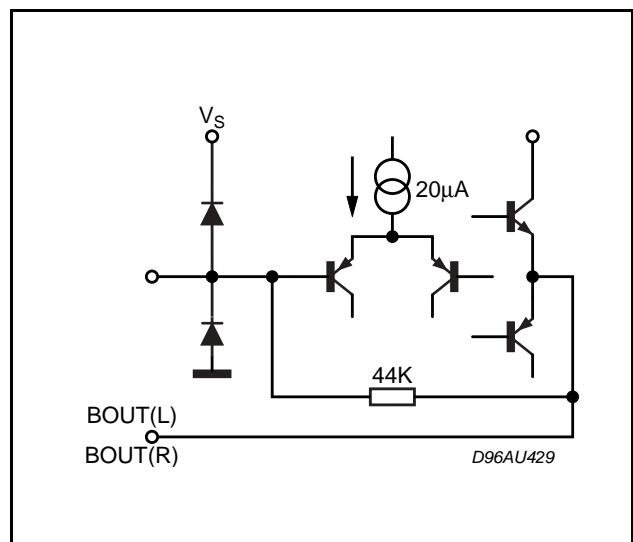


Figure 24. PINS: 16, 17

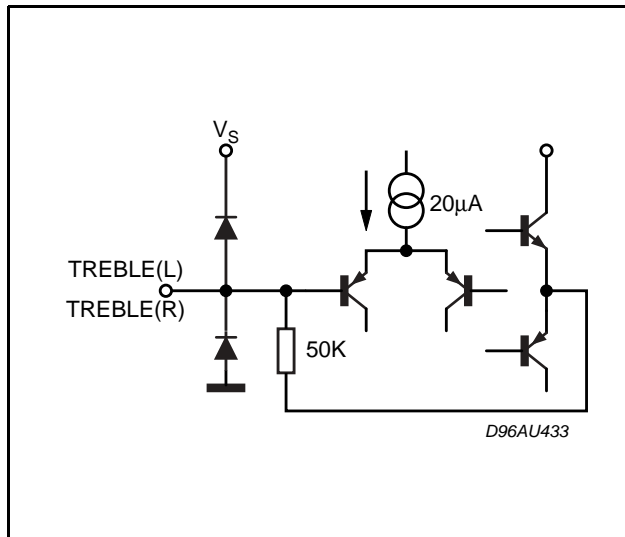


Figure 26. PIN 20

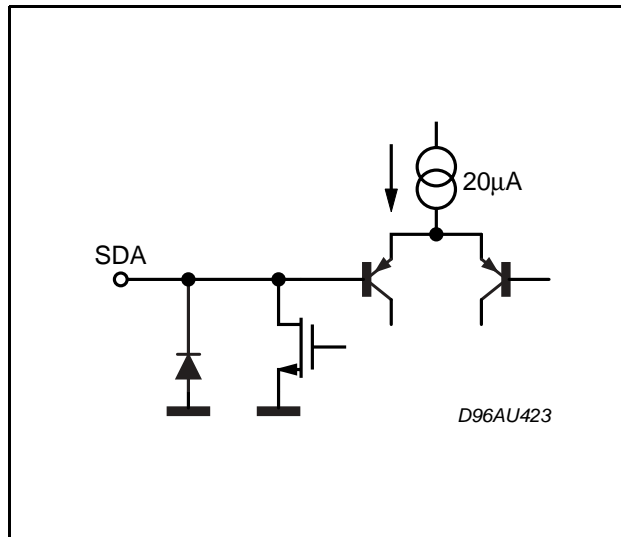


Figure 25. PIN: 19

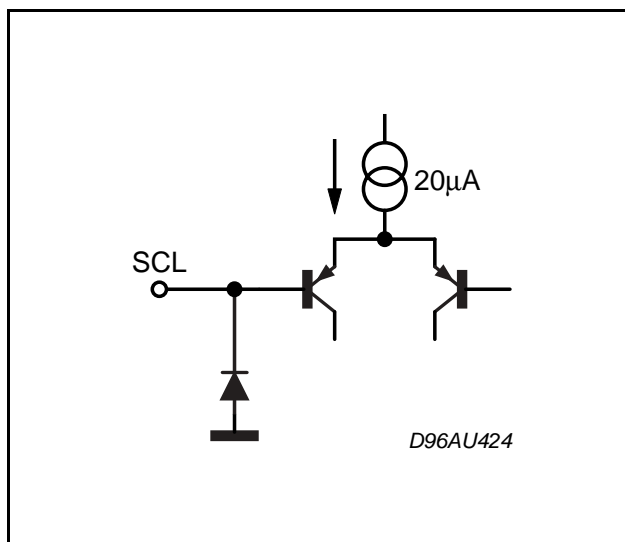
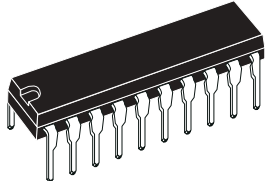


Figure 27. DIP20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

OUTLINE AND MECHANICAL DATA



DIP20

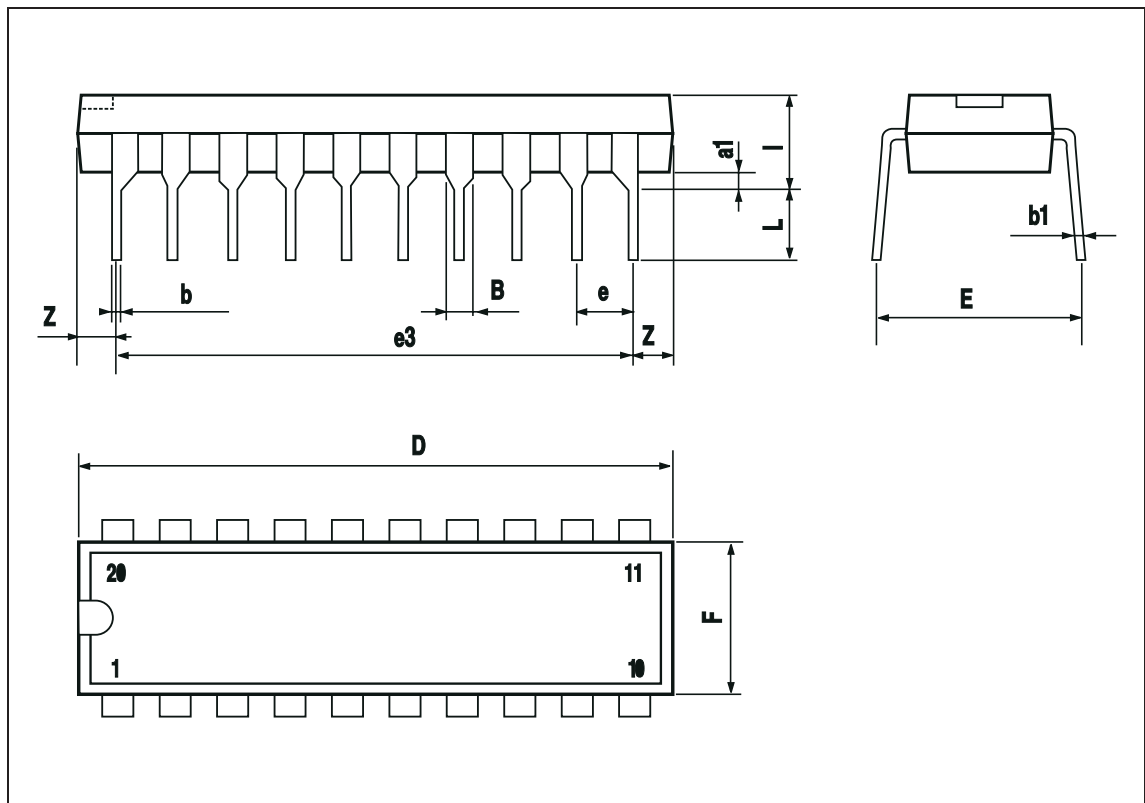
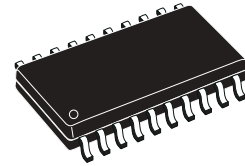


Figure 28. SO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

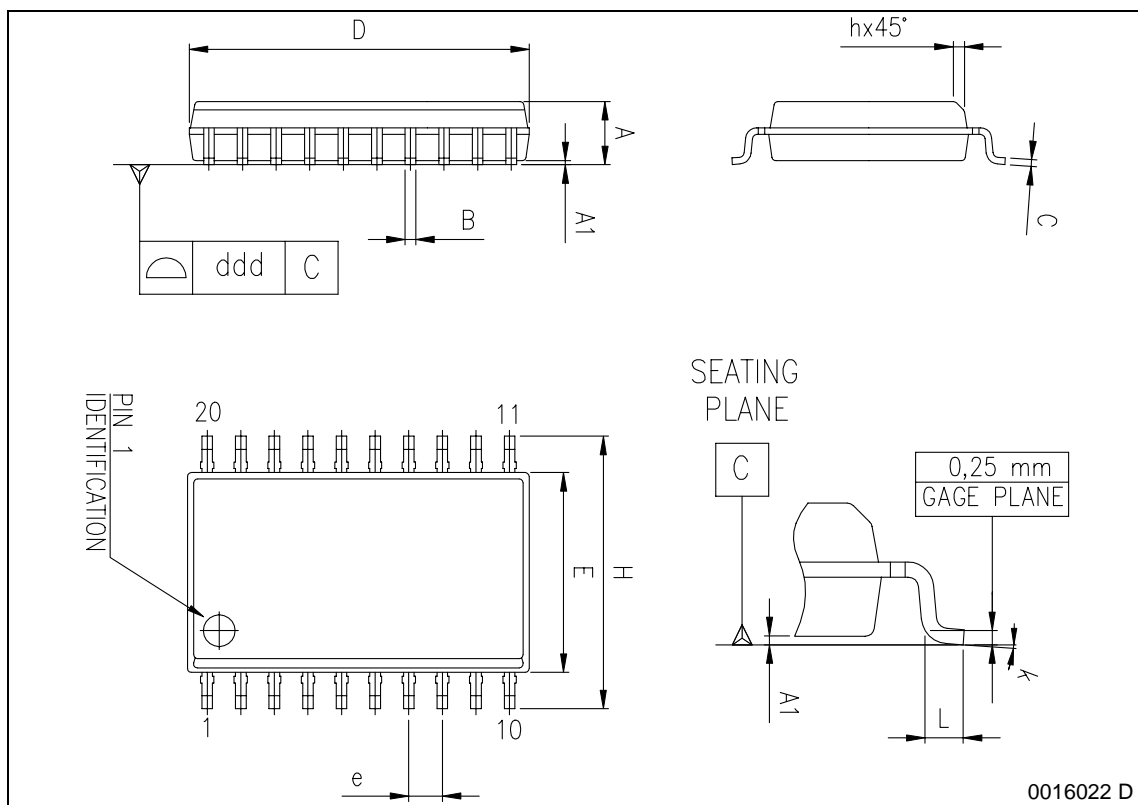


Table 14. Revision History

Date	Revision	Description of Changes
March 2004	3	Third Issue
June 2004	4	Modified the style-sheet in compliance with the last revision of the "Corporate Technical Publications Design Guide".

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