DATA SHEET

TDA9853H

I²C-bus controlled economic BTSC stereo decoder and audio processor

Product specification
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File under Integrated Circuits, IC02

Philips
Semiconductors

PHILIPS

I²C-bus controlled economic BTSC stereo decoder and audio processor

TDA9853H

FEATURES

- Voltage Controlled Amplifier (VCA) noise reduction circuit
- Stereo or mono selectable at the AF outputs
- Stereo pilot PLL circuit with ceramic resonator
- Automatic pilot cancellation
- I²C-bus transceiver.

Audio processor

- Selector for internal and external signals (line in)
- Automatic Volume Level (AVL) control (control range +6 to –15 dB)
- Volume control (control range +12 to –63 dB)
- Mute control via I²C-bus
- 4 fixed tone settings.

GENERAL DESCRIPTION

The TDA9853H is a bipolar-integrated BTSC stereo decoder and audio processor for application in TV sets, VCRs and multimedia PCs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9853H	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.8	8	9	V
I_{CC}	supply current		25	33	45	mA
$V_{o(rms)}$	output voltage (RMS value)	composite input voltage 250 mV (RMS) for 100% modulation L + R (25 kHz deviation); f_{mod} = 300 Hz	–	500	–	mV
$\alpha_{csL,R}$	stereo channel separation L and R	14% modulation; f_L = 300 Hz; f_R = 3 kHz	15	20	–	dB
$THD_{L,R}$	total harmonic distortion L and R	100% modulation L or R; f_{mod} = 1 kHz	–	0.2	1	%
S/N	signal-to-noise ratio at line out and at AF output	mono via I²C-bus; referenced to 500 mV output signal; volume 0 dB				
		CCIR 468-2 weighted; quasi peak	50	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
$V_{I, O(rms)}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	AVL control range		–15	–	+6	dB
G_c	volume control range		–63	–	+12	dB
L_{linear}	linear tone control		–	0	–	dB
$L_{bass(max)}$	tone control with maximum bass	referenced to linear position; f_{mod} = 20 Hz	10	12	–	dB
$L_{bass(min)}$	tone control with minimum bass	referenced to linear position; f_{mod} = 20 Hz	3.5	5	–	dB
$L_{treble(max)}$	tone control with maximum treble	referenced to linear position; f_{mod} = 20 kHz	6	8	–	dB
$L_{treble(min)}$	tone control with minimum treble	referenced to linear position; f_{mod} = 20 kHz	–	–1.5	–	dB

BLOCK DIAGRAM

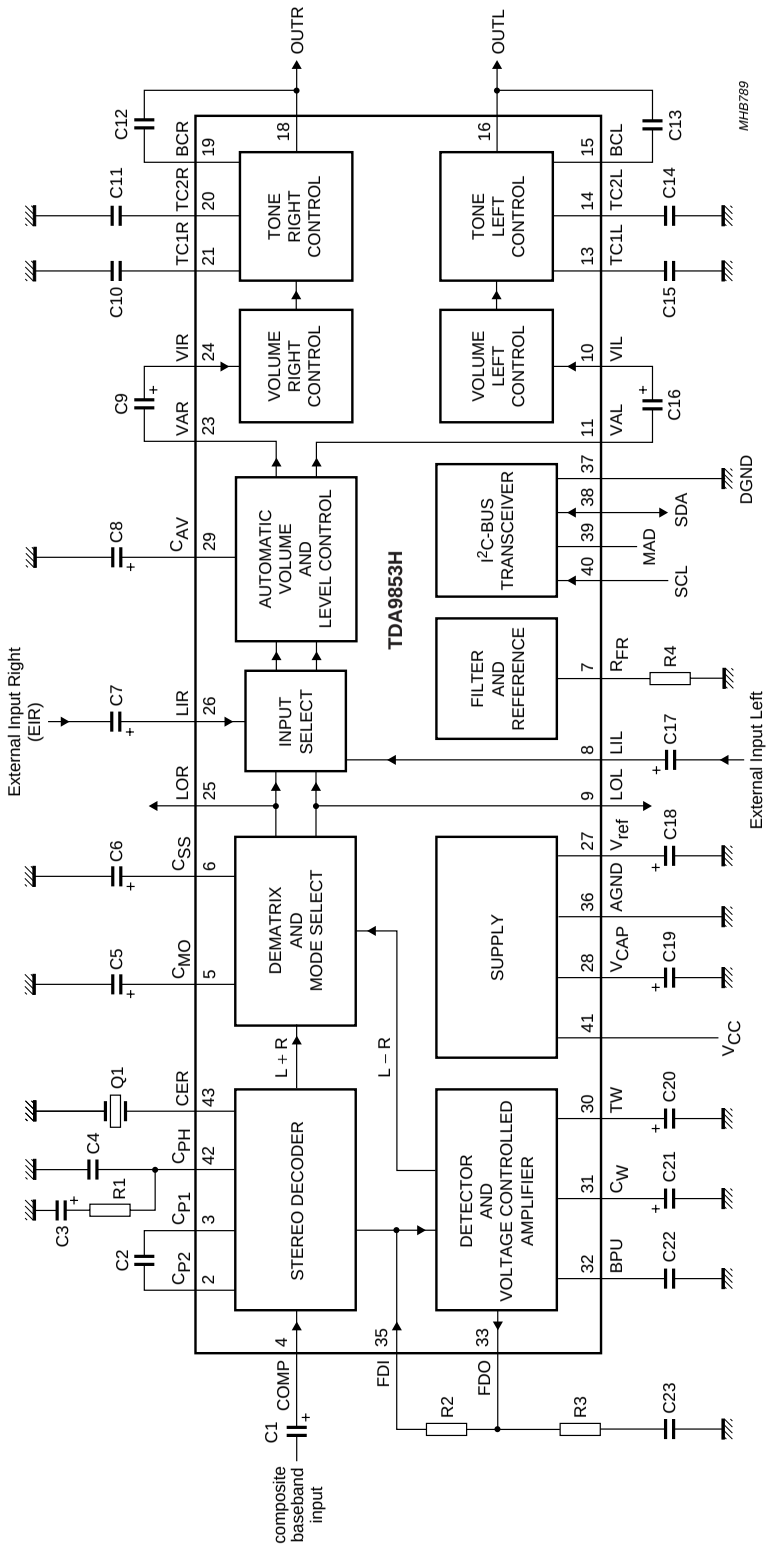


Fig.1 Block diagram.

Component list

Electrolytic capacitors ±20%; foil capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENT	VALUE	TYPE	REMARK
C1	2.2 µF	electrolytic	63 V
C2	220 nF	foil	
C3	2.2 µF	electrolytic	63 V
C4	220 nF	foil	
C5	2.2 µF	electrolytic	63 V
C6	2.2 µF	electrolytic	63 V
C7	2.2 µF	electrolytic	63 V
C8	4.7 µF	electrolytic	63 V ±10%
C9	2.2 µF	electrolytic	63 V
C10	3.3 nF	foil	
C11	150 pF	foil	
C12	56 nF	foil	
C13	56 nF	foil	
C14	150 pF	foil	
C15	3.3 nF	foil	
C16	2.2 µF	electrolytic	63 V
C17	2.2 µF	electrolytic	63 V
C18	100 µF	electrolytic	16 V
C19	100 µF	electrolytic	16 V
C20	10 µF	electrolytic	63 V
C21	1 µF	electrolytic	63 V
C22	4.7 nF	foil	
C23	22 nF	foil	
R1	3.3 kΩ		
R2	15 kΩ		
R3	1.3 kΩ		
R4	100 kΩ		
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
C_{P2}	2	connector 2 for pilot detector capacitor
C_{P1}	3	connector 1 for pilot detector capacitor
COMP	4	composite input signal
C_{MO}	5	capacitor for DC-decoupling mono
C_{SS}	6	capacitor for DC-decoupling stereo
R_{FR}	7	resistor for filter reference
LIL	8	line input; left channel
LOL	9	line output; left channel
VIL	10	volume control input; left channel
VAL	11	AVL output; left channel
n.c.	12	not connected
TC1L	13	treble capacitor 1; left channel
TC2L	14	treble capacitor 2; left channel
BCL	15	bass capacitor; left channel
OUTL	16	left channel output
n.c.	17	not connected
OUTR	18	right channel output
BCR	19	bass capacitor; right channel
TC2R	20	treble capacitor 2; right channel
TC1R	21	treble capacitor 1; right channel
n.c.	22	not connected
VAR	23	AVL output; right channel
VIR	24	volume control input; right channel
LOR	25	line output; right channel
LIR	26	line input; right channel
V_{ref}	27	reference voltage ($0.5V_{CC}$)
V_{CAP}	28	capacitor for electronic filtering of supply
C_{AV}	29	capacitor for AVL
TW	30	capacitor timing
C_W	31	capacitor for VCA and band-pass filter lower corner frequency
BPU	32	band-pass filter upper corner frequency
FDO	33	fixed de-emphasis output
n.c.	34	not connected
FDI	35	fixed de-emphasis input
AGND	36	analog ground
DGND	37	digital ground
SDA	38	serial data input/output
MAD	39	programmable address bit (module address)
SCL	40	serial clock input
V_{CC}	41	supply voltage
C_{PH}	42	capacitor for phase detector
CER	43	ceramic resonator
n.c.	44	not connected

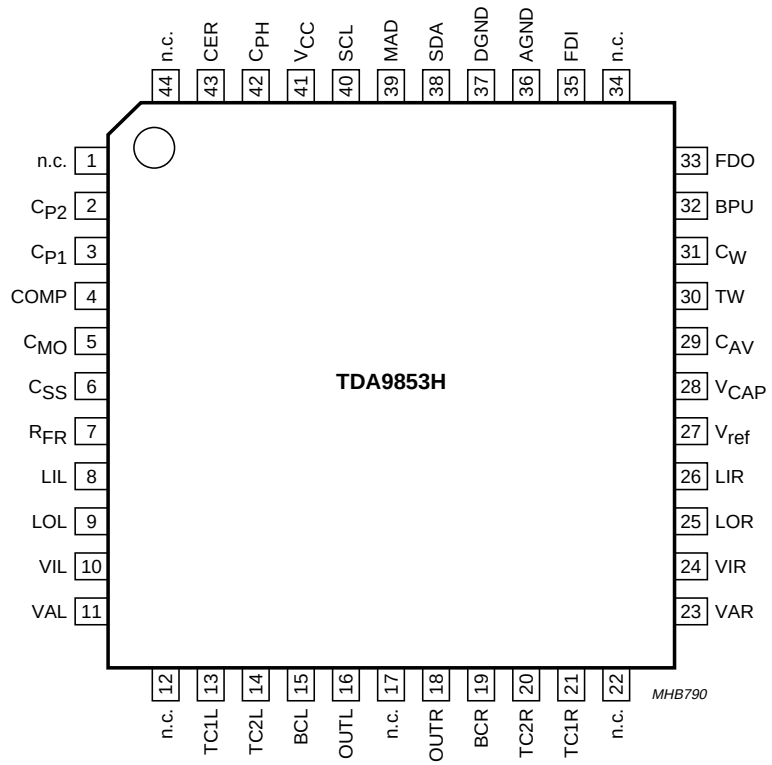


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Stereo decoder

The composite signal is fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L – R is applied to the Volume Controlled Amplifier (VCA) circuit. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator.

Mode selection

The L – R signal is fed via the internal VCA circuit to the dematrix/switching circuit. Mode selection is achieved via the I²C-bus (see Table 9).

The dematrix outputs can be muted via the I²C-bus (see Table 14).

Automatic volume level control

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range between 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and because of changes in the programme material; this function can be switched off. To avoid audible plops during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7 μF) at pin C_{AV} determines the attack and decay time constants. In addition the ratio of attack and decay times can be changed via the I²C-bus.

Integrated filters

The filter functions necessary for stereo demodulation are provided on-chip using transconductor circuits. The filter frequencies are controlled by the filter reference circuit via the external resistor R4.

Audio processor

SELECTOR

The selector enables the selection of either the internal line output signals LOR and LOL (dematrix output) or the external line input signals LIR and LIL (see Table 16). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is DC-coupled to the automatic volume level control circuit.

VOLUME

The volume control range is from +12 dB to −63 dB in steps of 1 dB and ends with a mute step (see Table 8). Balance control is achieved by the independent volume control of each channel.

BASS FUNCTION

A single external 56 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass range of +12 dB for high bass and +5 dB for low bass.

TREBLE FUNCTION

Two external capacitors C15 = 3.3 nF and C14 = 150 pF for each channel in combination with a linear operational amplifier and internal resistors provide a treble range of +8 dB for high treble and −1.5 dB for low treble.

MUTE

The mute function can be activated independently with the last step of volume control at the left or right output. By setting the general mute bit GMU the audio outputs OUTL and OUTR are muted.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–	9.5	V
V_{SDA}, V_{SCL}	voltage at pins SDA and SCL referenced to GND	$V_{CC} \leq 9$ V	−0.3	$+V_{CC}$	V
		$V_{CC} > 9$ V	−0.3	+9	V
V_n	voltage of all other pins to GND		0	V_{CC}	V
T_{amb}	ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling voltage	note 1	−200	+200	V
		note 2	−2000	+2000	V

Notes

1. Machine model class B, equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (‘0 Ω’ is actually 0.75 μH + 10 Ω).
2. Human body model class B, equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8 V; R_s = 600 Ω; AC-coupled; R_L = 10 kΩ; C_L = 2.5 nF; f_{mod} = 1 kHz mono signal; composite input voltage 250 mV (RMS) for 100% modulation L + R (25 kHz deviation); pilot 50 mV (RMS); G_v = 0 dB; linear tone control; AVL off; T_{amb} = 25 °C; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		7.8	8	9	V
I_{CC}	supply current		25	33	45	mA
V_{ref}	internal reference voltage at pin V_{ref}		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
Input stage						
$V_{i(max)(rms)}$	maximum input voltage (RMS value)		2	–	–	V
Z_i	input impedance		20	25	32	kΩ
Stereo decoder						
HR	headroom for L + R, L and R	f_{mod} = 300 Hz; THD < 15%	9	–	–	dB
$V_{pil(rms)}$	nominal stereo pilot voltage (RMS value)		–	50	–	mV
$V_{th(on)(rms)}$	pilot threshold voltage, stereo on (RMS value)		–	–	35	mV
$V_{th(off)(rms)}$	pilot threshold voltage, stereo off (RMS value)		15	–	–	mV
hys	hysteresis		–	2.5	–	dB
$V_{o(rms)}$	output voltage (RMS value)	100% modulation L + R; f_{mod} = 300 Hz	–	500	–	mV
$\alpha_{cs(L,R)}$	stereo channel separation L and R	14% modulation; f_L = 300 Hz; f_R = 3 kHz	15	20	–	dB
$THD_{L,R}$	total harmonic distortion L and R	100% modulation L or R; f_{mod} = 1 kHz	–	0.2	1	%
S/N	signal-to-noise ratio at line output and AF output	mono via I²C-bus; referenced to 500 mV output signal				
		CCIR 468-2 weighted; quasi peak	50	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
α_{mute}	mute attenuation at LOL, LOR, VAL and VAR	100% modulation L + R; f_{mod} = 300 Hz; mute via bit E6	63	–	–	dB
Stereo decoder, oscillator (VCXO); note 1						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
Δf_{fr}	spread of free-running frequency	with nominal ceramic resonator	500	–	507	kHz
Δf_{cr}	capture range frequency	nominal pilot	±190	±265	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio control part; input pins VIL and VIR to pins OUTL and OUTR						
V_O	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
Z_i	volume input impedance		25	30	38	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		0	–	2.5	nF
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	tbf	2	–	V
THD	total harmonic distortion	1 V (RMS) input voltage	–	0.05	–	%
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 10 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		mute position	–	10	–	μV
G_c	volume control range	maximum boost	–	12	–	dB
		maximum attenuation	–	63	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between adjoining step	G_v = +12 to –15 dB and G_v = –16 to –63 dB; note 2	–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +12 to –50 dB	–	–	2	dB
		G_v = –51 to –63 dB	–	–	3	dB
ΔG_L	gain tracking error	G_v = +12 to –50 dB	–	–	2	dB
α_m	mute attenuation		80	–	–	dB
$V_{DC(OS)}$	DC step offset between any adjacent step	G_v = +12 to 0 dB	–	0.2	10	mV
		G_v = 0 to –63 dB	–	–	5	mV
	DC step offset between any step to mute	G_v = +12 to 0 dB	–	2	15	mV
		G_v = –1 to –63 dB	–	1	10	mV
Tone control part						
L_{linear}	linear tone control		–	0	–	dB
$L_{bass(max)}$	tone control with maximum bass	referenced to linear position; f_{mod} = 20 Hz	10	12	–	dB
$L_{bass(min)}$	tone control with minimum bass	referenced to linear position; f_{mod} = 20 Hz	3.5	5	–	dB
$L_{treble(max)}$	tone control with maximum treble	referenced to linear position; f_{mod} = 20 kHz	6	8	–	dB
$L_{treble(min)}$	tone control with minimum treble	referenced to linear position; f_{mod} = 20 kHz	–	–1.5	–	dB

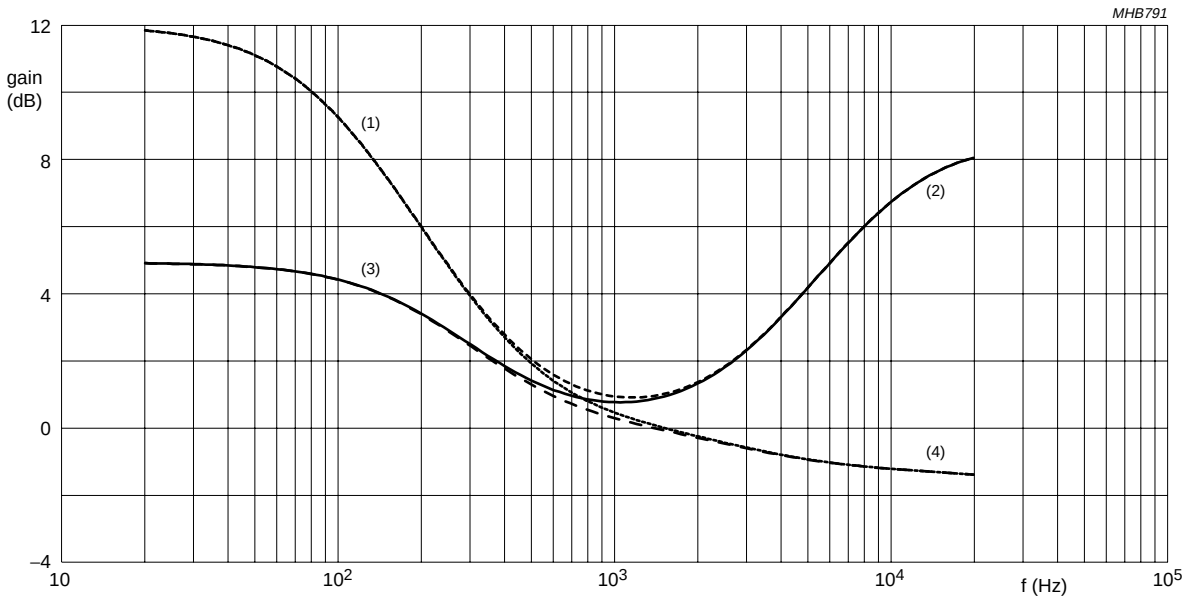
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCA						
I_s	nominal timing current for nominal release rate of VCA detector	I_s can be measured at pin TW via current meter connected to $0.5V_{CC}$ + 1 V	6.5	8	9.5	μA
Rel_{rate}	nominal detector release rate	nominal timing current and external capacitor values	–	125	–	dB/s
Automatic volume level control						
G_v	voltage gain	maximum boost; note 3	5	6	7	dB
		maximum attenuation; note 3	14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{i(rms)}$	input voltage (RMS value)	maximum boost; note 3	–	0.1	–	V
		maximum attenuation; note 3	–	1.125	–	V
$V_{o(AVL)(rms)}$	output voltage in AVL operation (RMS value)		160	200	250	mV
$V_{offset(DC)}$	DC offset voltage between different gain steps	voltage at pin C_{AV} 6 to 5.83 V or 5.83 to 5.61 V or 5.61 to 4.83 V or 4.83 to 2.1 V; note 4	–	–	20	mV
R_{att}	discharge resistors for attack time constant	AT1 = 0; AT2 = 0; note 5	340	420	520	Ω
		AT1 = 1; AT2 = 0; note 5	590	730	910	Ω
		AT1 = 0; AT2 = 1; note 5	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1; note 5	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	normal mode; CCD = 0; note 6	1.6	2	2.4	μA
		Power-on speed-up; CCD = 1; note 6	–	30	–	μA
Selector internal and external						
Z_i	input impedance		16	20	25	kΩ
α_s	input isolation of one selected source to the other input	V_i = 1 V; f_i = 1 kHz	70	76	–	dB
		V_i = 1 V; f_i = 12.5 kHz	70	76	–	dB
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2	–	V
G_v	voltage gain, selector		–	0	–	dB
Line output; pins LOL and LOR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
HR_o	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Monitor output; pins VAL and VAR						
V_O	DC output voltage		–	$0.5V_{CC}$	–	V
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance	with 100 Ω in series	–	–	2.5	nF
Muting at power supply voltage drop for OUTR and OUTL						
ΔV_{CC}	supply voltage drop for mute active		–	$V_{CAP} - 0.7$	–	V
Power-on reset; note 7						
$V_{POR(start)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	–	tbf	–	V
$V_{POR(end)}$	end of reset voltage	increasing supply voltage	–	tbf	–	V
Digital part (I²C-bus pins); note 8						
V_{IH}	HIGH-level input voltage		3	–	V_{CC}(9)	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage	I_{IL} = 3 mA	–	–	0.4	V

Notes

1. The oscillator is designed to operate together with Murata resonator CSB503F58 or CSB503JF958 as SMD. Change of the resonator supplier is possible, but the resonator specification must be close to the specified ones.
2. 1.5 dB step error between –15 and –16 dB.
3. The AVL input voltage is internal. It corresponds to the output voltage OUTL and OUTR at AVL off.
4. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB and –15 dB.
5. Attack time constant = $C_{CAV} \times R_{att}$ with C_{CAV} = C8 (see Fig.1).
6. Decay time $= \dfrac{C_{CAV} \times 0.76\ V \left(10^{\frac{-G_1}{20}} - 10^{\frac{-G_2}{20}} \right)}{I_{dec}}$

   a) Example: C_{CAV} = 4.7 µF; I_{dec} = 2 µA; G_1 = –9 dB; G_2 = +6 dB → decay time results in 4.14 s.
7. When reset is active the GMU bit (mute) is set and the I²C-bus receiver is in the reset position.
8. The AC characteristics are in accordance with the I²C-bus specification for standard mode (clock frequency maximum 100 kHz). A higher frequency, up to 280 kHz, can be used if all clock and data times are interpolated between standard mode (100 kHz) and fast mode (400 kHz) in accordance with the I²C-bus specification. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011).
9. Maximum 9 V if V_{CC} > 9 V.



(1) Maximum bass.
(2) Maximum treble.
(3) Minimum bass.
(4) Minimum treble.

Fig.3 Tone control.

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	AN	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	1011011; pin MAD not connected
Pin programmable SLAVE ADDRESS	1011010; pin MAD connected to ground
R/$\overline{W}$	logic 1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
AN	acknowledge not; generated by the master
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

MSB							**LSB**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Y	Y	Y	Y	Y	Y	PONR	STP

Table 3 Bit functions of Table 2

BIT	FUNCTION
STP	stereo pilot identification (stereo received = 1)
PONR	Power-on reset; if PONR = 1, then Power-on reset is detected
Y	indefinite

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	SUBADDRESS	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS	101 101 1; pin MAD not connected
Pin programmable SLAVE ADDRESS	101 101 0; pin MAD connected to ground
R/$\overline{W}$	logic 0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

Table 5 Subaddress definition (second byte after slave address)

FUNCTION	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1[1]	D0[1]
Volume right	0	0	0	0	0	0	0	0
Volume left	0	0	0	0	0	0	0	1
Control 1	0	0	0	0	0	0	1	0
Control 2	0	0	0	0	0	0	1	1

Note

1. Significant subaddress bits.

Table 6 Data definition (third byte after slave address)

FUNCTION	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Volume right	0	B6	B5	B4	B3	B2	B1	B0
Volume left	0	C6	C5	C4	C3	C2	C1	C0
Control 1	0	E6	E5	E4	E3	E2	E1	E0
Control 2	0	0	0	F4	F3	F2	F1	F0

Table 7 Bit functions of Table 6

BITS	SYMBOL	FUNCTION
B0 to B6	VR0 to VR6	volume control right
C0 to C6	VL0 to VL6	volume control left
E0	STEREO	mode selection for line out
E1	GMU	mute control for OUTL and OUTR
E2	AVLON	AVL **on**/**off**
E3	CCD	increased AVL decay current **on**/**off**
E4 and E5	AT1 and AT2	attack time at AVL
E6	LMU	line out mute **on**/**off**
F0 and F1	TONE	selection between four fixed tone controls
F2	MODE	selection between intern and extern
F3	MONO	forced mono **on**/**off** at OUTL and OUTR
F4	LITO	linear tone control **on**/**off**

Table 8 Volume setting

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
12	1	1	1	1	0	1	1
11	1	1	1	1	0	1	0
10	1	1	1	1	0	0	1
9	1	1	1	1	0	0	0
8	1	1	1	0	1	1	1
7	1	1	1	0	1	1	0
6	1	1	1	0	1	0	1
5	1	1	1	0	1	0	0
4	1	1	1	0	0	1	1
3	1	1	1	0	0	1	0
2	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0
0	1	1	0	1	1	1	1
–1	1	1	0	1	1	1	0
–2	1	1	0	1	1	0	1
–3	1	1	0	1	1	0	0
–4	1	1	0	1	0	1	1
–5	1	1	0	1	0	1	0
–6	1	1	0	1	0	0	1
–7	1	1	0	1	0	0	0
–8	1	1	0	0	1	1	1
–9	1	1	0	0	1	1	0
–10	1	1	0	0	1	0	1
–11	1	1	0	0	1	0	0
–12	1	1	0	0	0	1	1
–13	1	1	0	0	0	1	0
–14	1	1	0	0	0	0	1
–15	1	1	0	0	0	0	0
–16	1	0	1	1	1	1	1
–17	1	0	1	1	1	1	0
–18	1	0	1	1	1	0	1
–19	1	0	1	1	1	0	0
–20	1	0	1	1	0	1	1
–21	1	0	1	1	0	1	0
–22	1	0	1	1	0	0	1
–23	1	0	1	1	0	0	0
–24	1	0	1	0	1	1	1
–25	1	0	1	0	1	1	0

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
−26	1	0	1	0	1	0	1
−27	1	0	1	0	1	0	0
−28	1	0	1	0	0	1	1
−29	1	0	1	0	0	1	0
−30	1	0	1	0	0	0	1
−31	1	0	1	0	0	0	0
−32	1	0	0	1	1	1	1
−33	1	0	0	1	1	1	0
−34	1	0	0	1	1	0	1
−35	1	0	0	1	1	0	0
−36	1	0	0	1	0	1	1
−37	1	0	0	1	0	1	0
−38	1	0	0	1	0	0	1
−39	1	0	0	1	0	0	0
−40	1	0	0	0	1	1	1
−41	1	0	0	0	1	1	0
−42	1	0	0	0	1	0	1
−43	1	0	0	0	1	0	0
−44	1	0	0	0	0	1	1
−45	1	0	0	0	0	1	0
−46	1	0	0	0	0	0	1
−47	1	0	0	0	0	0	0
−48	0	1	1	1	1	1	1
−49	0	1	1	1	1	1	0
−50	0	1	1	1	1	0	1
−51	0	1	1	1	1	0	0
−52	0	1	1	1	0	1	1
−53	0	1	1	1	0	1	0
−54	0	1	1	1	0	0	1
−55	0	1	1	1	0	0	0
−56	0	1	1	0	1	1	1
−57	0	1	1	0	1	1	0
−58	0	1	1	0	1	0	1
−59	0	1	1	0	1	0	0
−60	0	1	1	0	0	1	1
−61	0	1	1	0	0	1	0
−62	0	1	1	0	0	0	1
−63	0	1	1	0	0	0	0
Mute	0	1	0	1	1	1	1

Table 9 Mode setting

FUNCTION MODE		READABLE BIT D0/STP	SETTING BIT E0/STEREO
LOL	LOR		
Left	right	logic 1 (stereo received)	1
Mono	mono	logic 1 (stereo received)	0
Mono	mono	logic 0 (no stereo received)	1
Mono	mono	logic 0 (no stereo received)	0

Table 10 Mute setting

FUNCTION	DATA
MUTE CONTROL FOR OUTR AND OUTL	**E1**
Forced mute at OUTR and OUTL	1
No forced mute at OUTR and OUTL	0

Table 11 AVLON bit setting

FUNCTION	DATA
AVL	**E2**
Automatic volume control **on**	1
Automatic volume control **off**	0

Table 12 CCD bit setting

FUNCTION	DATA
AVL CURRENT	**E3**
Increased load current	1
Load current for normal AVL decay time	0

Table 13 AVL attack time; see Chapter “Characteristics” note 5

FUNCTION	DATA	
R_{att} (Ω)	E5	E4
420	0	0
730	0	1
1200	1	0
2100	1	1

Table 14 Line out mute setting

FUNCTION	DATA
MUTE LINE OUTPUT	**E6**
Line output mute	1
Line output active	0

Table 15 Tone setting

FUNCTION	DATA	
TONE	F1	F0
Maximum bass and maximum treble	1	1
Maximum bass and minimum treble	1	0
Minimum bass and maximum treble	0	1
Minimum bass and minimum treble	0	0

Table 16 Selector setting

FUNCTION	DATA
MODE INTERNAL/EXTERNAL	**F2**
External left and right	1
Internal left and right	0

Table 17 Mono setting

FUNCTION	DATA
MONO AT OUTL AND OUTR	**F3**
Forced mono	1
No forced mono	0

Table 18 Linear setting

FUNCTION	DATA
MODE TONE	**F4**
Linear	1
Tone	0

INTERNAL PIN CONFIGURATIONS

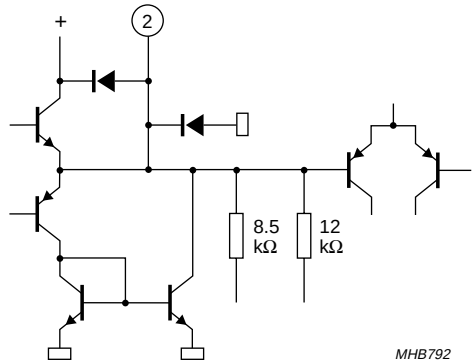


Fig.4 Pin 2: C_{P2}.

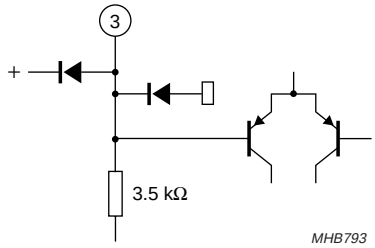


Fig.5 Pin 3: C_{P1}.

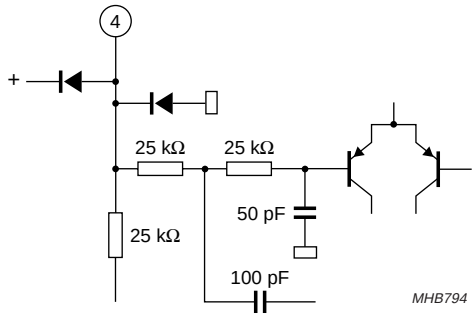


Fig.6 Pin 4: COMP.

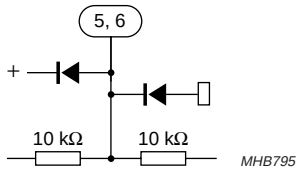


Fig.7 Pin 5: C_{MO}; pin 6: C_{SS}.

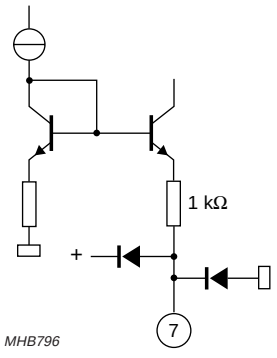


Fig.8 Pin 7: R_{FR}.

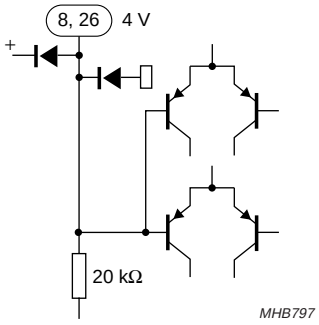


Fig.9 Pin 8: LIL; pin 26: LIR.

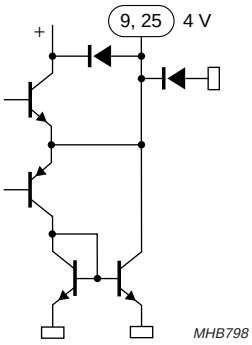


Fig.10 Pin 9: LOL; pin 25: LOR.

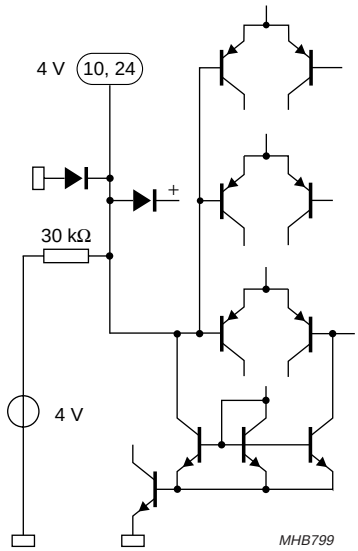


Fig.11 Pin 10: VIL; pin 24: VIR.

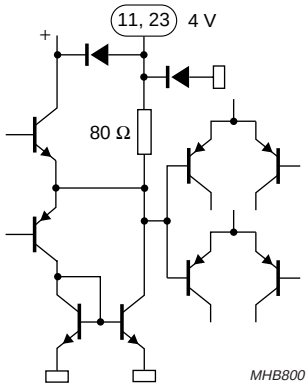


Fig.12 Pin 11: VAL; pin 23: VAR.

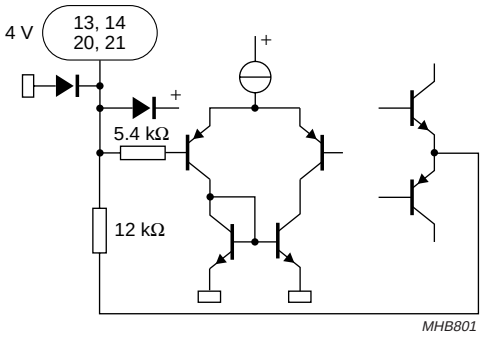


Fig.13 Pin 13: TC1L; pin 14: TC2L; pin 20: TC2R; pin 21: TC1R.

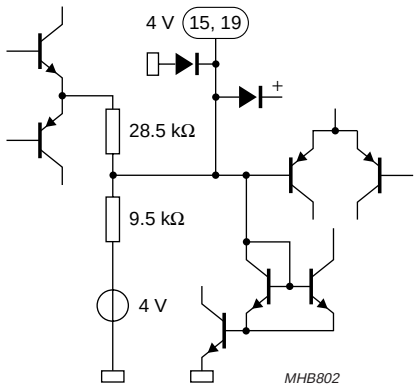


Fig.14 Pin 15: BCL; pin 19: BCR.

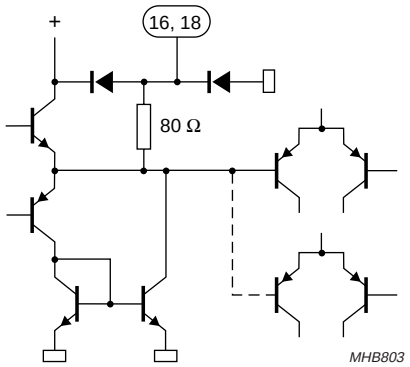


Fig.15 Pin 16: OUTL; pin 18: OUTR.

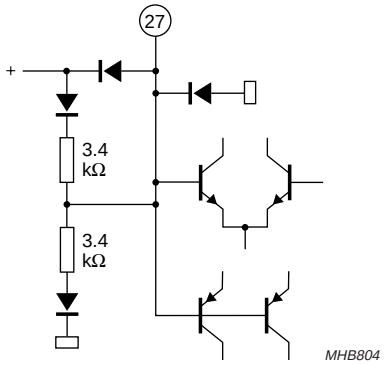


Fig.16 Pin 27: V_{ref}.

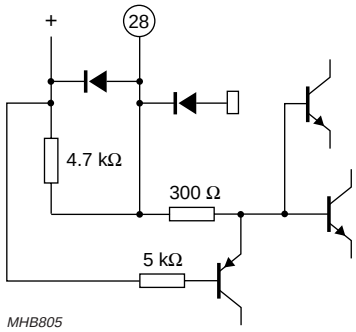


Fig.17 Pin 28: V_{CAP}.

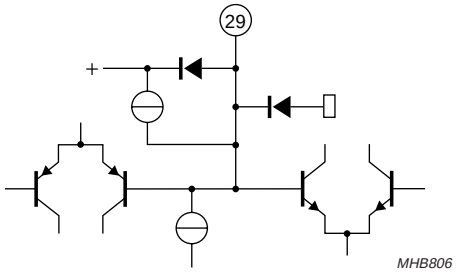


Fig.18 Pin 29: C_{AV}.

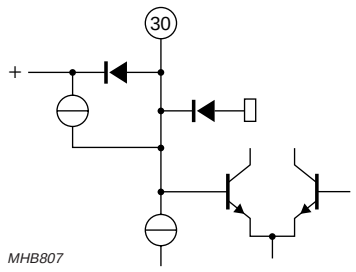


Fig.19 Pin 30: TW.

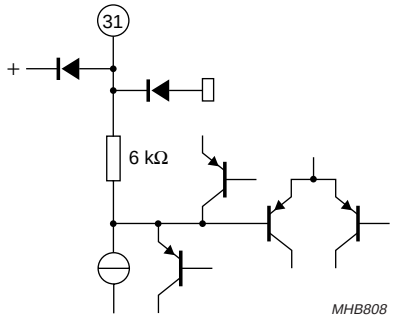


Fig.20 Pin 31: C_W.

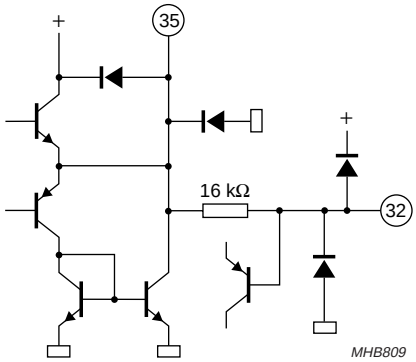


Fig.21 Pin 32: BPU; pin 35: FDI.

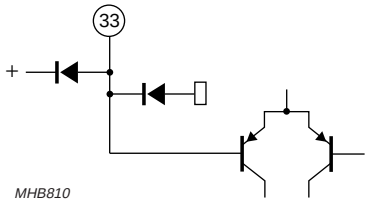


Fig.22 Pin 33: FDO.

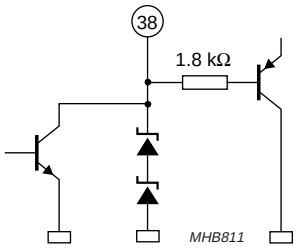


Fig.23 Pin 38: SDA.

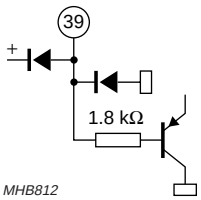


Fig.24 Pin 39: MAD (I²C-bus address switch).

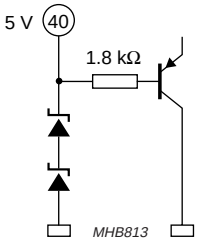


Fig.25 Pin 40: SCL.

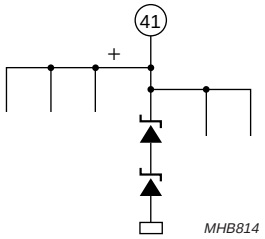


Fig.26 Pin 41: V_{CC}.

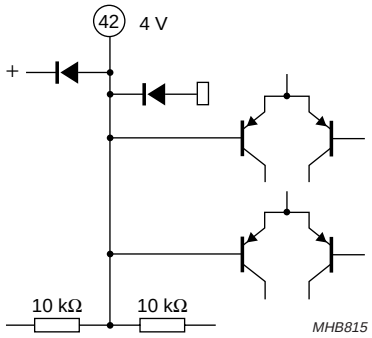


Fig.27 Pin 42: C_{PH}.

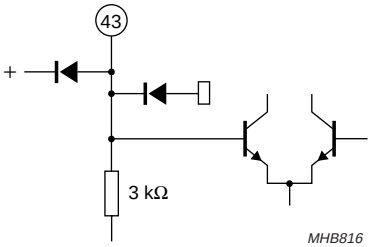
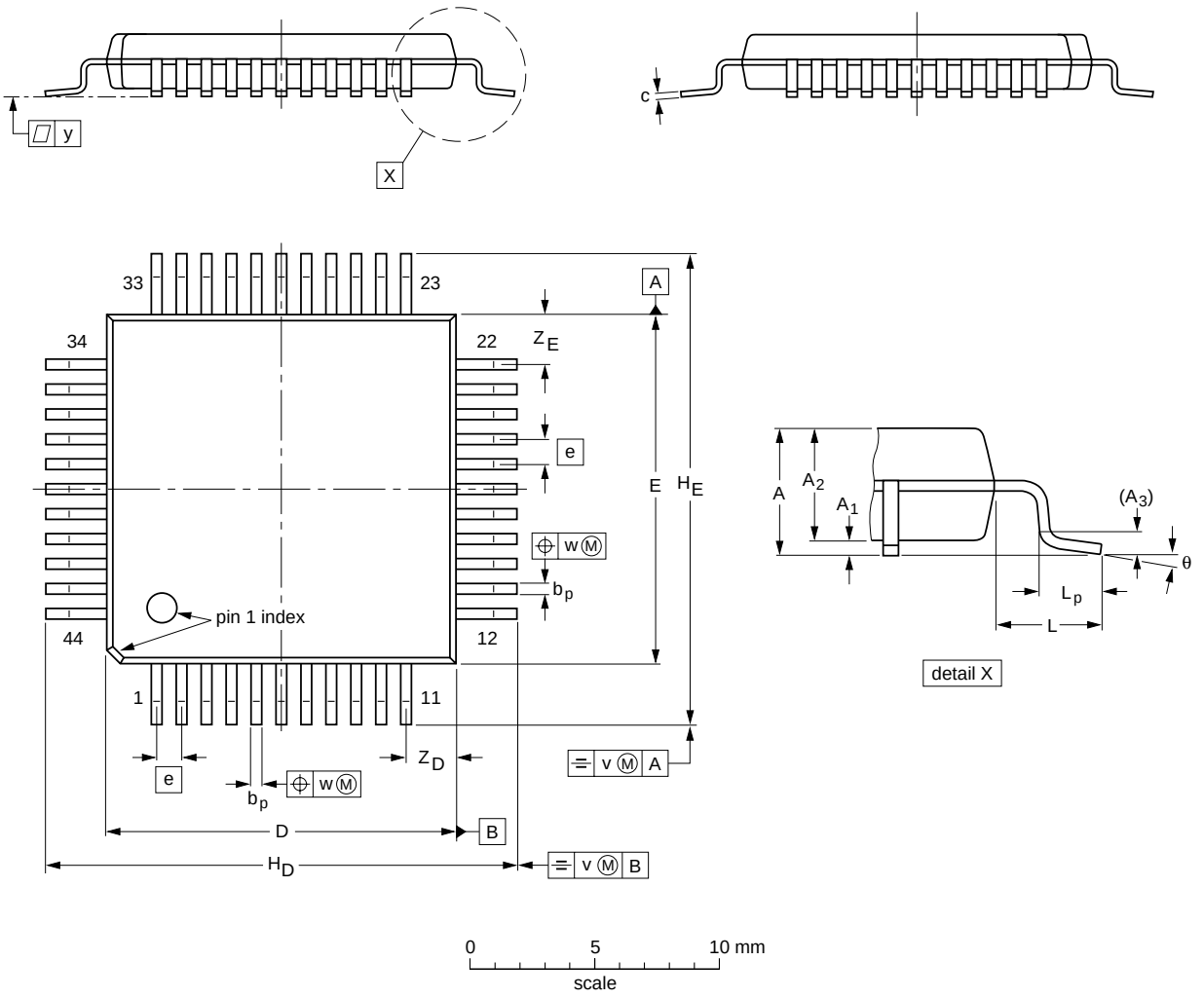


Fig.28 Pin 43: CER.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01					~~97-08-01~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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