TDA7491P
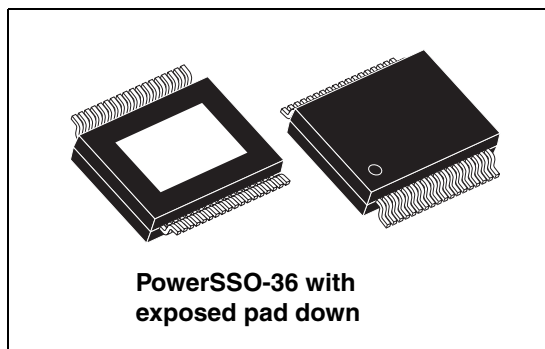
10 W + 10 W dual BTL class-D audio amplifier

Features

- 10 W + 10 W continuous output power:
  $R_L = 6\ \Omega$, THD = 10% at $V_{CC} = 11$ V
- 9.5 W + 9.5 W continuous output power:
  $R_L = 8\ \Omega$, THD = 10% at $V_{CC} = 12$ V
- Wide range single supply operation (5 V - 18 V)
- High efficiency ($\eta = 90\%$)
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No 'pop' at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable

PowerSSO-36 with exposed pad down

Description

The TDA7491P is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no separate heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

The TDA7491P is pin to pin compatible with the TDA7491LP and TDA7491HV.

Table 1.   Device summary

Order code	Operating temperature	Package	Packaging
TDA7491P	0 to 70 °C	PowerSSO-36 EPD	Tube
TDA7491P13TR	0 to 70 °C	PowerSSO-36 EPD	Tape and reel

Contents

List of tables

List of figures

1   Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491P.

Figure 1.   Internal block diagram (one channel only)
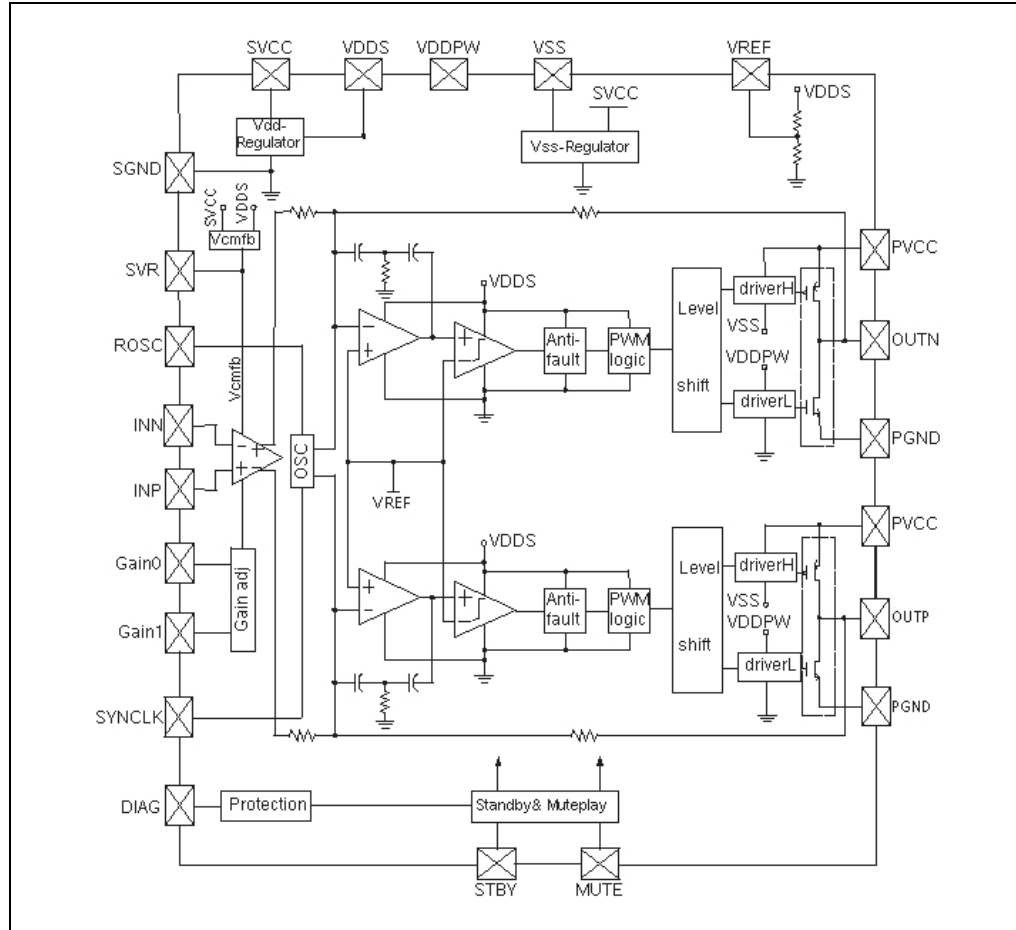
2 Pin description

2.1 Pin out

Figure 2. Pin connection (top view, PCB view)

Pin	Left signal	Pin	Right signal
1	SUB_GND	36	VSS
2	OUTPB	35	SVCC
3	OUTPB	34	VREF
4	PGNDB	33	INNB
5	PGNDB	32	INPB
6	PVCCB	31	GAIN1
7	PVCCB	30	GAIN0
8	OUTNB	29	SVR
9	OUTNB	28	DIAG
10	OUTNA	27	SGND
11	OUTNA	26	VDDS
12	PVCCA	25	SYNCLK
13	PVCCA	24	ROSC
14	PGNDA	23	INNA
15	PGNDA	22	INPA
16	OUTPA	21	MUTE
17	OUTPA	20	STBY
18	PGND	19	VDDPW

EP
exposed pad down
Connect to ground
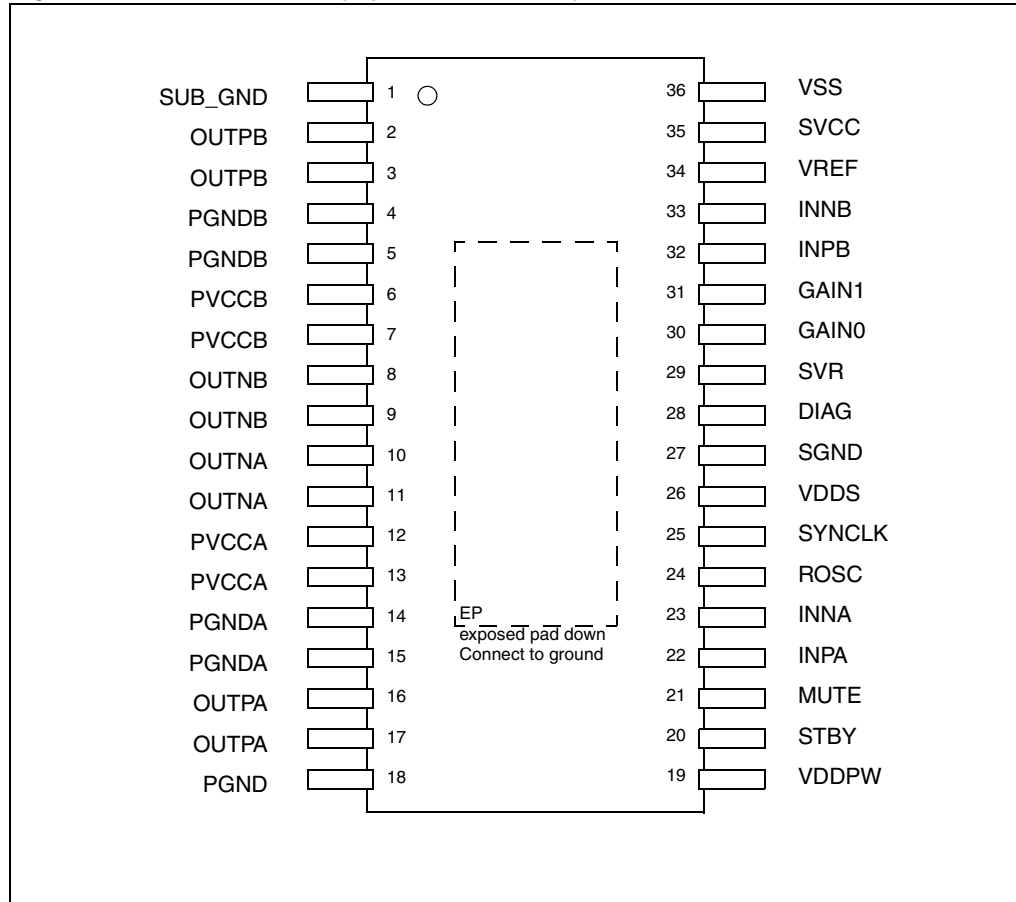
2.2 Pin list

Table 2. Pin description list

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM for right channel
4,5	PGNDB	POWER	Power stage ground for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for right channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage ground for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage ground
19	VDDPW	OUT	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for ground-plane heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage for pins PVCCA, PVCCB, SVCC	20	V
T_{op}	Operating temperature	0 to 70	°C
T_j	Junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient (mounted on recommended PCB)[1]	-	24	-	

1. FR4 with vias to copper area of 9 cm^2 (see also *Section 7.9: Heatsink requirements on page 38*).

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 5* below are given for the conditions:
V_{CC} = 11 V, R_L (load) = 6 Ω, R_{OSC} = R3 = 39 kΩ, C8 = 100 nF, f = 1 kHz, G_V = 20 dB, and Tamb = 25 °C.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB, SVCC	-	5	-	18	V
I_q	Total quiescent current	Without LC filter	-	26	35	mA
I_{qSTBY}	Quiescent current in standby	-	-	2.5	5.0	µA
V_{OS}	Output offset voltage	Play mode	-150	-	150	mV
V_{OS}	Output offset voltage	Mute mode	-60	-	60	mV
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	3	5	-	A
T_j	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	55	60	-	kΩ
V_{OVP}	Overvoltage protection threshold	-	19	21	-	V

Table 5.   **Electrical specifications (continued)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVP}	Undervoltage protection threshold	-	-	-	4	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	10	-	W
		THD = 1%	-	8.0	-	
P_o	Output power	$R_L = 8\ \Omega$, THD = 10% $V_{CC} = 12$ V	-	9.5	-	W
		$R_L = 8\ \Omega$, THD = 1% $V_{CC} = 12$ V	-	7.2	-	
P_D	Dissipated power	$P_o = 10$ W + 10 W, THD = 10%	-	2.0	-	W
η	Efficiency	$P_o = 10$ W + 10 W	80	90	-	%
THD	Total harmonic distortion	$P_o = 1$ W	-	0.1	0.2	%
G_V	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG_V	Gain matching	-	-1	-	1	dB
CT	Cross talk	f = 1 kHz	-	50	-	dB
eN	Total input noise	A Curve, G_V = 20 dB	-	20	-	µV
		f = 22 Hz to 22 kHz	-	25	35	
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 V, $C_{SVR} = 10$ µF	40	50	-	dB
T_r, T_f	Rise and fall times	-	-	50	-	ns
f_{SW}	Switching frequency	Internal oscillator	290	310	330	kHz
f_{SWR}	Output switching frequency	With internal oscillator [1]	250	-	-	kHz
		With external oscillator [2]	250	-	-	
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	$V_{MUTE} = 1$ V	60	80	-	dB
Function mode	Standby, mute and play modes	V_{STBY} < 0.5 V, V_{MUTE} = X	Standby			-
		V_{STBY} > 2.5 V, V_{MUTE} < 0.8 V	Mute			-
		V_{STBY} > 2.5 V, V_{MUTE} > 2.5 V	Play			-

1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R3 = 39 kΩ (see *Figure 49.*).

2. $f_{SW} = f_{SYNCLK} / 2$ with the frequency of the external oscillator.

4 Characterization curves

The following characterization curves were made using the TDA7491P demo board. The LC filter for the 4-Ω load uses components of 15 µH and 470 nF, whilst that for the 6-Ω load uses 22 µH and 220 nF and that for the 8-Ω load uses 33 µH and 220 nF.

All other test conditions are given along side the corresponding curves.

4.1 With 4-Ω load at V_{CC} = 10 V

Figure 3.   THD vs output power (1 kHz)

Test Condition:

Vcc=10V,

RL=4 ohm,

Rosc=39kΩ, Cosc=100nF,

f =1kHz,

Gv=30dB,

Tamb=25℃

Specification Limit:

Typical:

Po=10W @ THD=10%
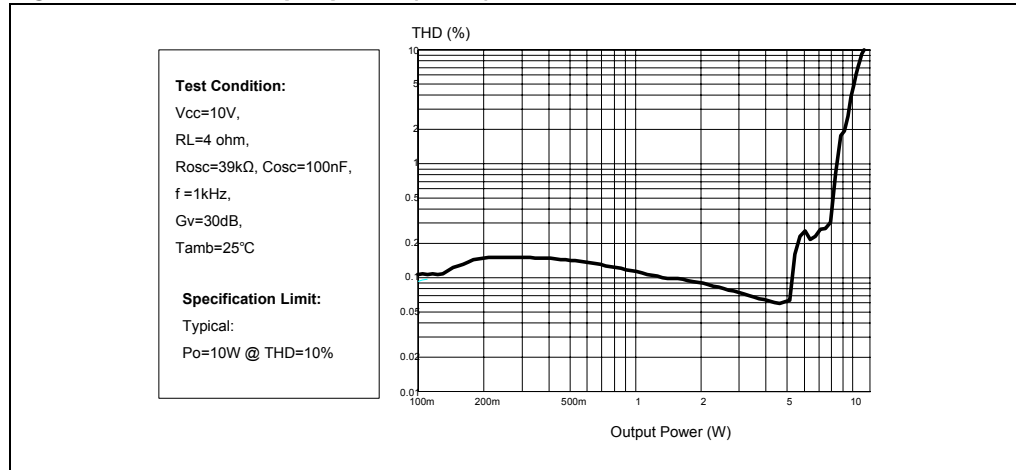
Figure 4.   THD vs output power (100 Hz)

Test Condition:

Vcc=10V,

 RL=4 ohm,

Rosc=39kΩ, Cosc=100nF,

f =100Hz,

Gv=30dB,

Tamb=25℃

Specification Limit:

Typical:

10W @ THD=10%
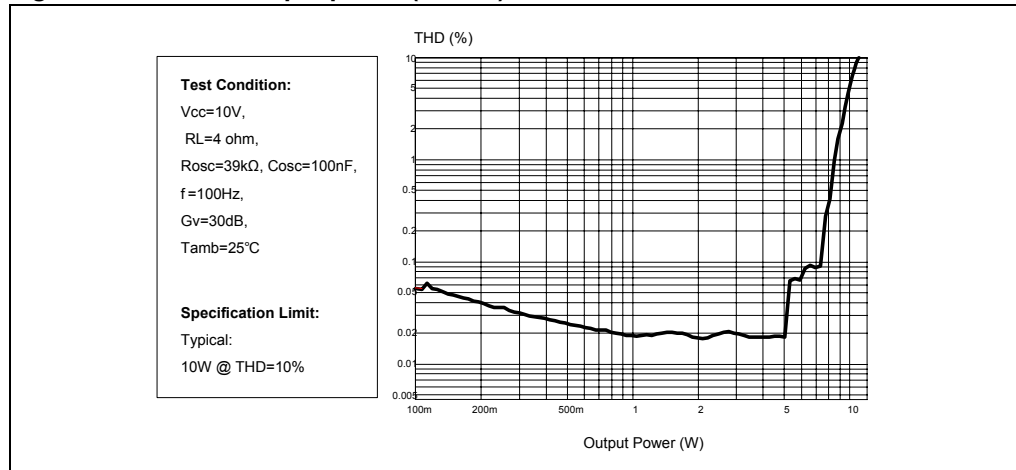
Figure 5.   THD vs frequency

Test Condition:

Vcc=10V,

RL=4 ohm,

Rosc=39kΩ, Cosc=100nF,

f = 1kHz,

Gv=30dB,

Po=1W

Tamb=25℃

Specification Limit:

Typical: THD <0.5%
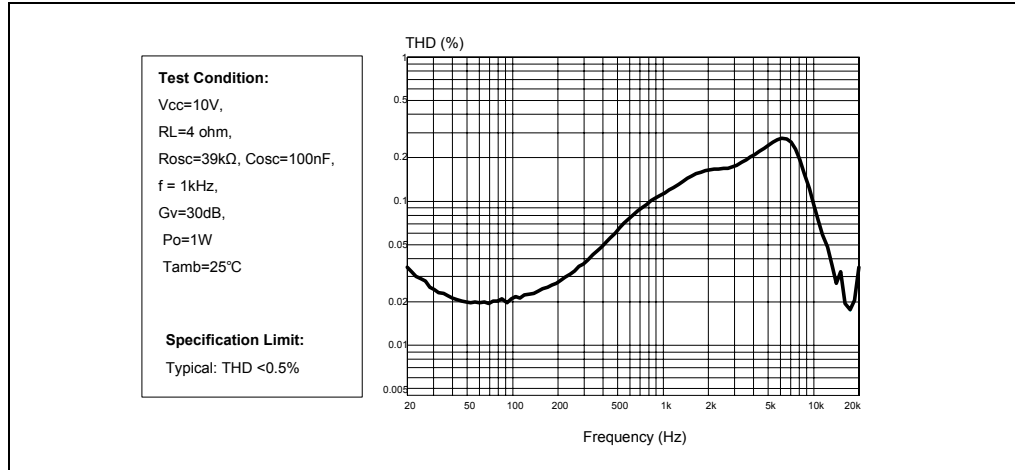
Figure 6.   Frequency response

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc=39kΩ, Cosc=100nF,

f = 1kHz,

Gv = 30dB,

Po =1W

Tamb = 25℃

Specification Limit:

Max: +/-3dB

@20Hz to 20kHz
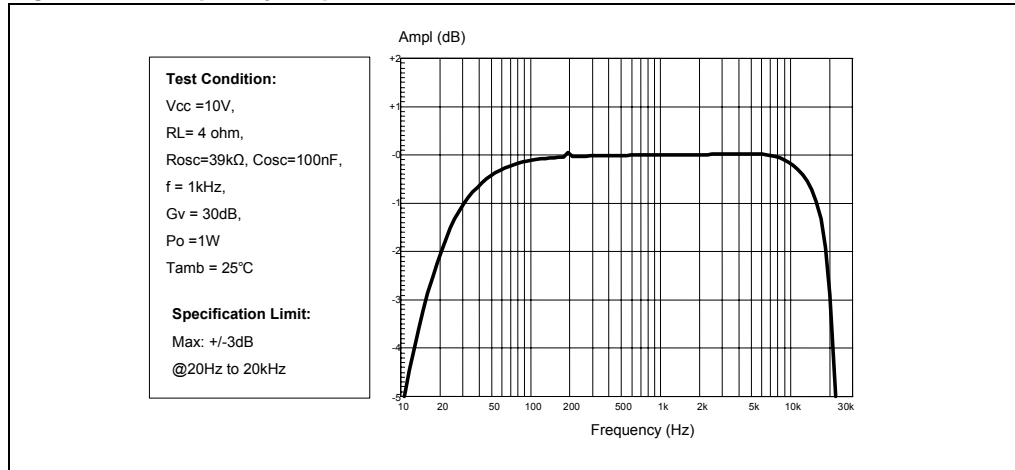
Figure 7.   Crosstalk vs frequency

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc= 39kΩ, Cosc = 100nF,

f = 1kHz,

Gv = 30dB,

Po = 1W

Tamb = 25℃

Specification Limit:

Typical: >50dB (@ f = 1kHz)

Figure 8. FFT (0 dB)

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc =100nF,

f =1kHz,

Gv = 30dB,

Po = 1W

Tamb = 25℃

Specification Limit:

Typical: >60dB

for the harmonic   frequency

Figure 9. FFT (-60 dB)

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

f = 1kHz,

Gv=30dB,

Po= -60dB (@ 1W =0dB)

Tamb=25℃

Specification Limit:

Typical: > 90dB

for the harmonic   frequency

Figure 10. Power supply rejection ratio vs frequency

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

Vin=0,

Gv=30dB,

0dB refers to 500mV, 100Hz,

Tamb=25℃

Ripple frequency=100Hz

Ripple voltage=500mV
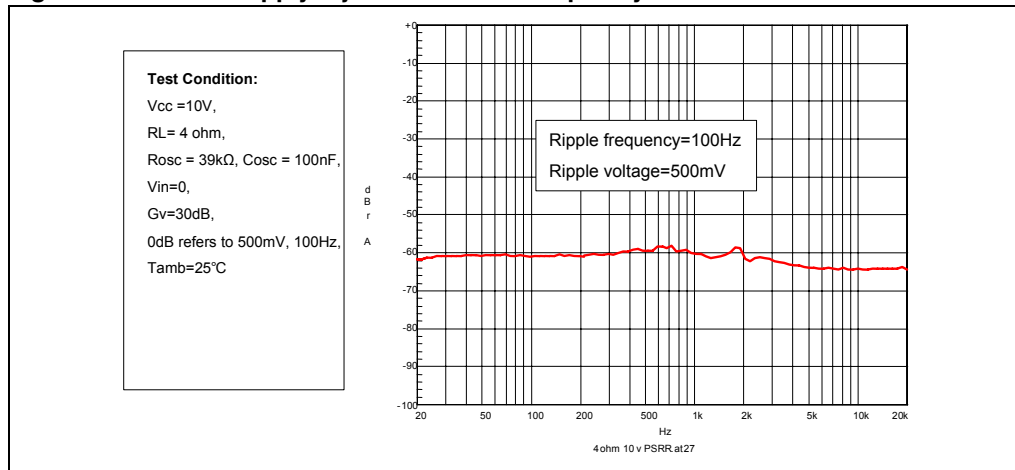
Figure 11.   Power dissipation and efficiency vs output power

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

f = 1kHz,

Gv=30dB,

Tamb=25℃

Vcc=10V
Rload=4ohm
Gain=30dB
f=1kHz
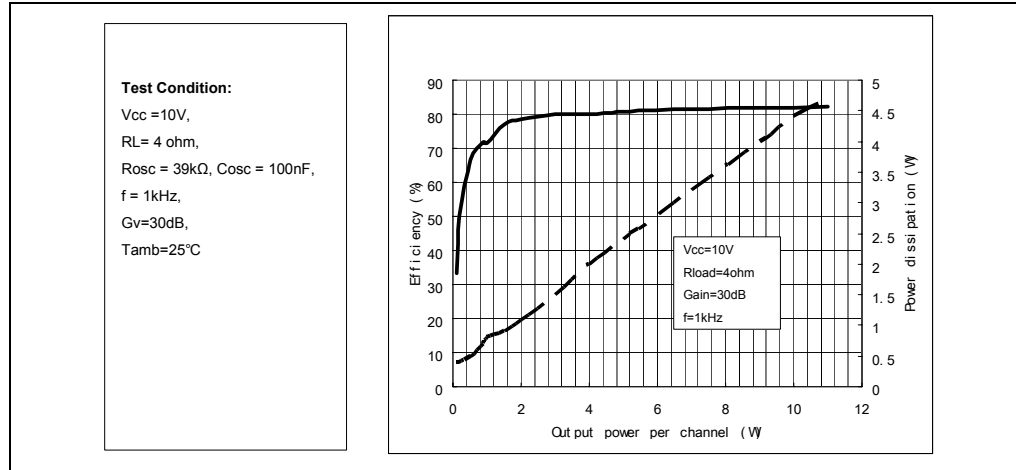
Figure 12.   Closed-loop gain vs frequency

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

f = 1kHz,

0dB@f=1kHz, Po=1w,
Gain=32dB,

Tamb=25℃

Gain=26dB   Gain=30dB

Gain=22dB   Gain=32dB
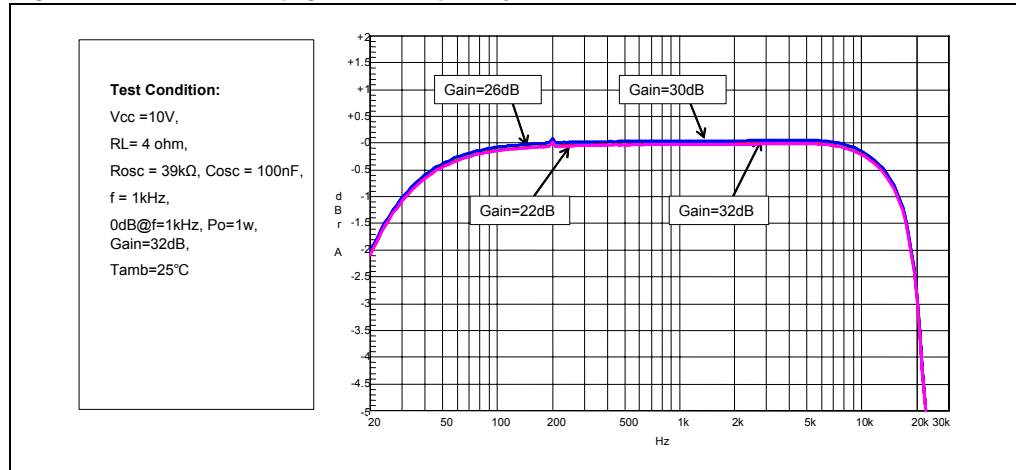
Figure 13.   Current consumption vs voltage on pin MUTE

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

Vin=0,

Gv=30dB,

Tamb=25℃

Vcc=10V
Rload=4ohm
Gain=30dB
Vin=0
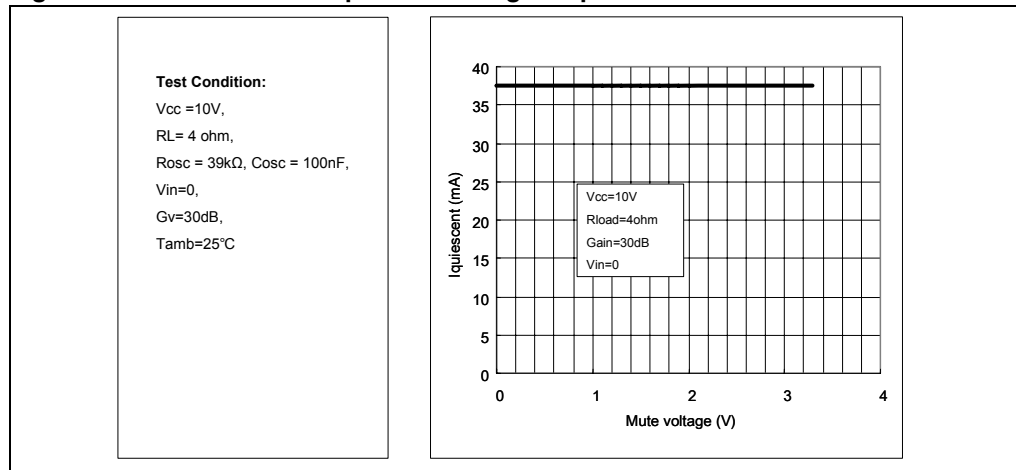
Figure 14. Attenuation vs voltage on pin MUTE

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

0dB@f=1kHz,Po=1w,

Gv=30dB,

Tamb=25℃

Vcc=10V
Rload=4ohm
Gain=30dB
0dB@f=1kHz, Po=1w

Attenuation (dB) / *Mute voltage (V)*
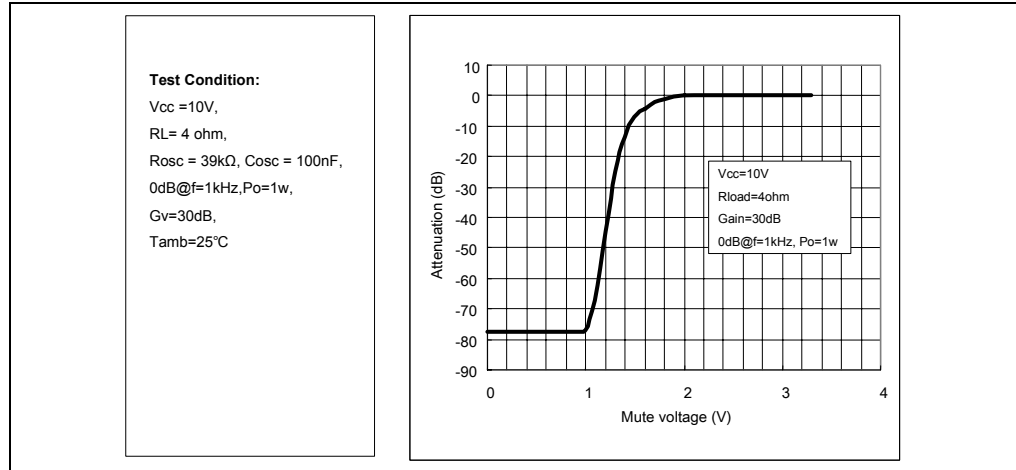
Figure 15. Current consumption vs voltage on pin STBY

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

Vin=0,

Gv=30dB,

Tamb=25℃

Vcc=10V
Rload=4ohm
Gain=30dB
Vin=0

Iquiescent (mA) / *Standby voltage (V)*
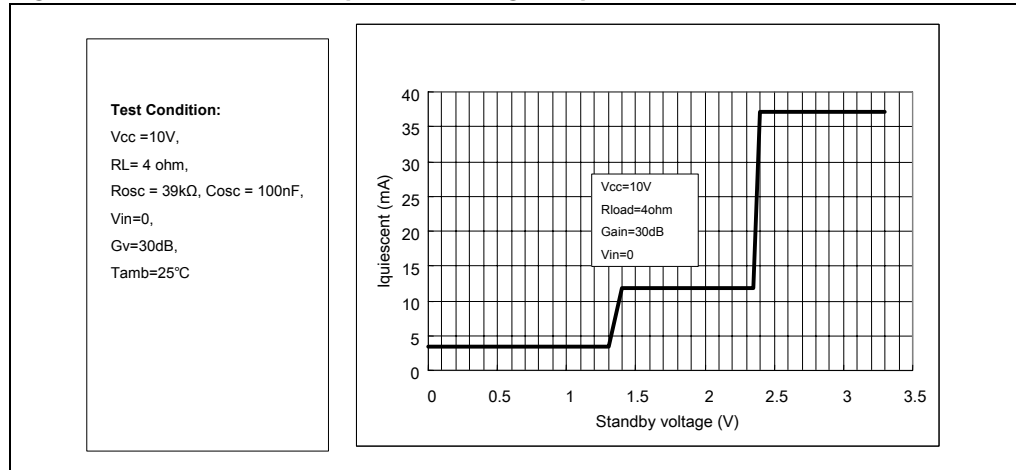
Figure 16. Attenuation vs voltage on pin STBY

Test Condition:

Vcc =10V,

RL= 4 ohm,

Rosc = 39kΩ, Cosc = 100nF,

0dB@f=1kHz,Po=1w,

Gv=30dB,

Tamb=25℃

Vcc=10V
Rload=4ohm
Gain=30dB
0dB@f=1kHz, Po=1w

Attenuation (dB) / *Standby voltage (V)*
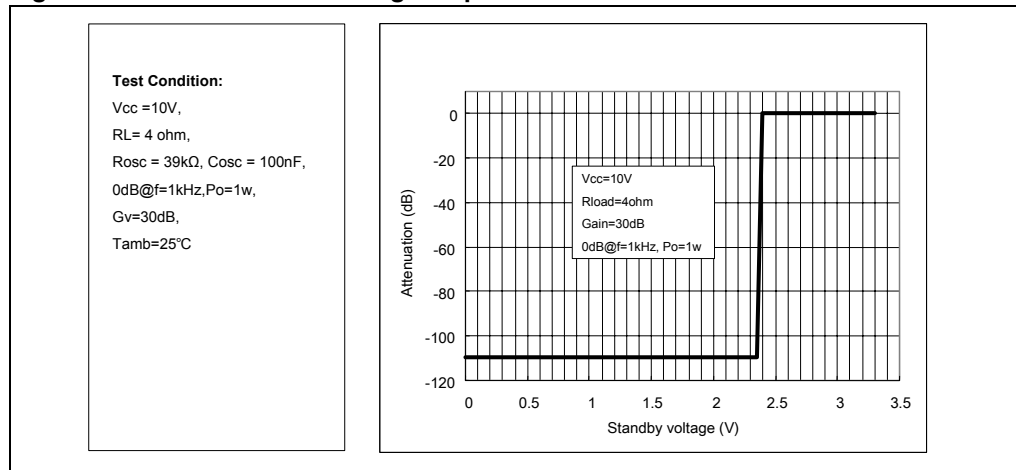
4.2   With 6-Ω load at V_{CC} = 11 V

Figure 17.   Output power vs supply voltage

Test Condition :
Vcc = 5~11V,
RL = 6 ohm,
Rosc = 39kO, Cosc = 100nF,
f =1kHz,
Gv = 30dB,
Tamb = 25℃

Specification Limit:
Typical:
Vs =11V,Rl =6 ohm
Po =10W @THD=10%
Po =8W @THD=1%

Figure 18.   THD vs output power (1 kHz)

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Tamb =25℃

 Specification Limit:
 Typical:
  Po=10W @ THD=10%
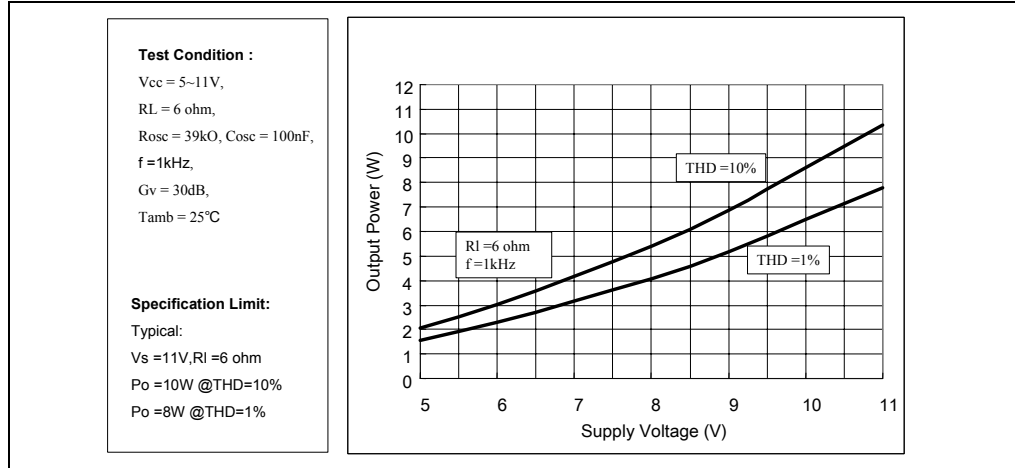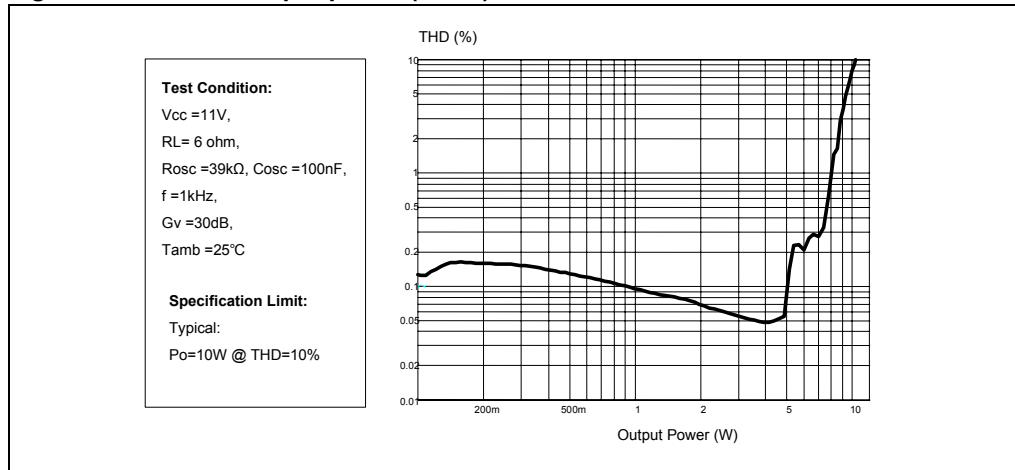
Figure 19.   THD vs output power (100 Hz)

Test Condition:
Vcc =11V,
 RL = 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f =100Hz,
Gv =30dB,
Tamb =25℃

Specification Limit:
Typical:
10W @ THD =10%

Figure 20.   THD vs frequency

Test Condition:
Vcc =11V,
RL= 6 ohm,
Ros c=39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
 Po =1W
 Tamb =25℃

Specification Limit:
Typical: THD<0.5%
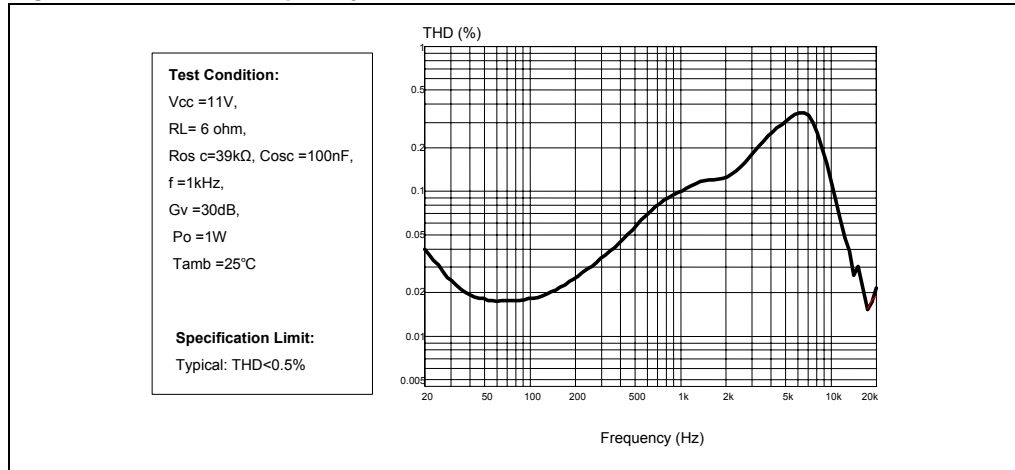
Figure 21.   Frequency response

Test Condition:
Vcc=11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv =30dB,
Po =1W
Tamb =25℃

Specification Limit:
Max: +/-3dB
@20Hz to 20kHz
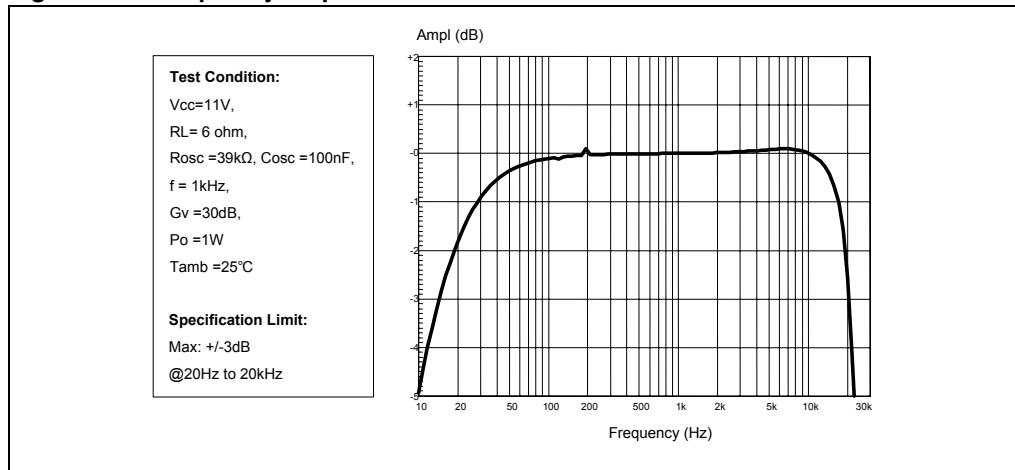
Figure 22. Crosstalk vs frequency

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv =30dB,
Po =1W
Tamb=25℃

Specification Limit:
Typical: >50dB (@ f =1kHz)

Figure 23. FFT (0 dB)

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Po =1W
Tamb =25℃

Specification Limit:
Typical: >60dB
for the harmonic frequency

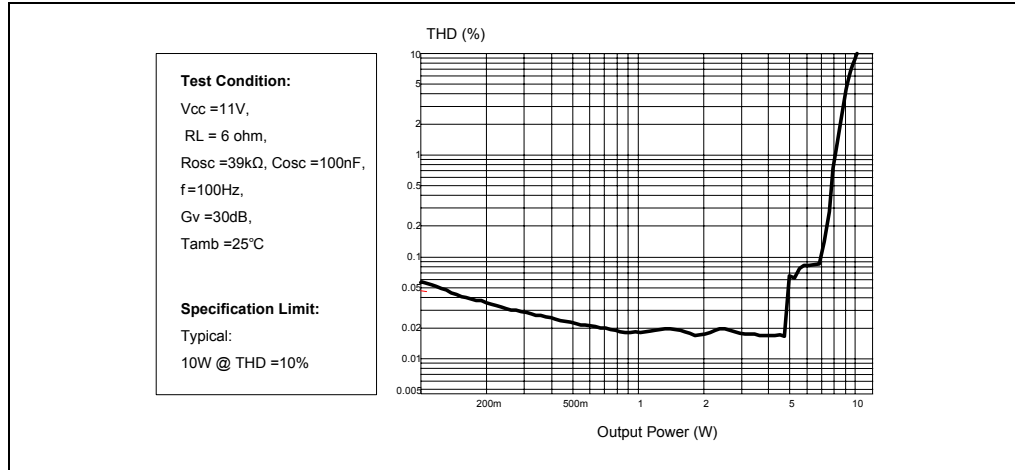**Figure 24. FFT (-60 dB)**

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Po = -60dB (@ 1W =0dB)
Tamb =25℃

Specification Limit:
Typical: > 90dB
for the harmonic frequency
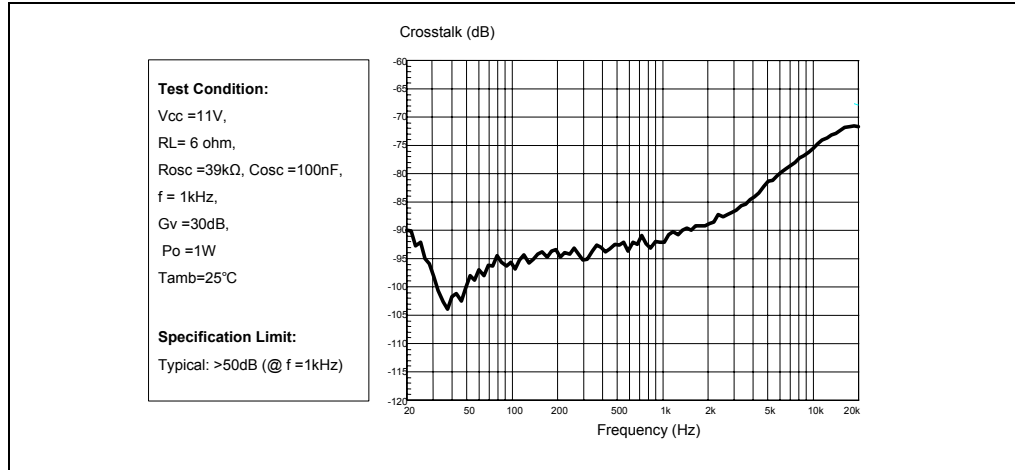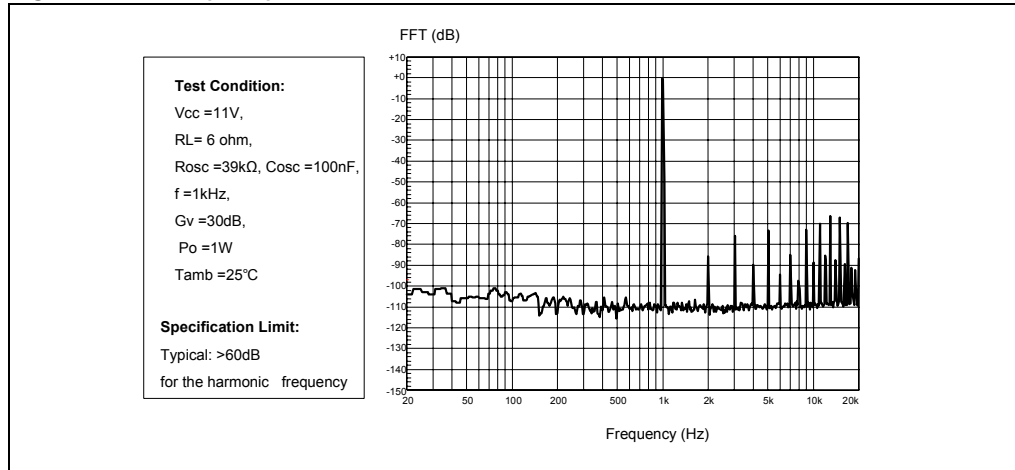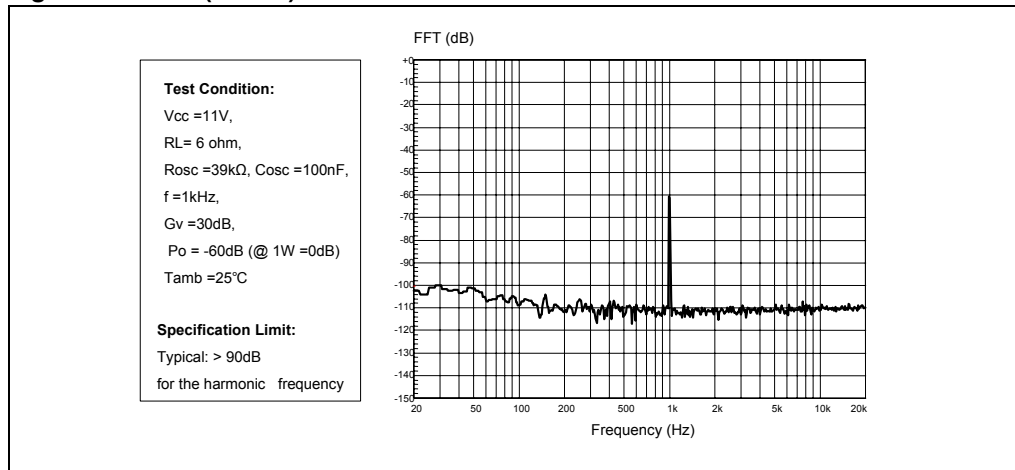
Figure 25. Power supply rejection ratio vs frequency

Test Condition:

Vcc =11V,

RL= 6 ohm,

Rosc =39kΩ, Cosc =100nF,

Vin=0,

Gv =30dB,

0dB refers to 500mV, 100Hz,

Tamb =25℃

Ripple frequency=100Hz

Ripple voltage=500mV

6ohm 11v PSRR.at27

Figure 26. Power dissipation and efficiency vs output power

Test Condition:

Vcc =11V,

RL= 6 ohm,

Rosc =39kΩ, Cosc =100nF,

F=1kHz,

Gv =30dB,

Tamb =25℃

Vcc=11V

Rload=6ohm

Gain=30dB

f=1kHz
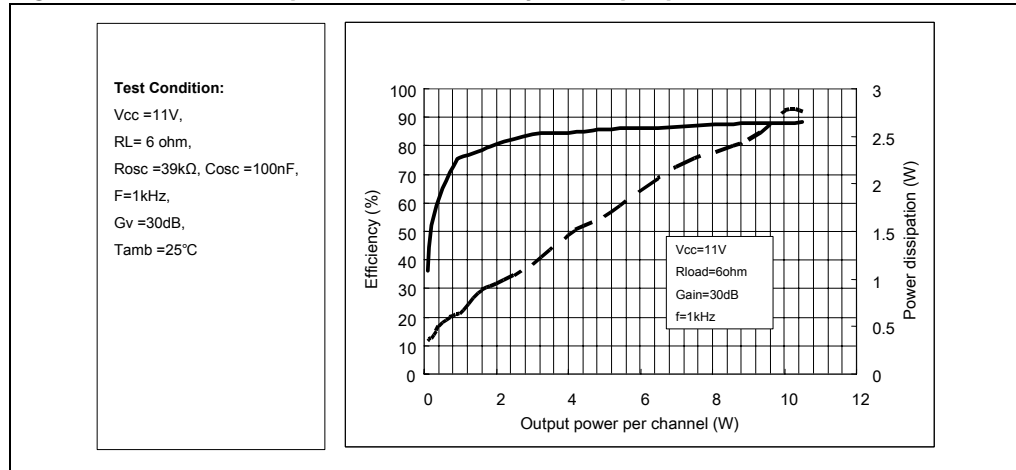
Figure 27. Closed-loop gain vs frequency

Test Condition:

Vcc =11V,

RL= 6 ohm,

Rosc =39kΩ, Cosc =100nF,

0dB@f=1kHz,Po=1w,
Gain=32dB,

Tamb =25℃

Gain=32dB

Gain=22dB

Gain=26dB

Gain=30dB
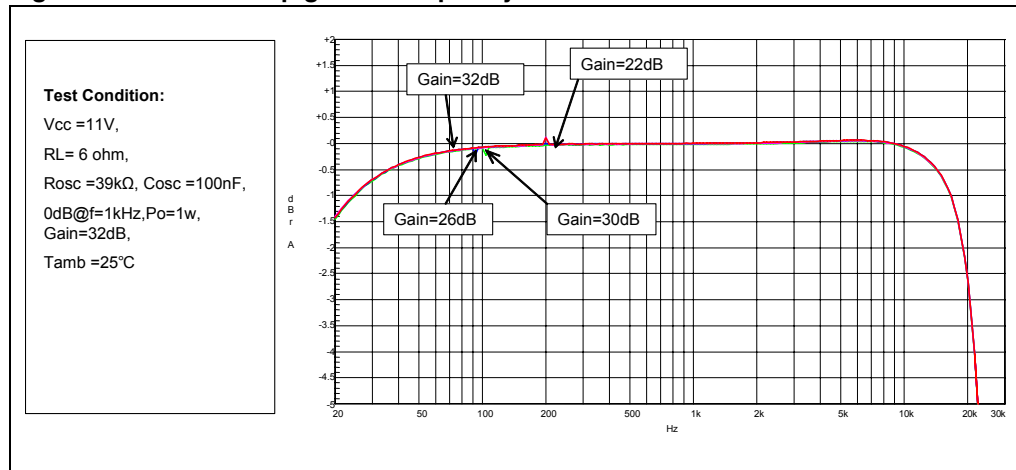
Figure 28.   Current consumption vs voltage on pin MUTE

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
Vin=0,
Gv =30dB,
Tamb =25℃

Vcc=11V
Rload=6ohm
Gain=30dB
Vin=0

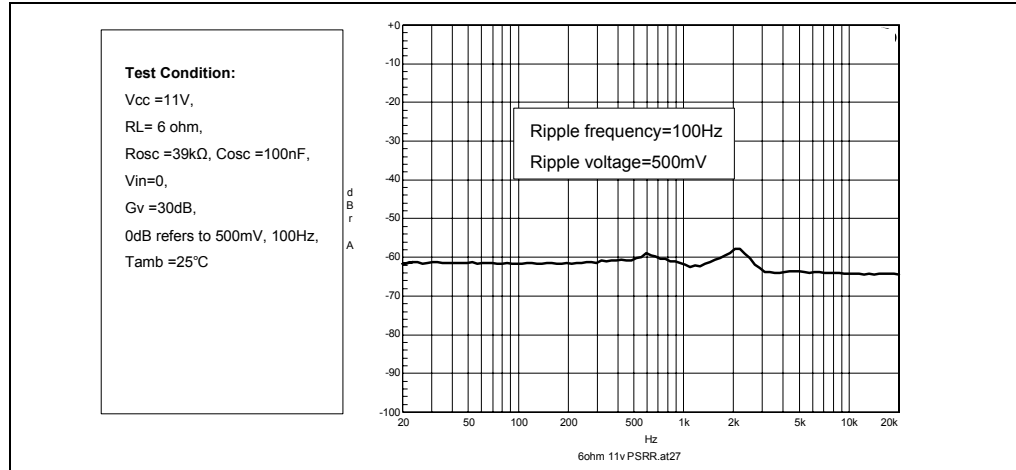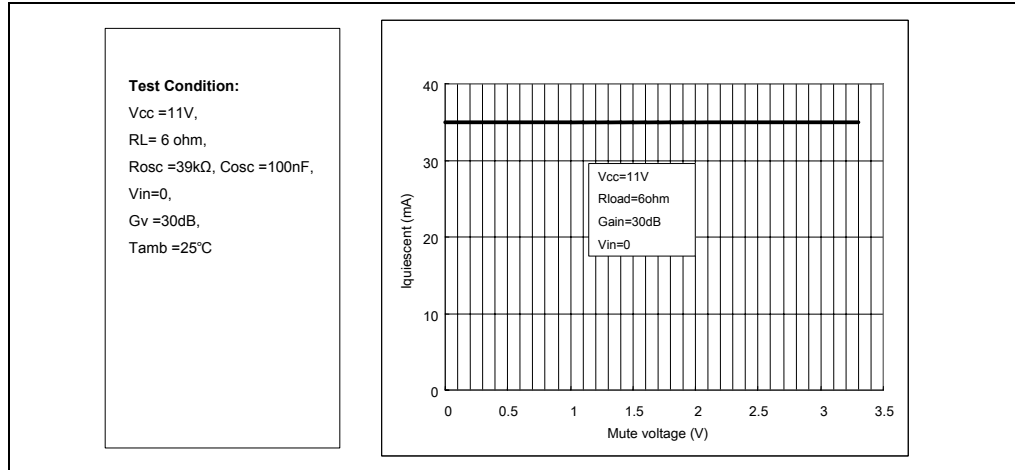**Figure 29.   Attenuation vs voltage on pin MUTE**

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
 f=1kHz,
0dB@f=1kHz, Po=1w,
Gv =30dB,
Tamb =25℃

Vcc=11V
Rload=6ohm
Gain=30dB
0dB@f=1kHz, Po=1w
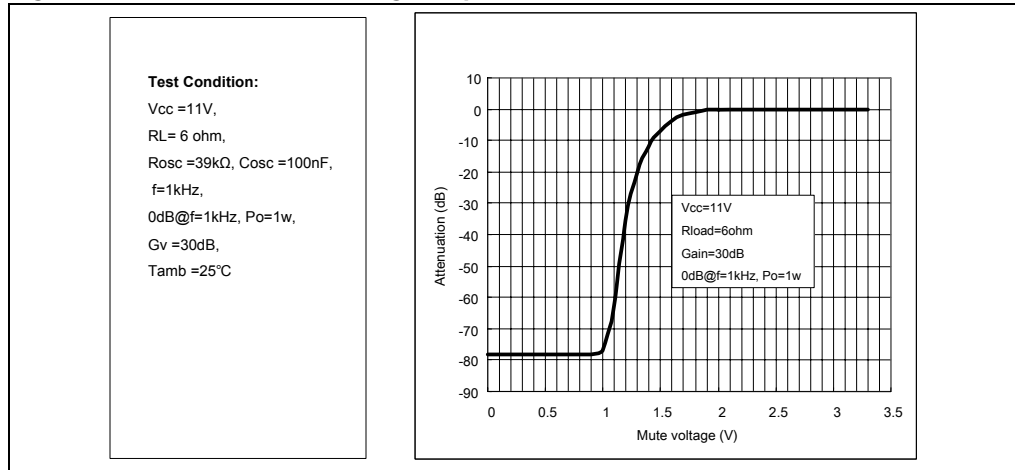
Figure 30.   Current consumption vs voltage on pin STBY

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
Vin=0,
Gv =30dB,
Tamb =25℃

Vcc=11V
Rload=6ohm
Gain=30dB
Vin=0
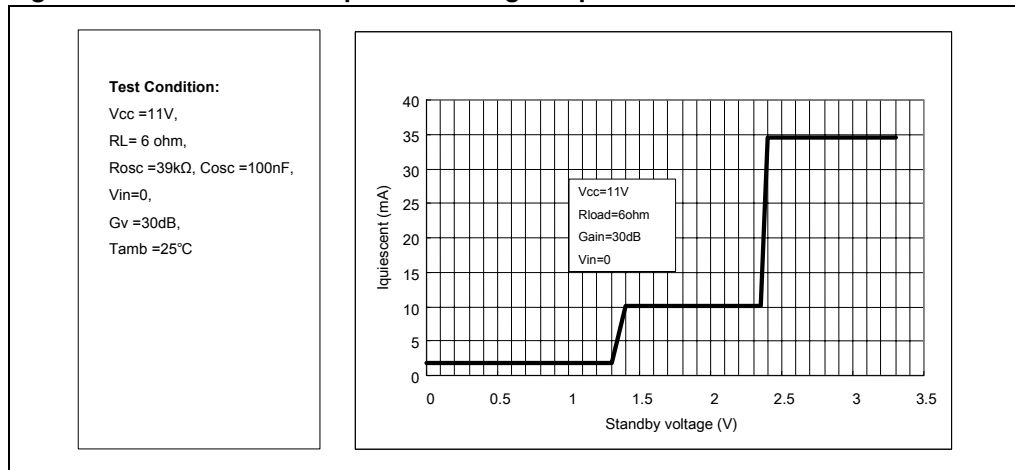
Figure 31. Attenuation vs voltage on pin STBY

Test Condition:
Vcc =11V,
RL= 6 ohm,
Rosc =39kΩ, Cosc =100nF,
 f=1kHz,
0dB@f=1kHz, Po=1w,
Gv =30dB,
Tamb =25℃

Vcc=11V
Rload=6ohm
Gain=30dB
0dB@f=1kHz, Po=1w
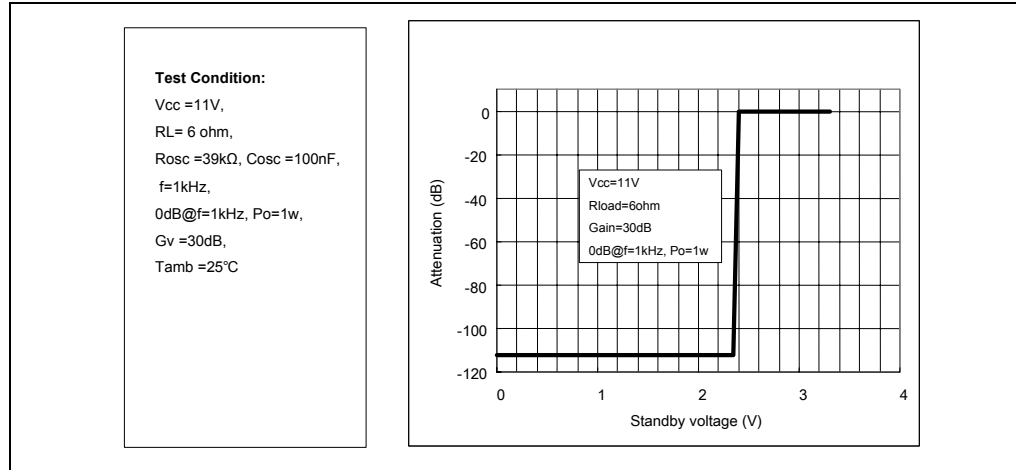
4.3 With 8-Ω load at V_{CC} = 12 V

Figure 32. Output power vs supply voltage

Test Condition :
Vcc = 5~12V,
RL = 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Tamb =25℃

Specification Limit:
Typical:
Vs =12V,Rl = 8 ohm
Po =9.5W @THD =10%
Po =7.2W @THD =1%

THD =10%
Rl =8 ohm
f =1kHz
THD =1%
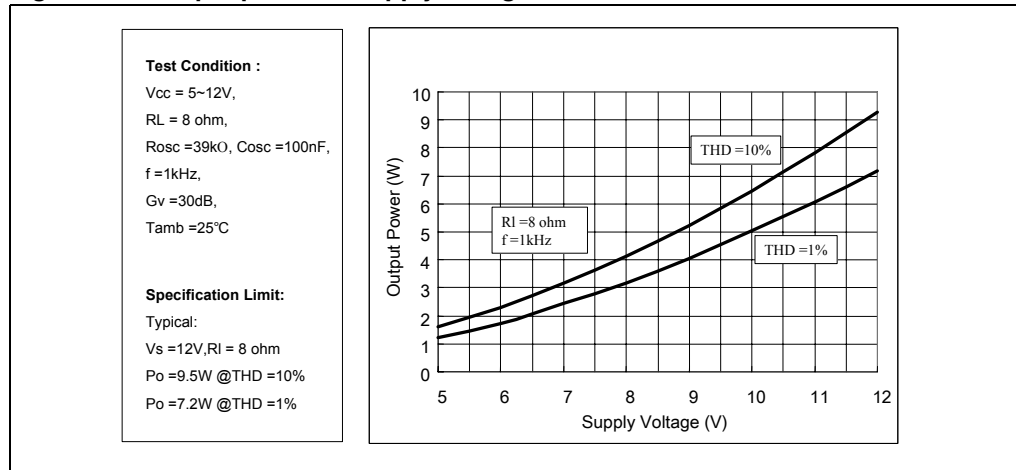
Figure 33.   THD vs output power (1 kHz)

THD (%)

Test Condition:

Vcc =12V,

RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =1kHz,

Gv =30dB,

Tamb =25℃

Specification Limit:

Typical:

Po =9.5W @ THD =10%
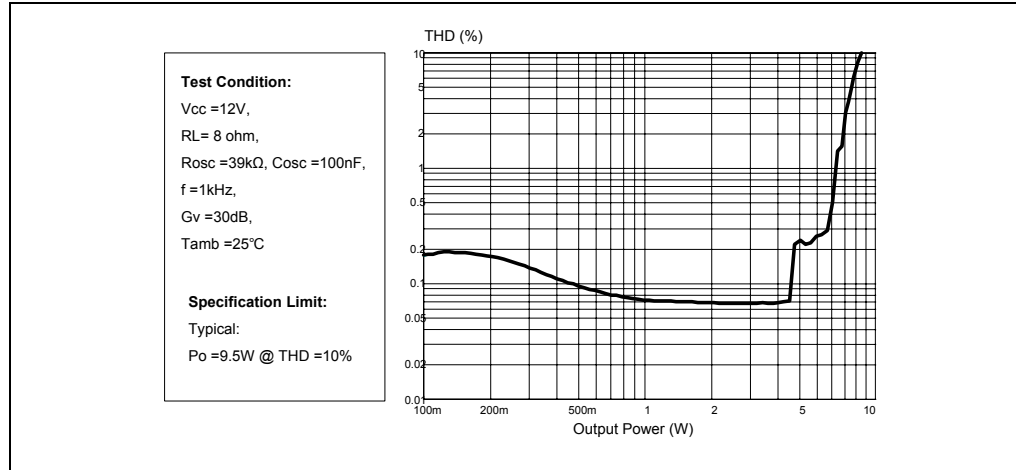
Output Power (W)

Figure 34.   THD vs output power (100 Hz)

THD (%)

Test Condition:

Vcc =12V,

 RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =100Hz,

Gv =30dB,

Tamb =25℃

Specification Limit:

Typical:

9.5W @ THD =10%
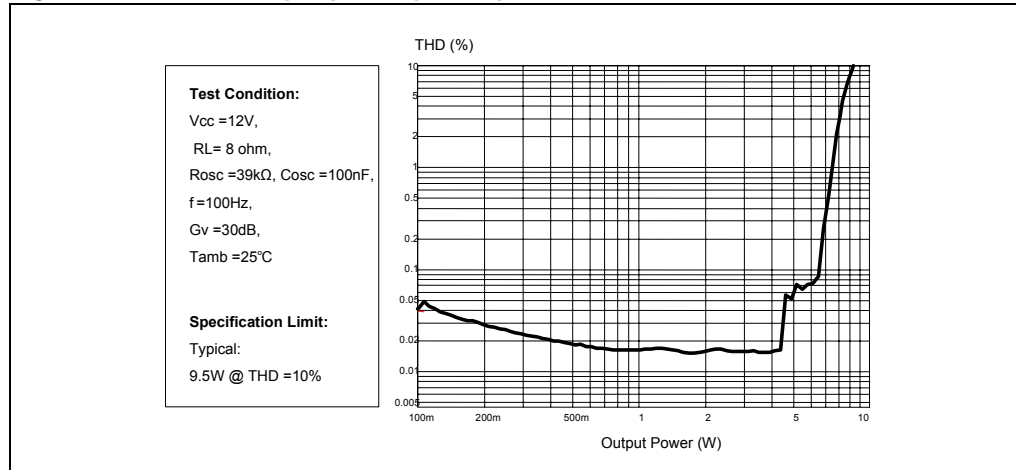
Output Power (W)

Figure 35.   THD vs frequency

THD (%)

Test Condition:

Vcc =12V,

RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =1kHz,

Gv =30dB,

Po =1W

Tamb =25℃

 Specification Limit:

Typical: THD<0.5%
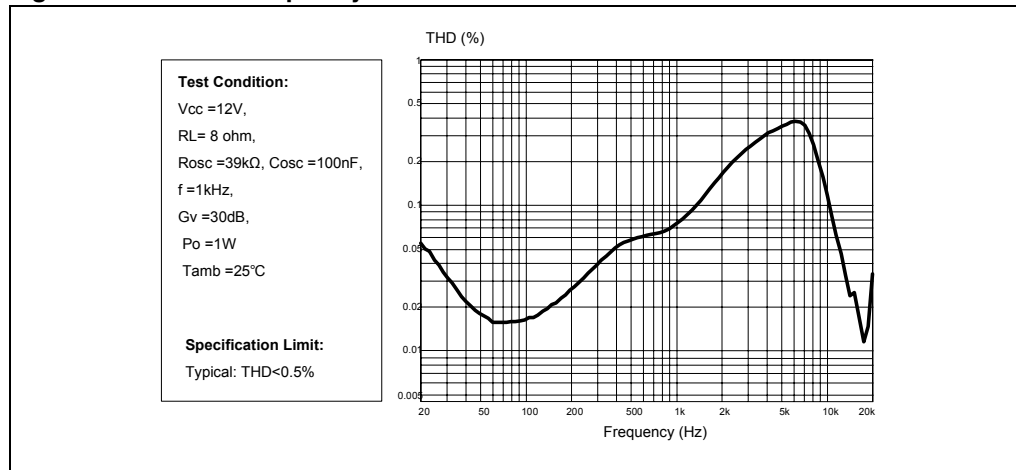
Frequency (Hz)

Figure 36. Frequency response

Test Condition:
Vcc =12V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Po =1W
Tamb =25℃

Specification Limit:
Max: +/-3dB
@20Hz to 20kHz
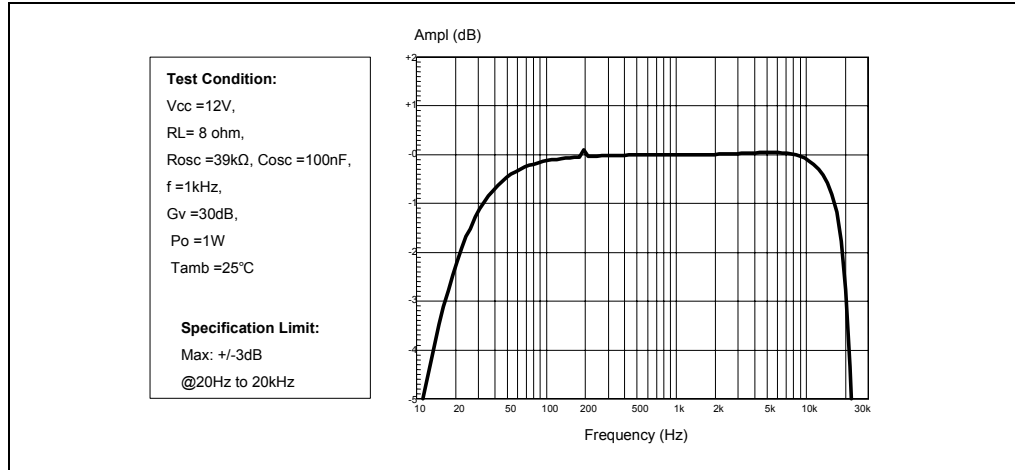
Figure 37. Crosstalk vs frequency

Test Condition:
Vcc =12V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv=30dB,
Po=1W
Tamb=25℃

Specification Limit:
Typical: >50dB (@ f =1kHz)

Figure 38. FFT (0 dB)

Test Condition:
Vcc =12V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv =30dB,
Po =1W
Tamb =25℃

Specification Limit:
Typical: >60dB
for the harmonic   frequency

Figure 39.   FFT (-60 dB)

Test Condition:

Vcc =12V,

RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =1kHz,

Gv =30dB,

 Po = -60dB (@ 1W =0dB)

Tamb =25℃

Specification Limit:

Typical: > 90dB

for the harmonic   frequency
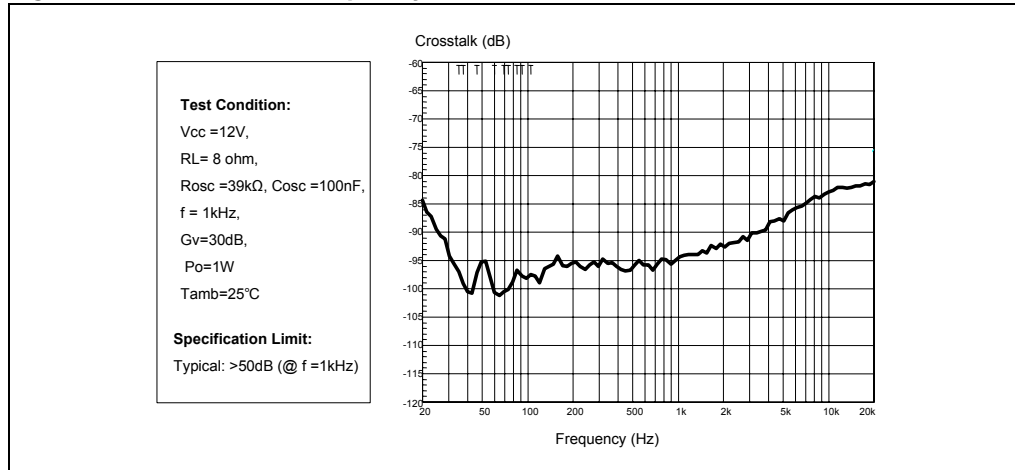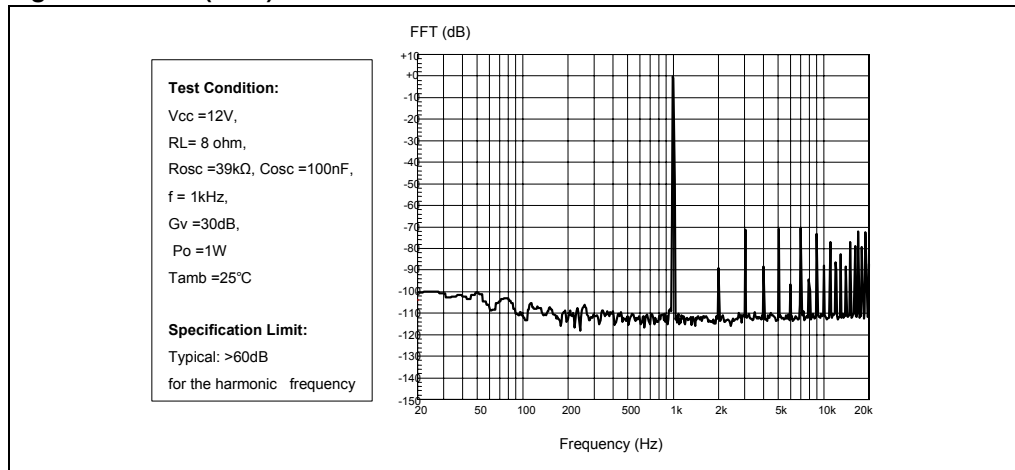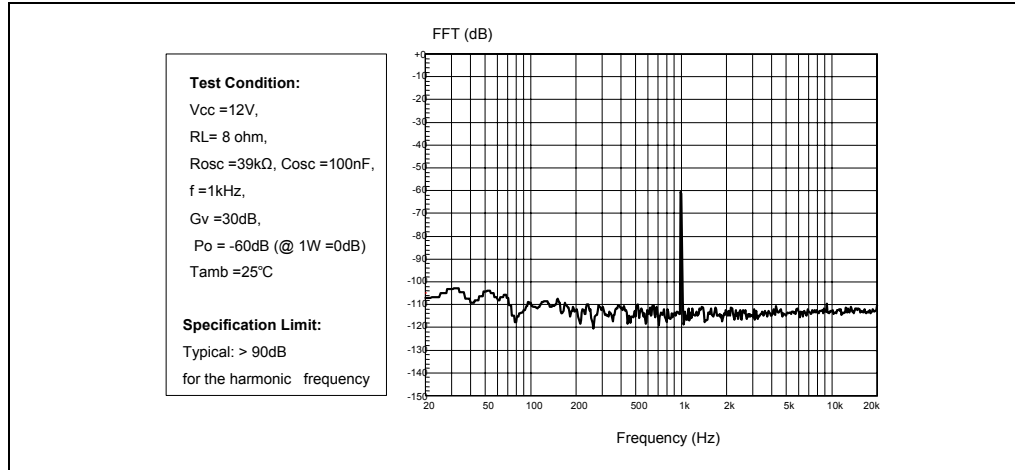
Figure 40.   Power supply rejection ratio vs frequency

Test Condition:

Vcc =12V,

RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =1kHz,

Gv =30dB,

0dB refers to 500mV, 100Hz,

Tamb =25℃
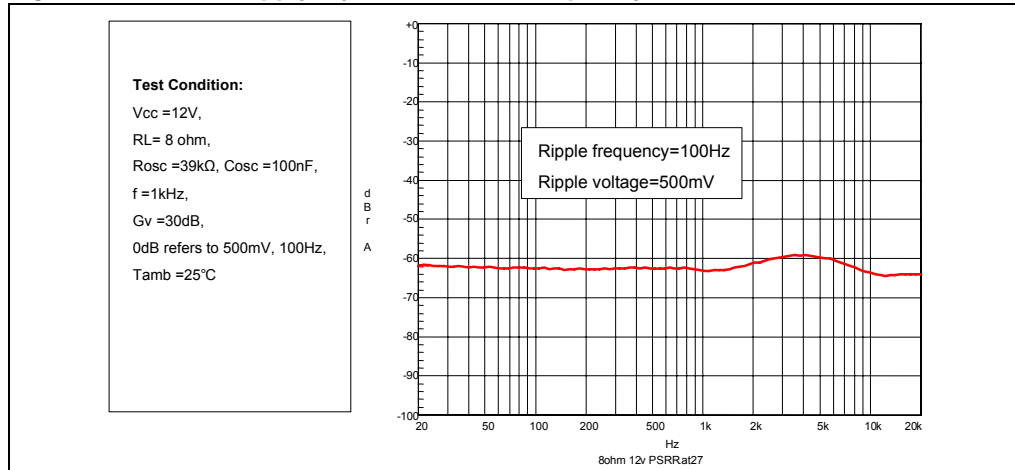
Figure 41.   Power dissipation and efficiency vs output power

Test Condition:

Vcc =12V,

RL= 8 ohm,

Rosc =39kΩ, Cosc =100nF,

f =1kHz,

Gv =30dB,

Tamb =25℃
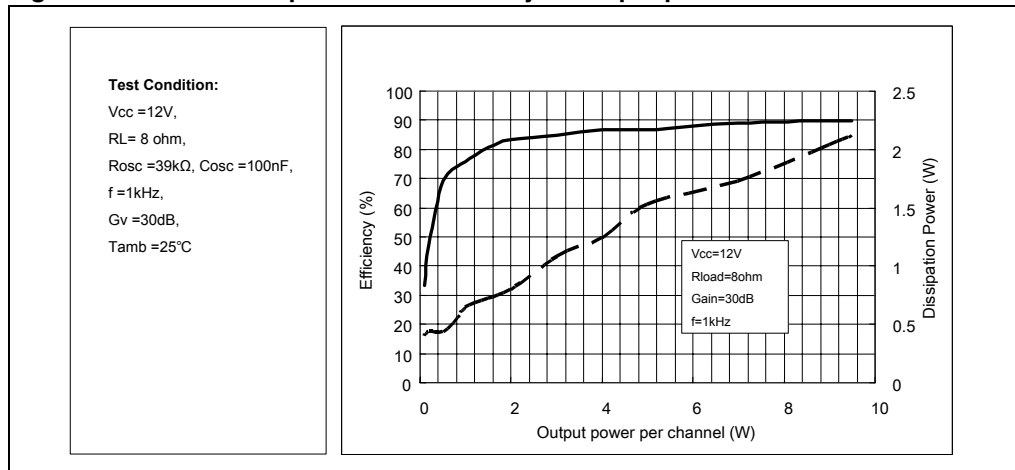
Figure 42.   Closed-loop gain vs frequency

Figure 43.   Current consumption vs voltage on pin MUTE
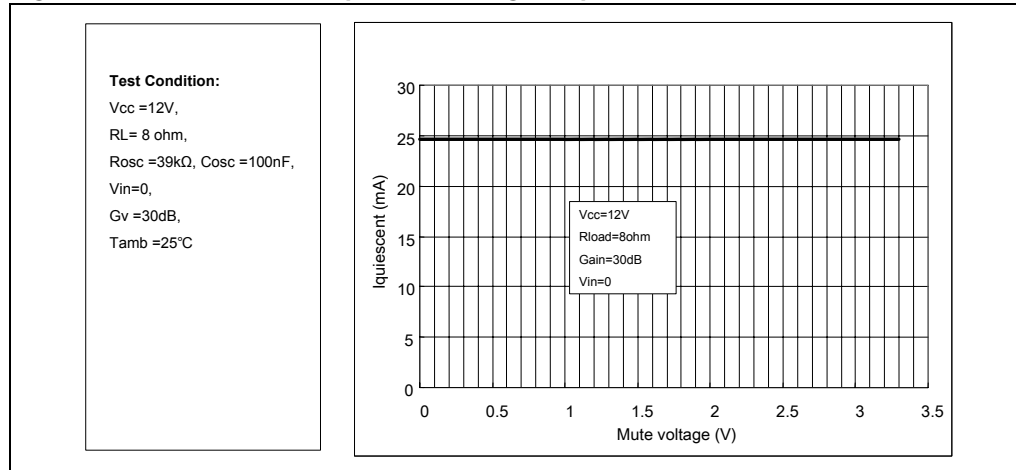
Figure 44.   Attenuation vs voltage on pin MUTE

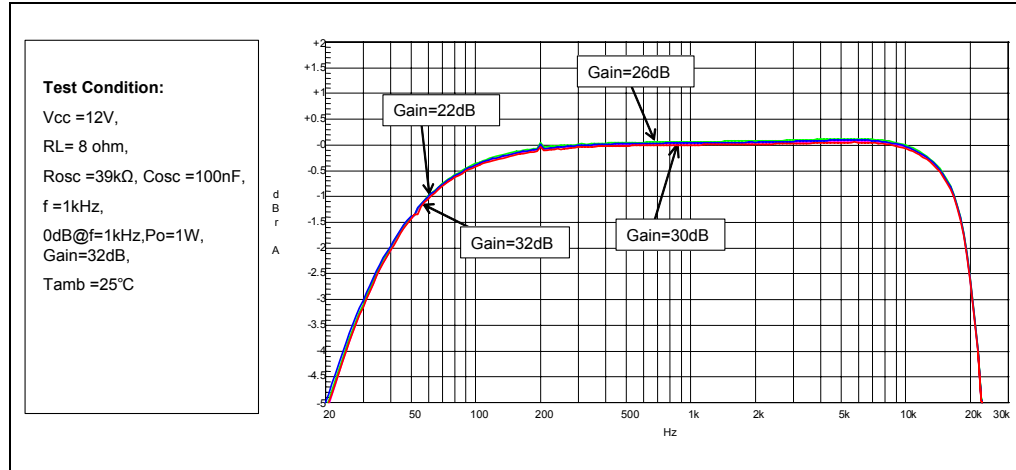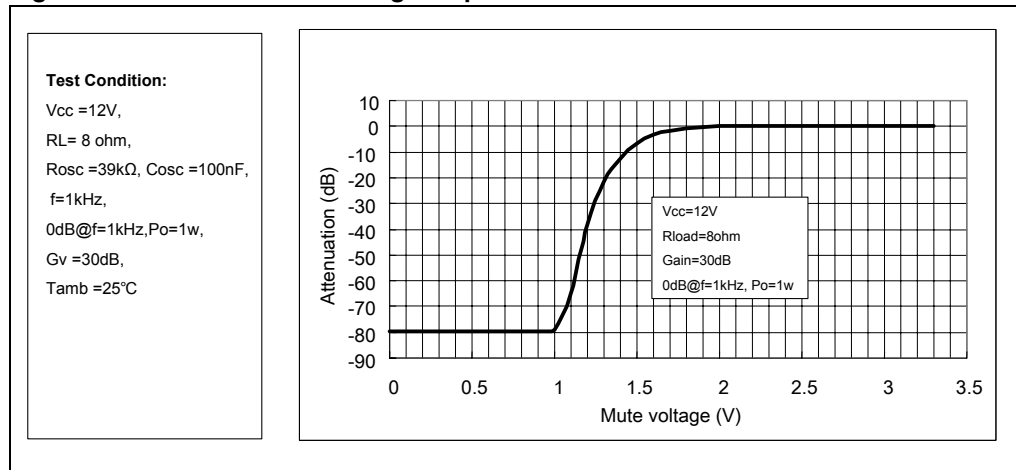**Figure 45.**   **Current consumption vs voltage on pin STBY**

Test Condition:
Vcc =12V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
Vin=0,
Gv =30dB,
Tamb =25℃
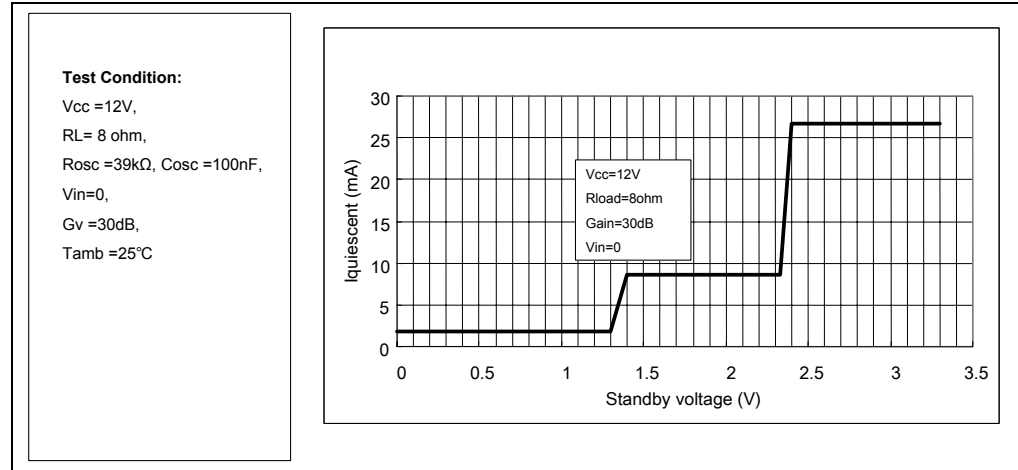
Figure 46.   **Attenuation vs voltage on pin STBY**

Test Condition:
Vcc =12V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
 f=1kHz,
0dB@f=1kHz,Po=1w,
Gv =30dB,
Tamb =25℃
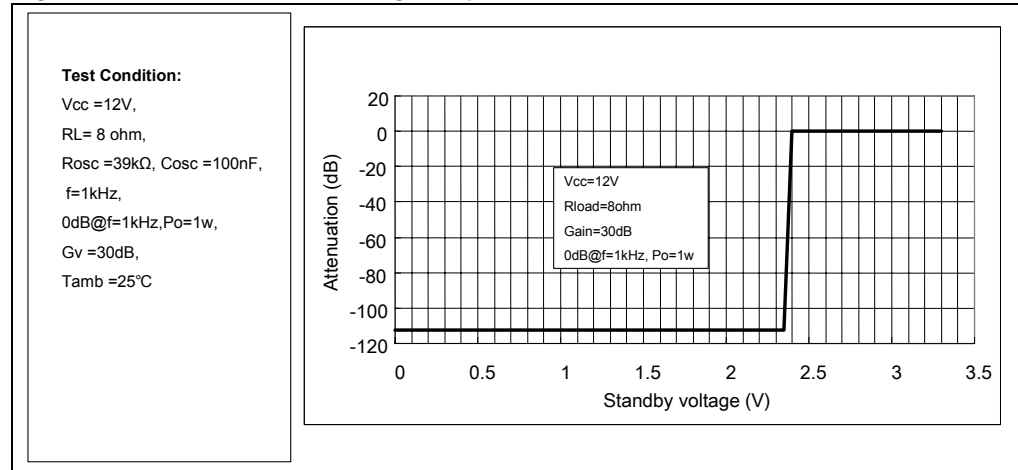
4.4 Test board

Figure 47.   Test board (TDA7491P) layout
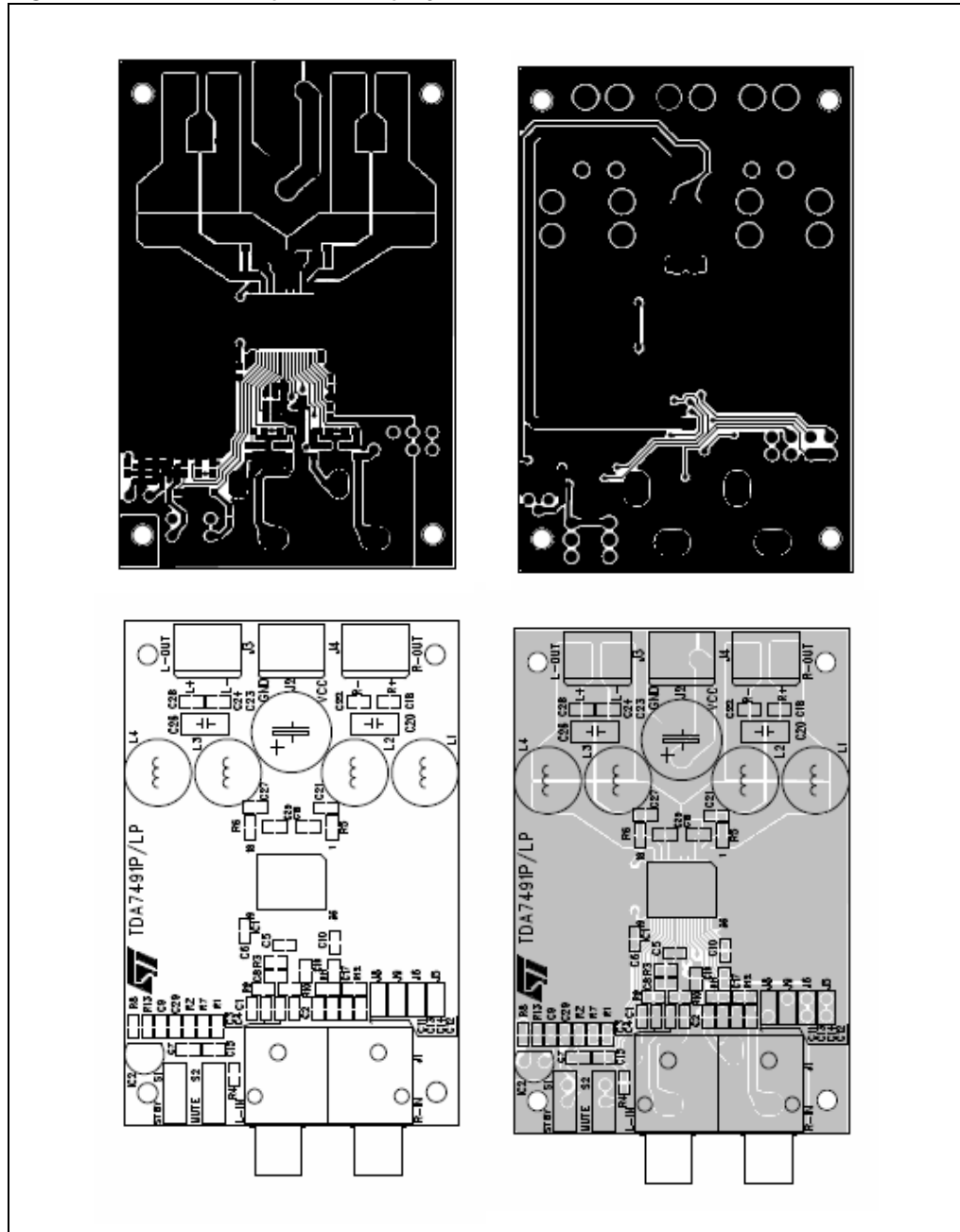
5   Package mechanical data

The TDA7491P comes in a 36-pin PowerSSO package with exposed pad down (EPD).

Figure 48 below shows the package outline and *Table 6* gives the dimensions.

Figure 48.   PowerSSO-36 EPD outline drawing

Table 6. **PowerSSO-36 EPD dimensions**

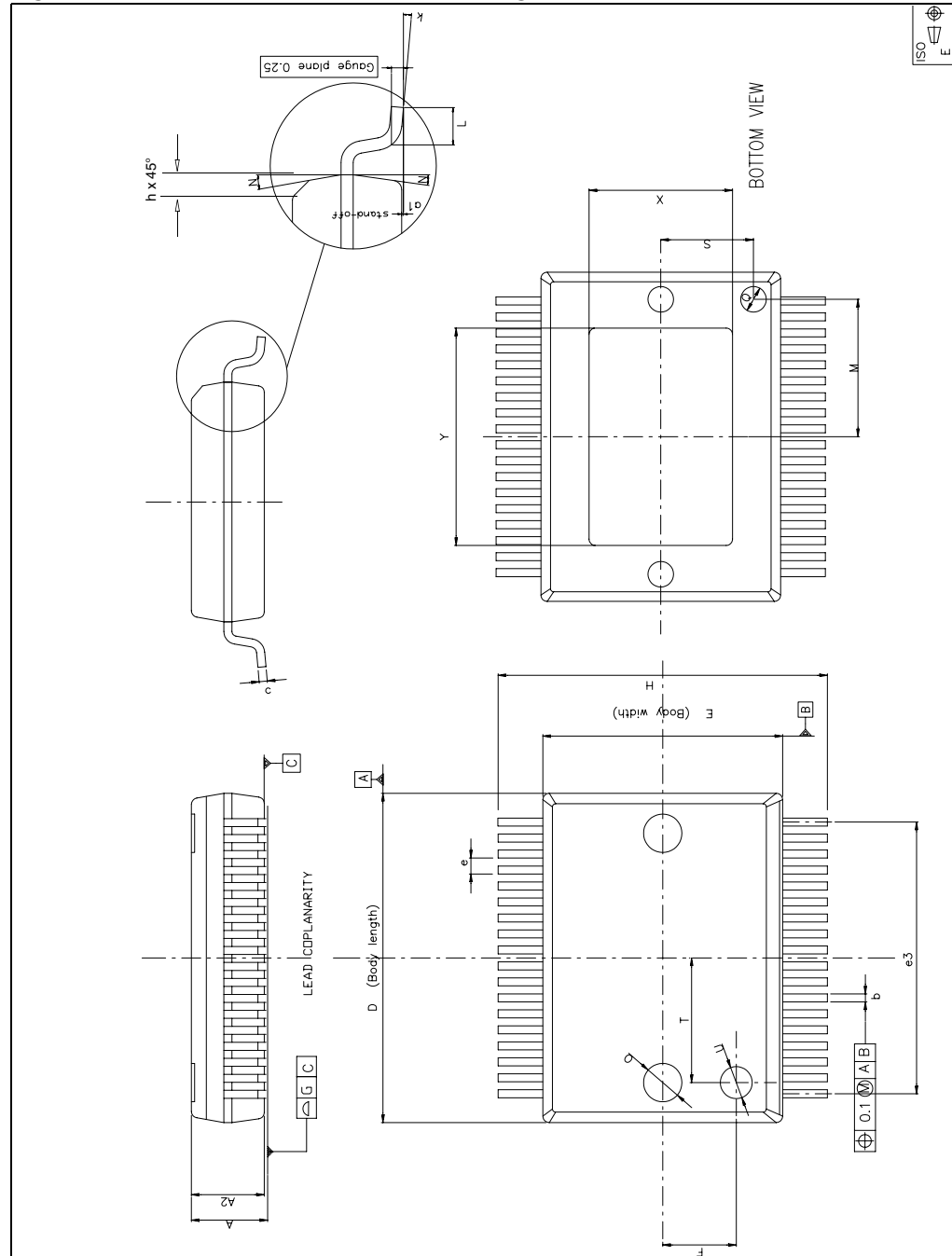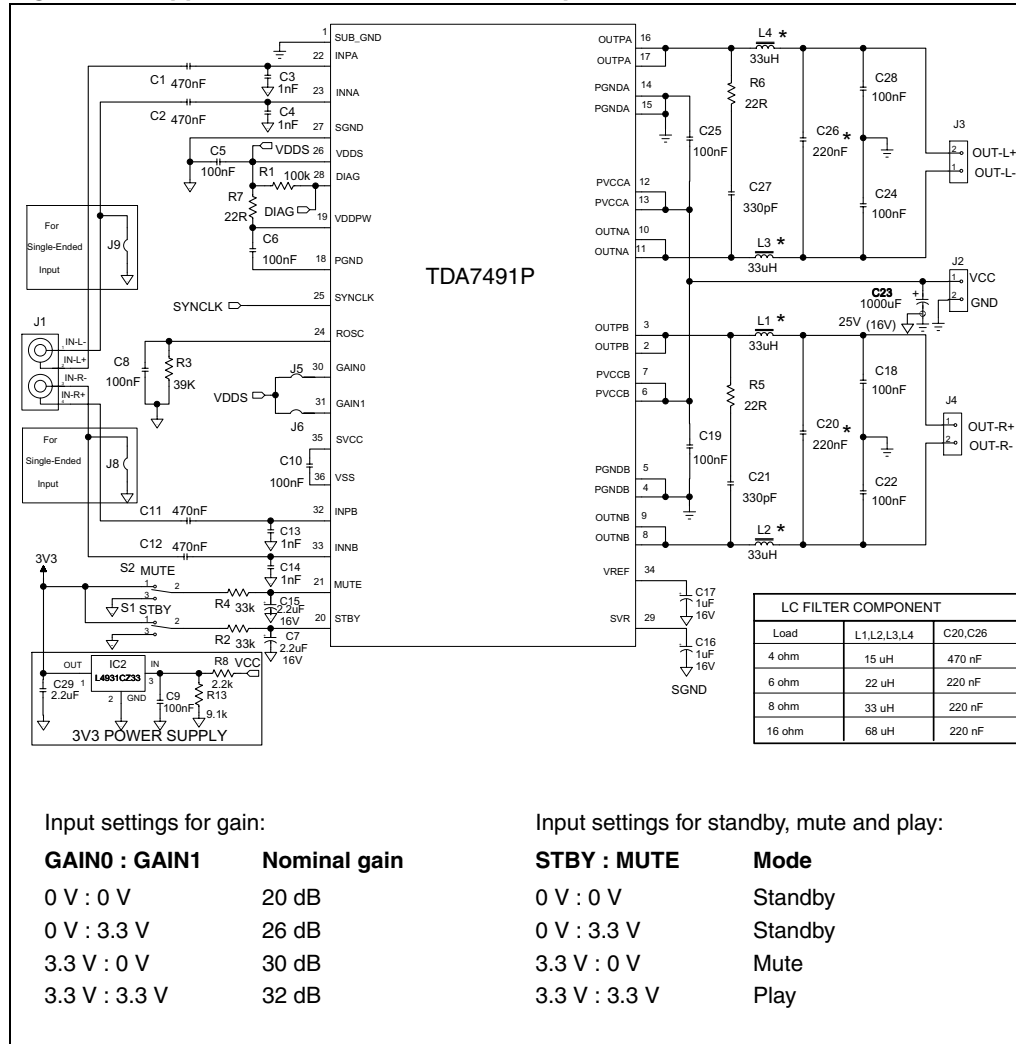| Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.000	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6   Applications circuit

Figure 49.   Applications circuit for class-D amplifier

TDA7491P

LC FILTER COMPONENT		
Load	L1,L2,L3,L4	C20,C26
4 ohm	15 uH	470 nF
6 ohm	22 uH	220 nF
8 ohm	33 uH	220 nF
16 ohm	68 uH	220 nF

Input settings for gain:

GAIN0 : GAIN1	Nominal gain
0 V : 0 V	20 dB
0 V : 3.3 V	26 dB
3.3 V : 0 V	30 dB
3.3 V : 3.3 V	32 dB

Input settings for standby, mute and play:

STBY : MUTE	Mode
0 V : 0 V	Standby
0 V : 3.3 V	Standby
3.3 V : 0 V	Mute
3.3 V : 3.3 V	Play

7 Applications information

7.1 Mode selection

The three operating modes of the TDA7491P are set by the two inputs STBY (pin 20) and MUTE (pin 21).

● Standby mode: all circuits are turned off, very low current consumption.

● Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.

● Play mode: the amplifiers are active.

The protection functions of the TDA7491P are realized by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 50*. The input current of the corresponding pins must be limited to 200 µA.

Table 7. Mode settings

Mode	STBY	MUTE
Standby	L [1]	X (don't care)
Mute	H [1]	L
Play	H	H

1. Drive levels defined in *Table 5: Electrical specifications on page 10*

Figure 50. Standby and mute circuits
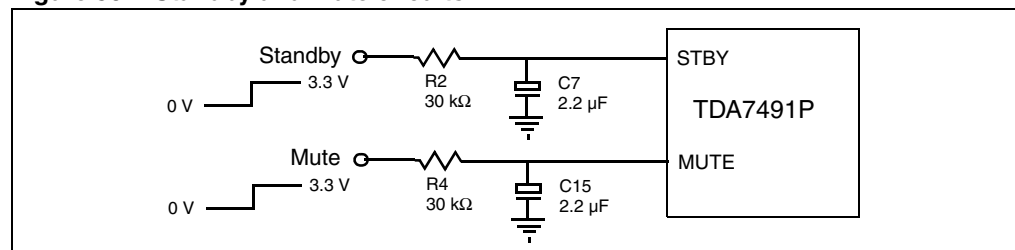
Figure 51. Turn-on/off sequence for minimizing speaker "pop"
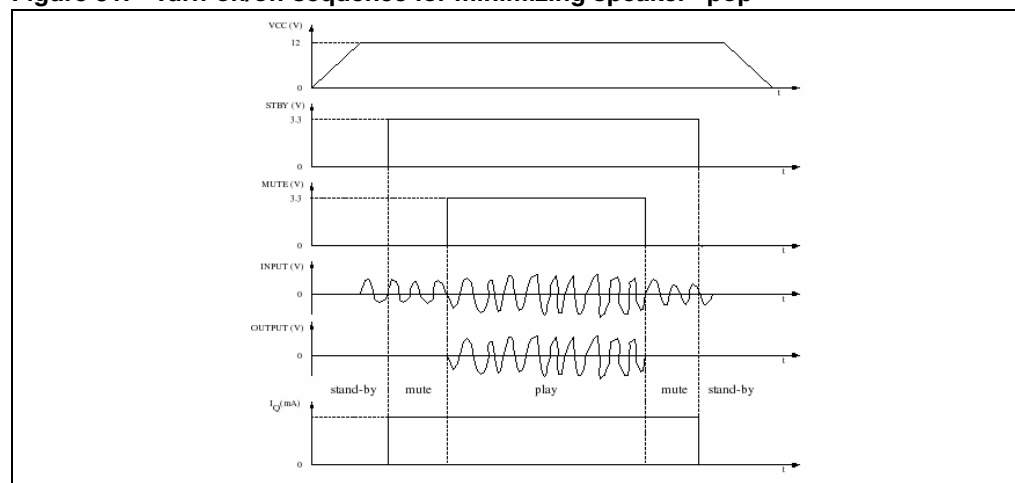
7.2   Gain setting

The gain of the TDA7491P is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 8.   Gain settings

| GAIN0	GAIN1	Nominal gain, G_v (dB)
0	0	20
0	1	26
1	0	30
1	1	32

7.3   Input resistance and capacitance

The input impedance is set by an internal resistor Ri = 60 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in *Figure 52*. For Ci = 220 nF the high-pass filter cut-off frequency is below 20 Hz:

fc = 1 / (2 * π * Ri * Ci)

Figure 52.   Device input circuit and frequency response
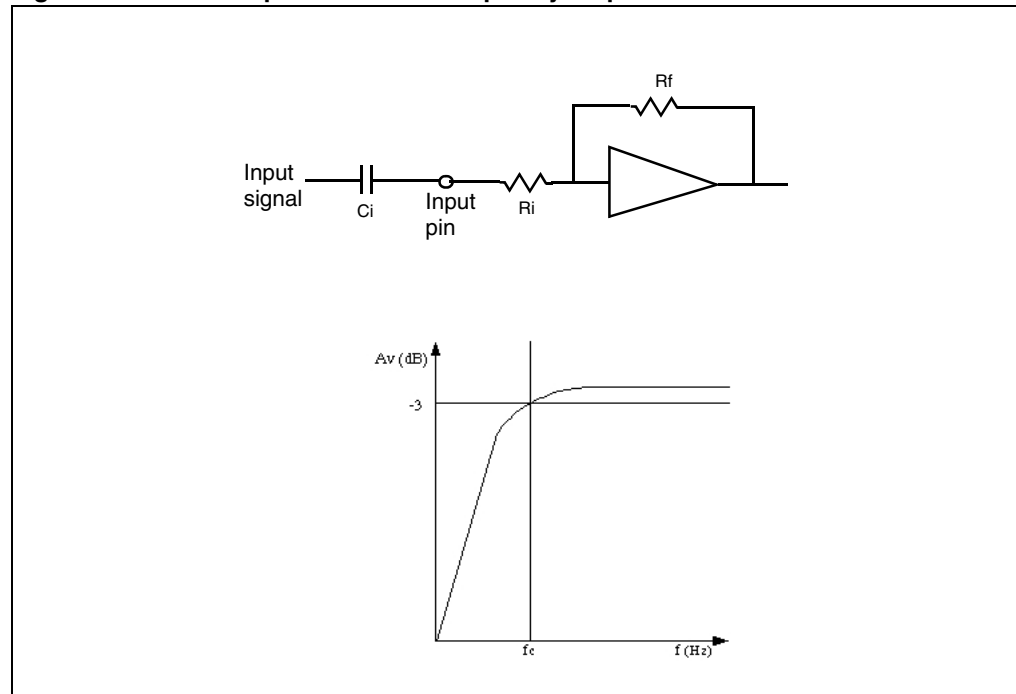
7.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7491P as master clock, while the other devices are in slave mode (that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

7.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, R_{OSC}, connected to pin ROSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where R_{OSC} is in kΩ.

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 kΩ as given below in *Table 9*.

7.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in *Table 9*.
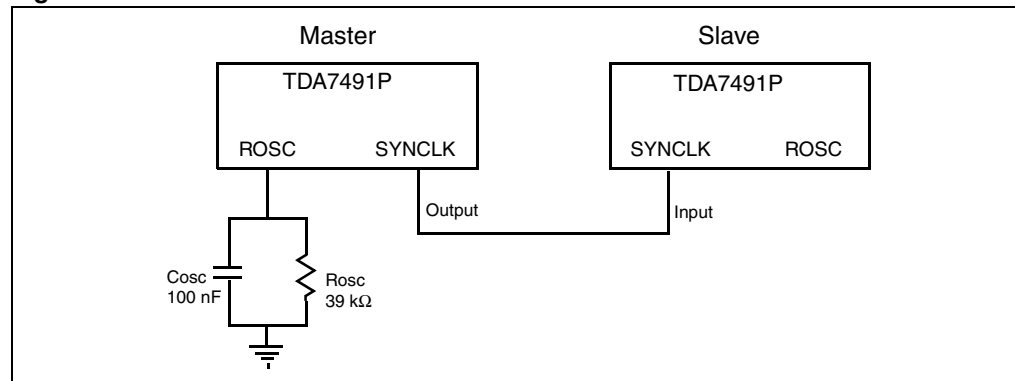
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 9. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating (not connected)	Input

**Figure 53. Master and slave connection**

7.5 Filterless modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM). The differential output voltages change between 0 V and +V_{CC} and between 0 V and -V_{CC}. This is in contrast to the traditional bipolar PWM outputs which change between +V_{CC} and -V_{CC}.

An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform. The OUTP and OUTN are in the same phase when the input is zero, then the switching current is low and the loss in the load is small. In practice, a short delay is introduced between these two outputs in order to avoid the BTL output switching at the same time.

TDA7491P can be used without a filter before the speaker, because the frequency of the TDA7491P output is beyond the audio frequency, the audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

Figure 54.   Unipolar PWM output
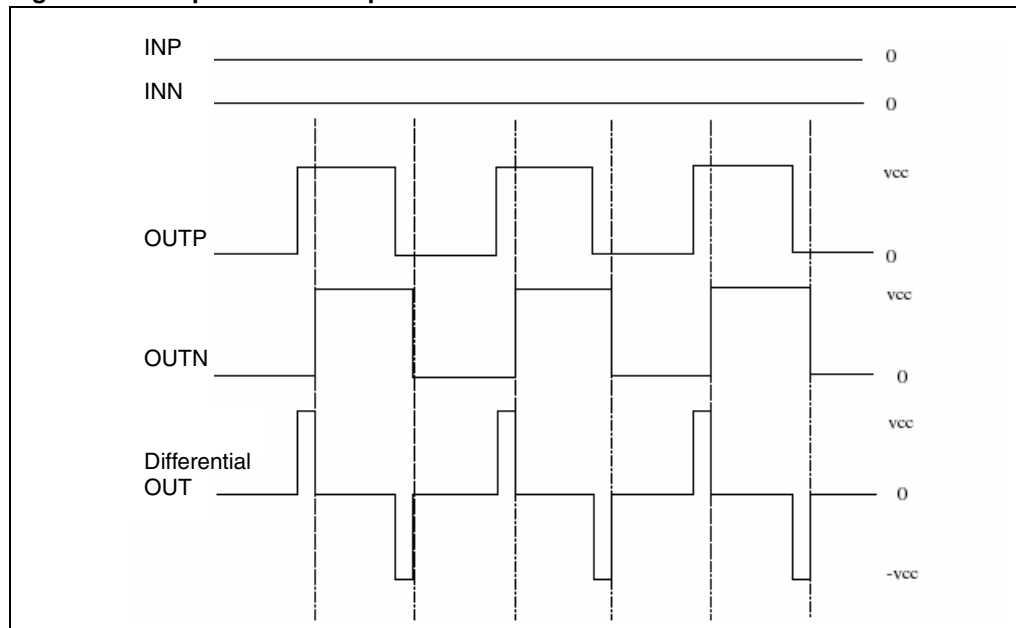
7.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in *Figure 55* and *Figure 56* below.

Figure 55.   Typical LC filter for a 8-Ω speaker
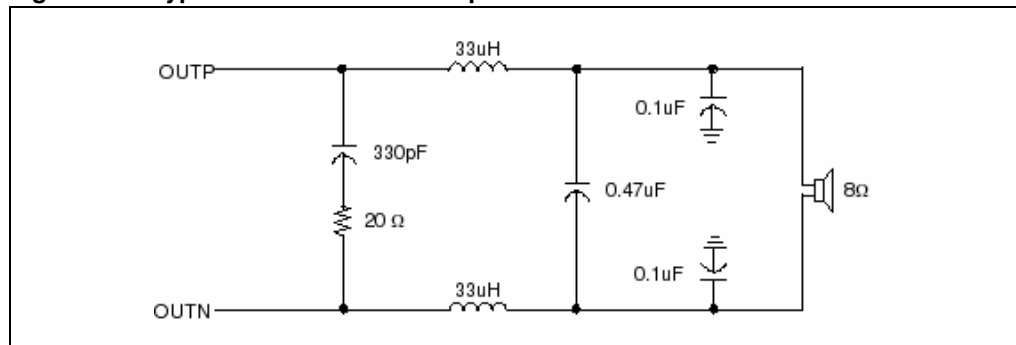
Figure 56.   Typical LC filter for a 4-Ω speaker

Doc ID 13540 Rev 4
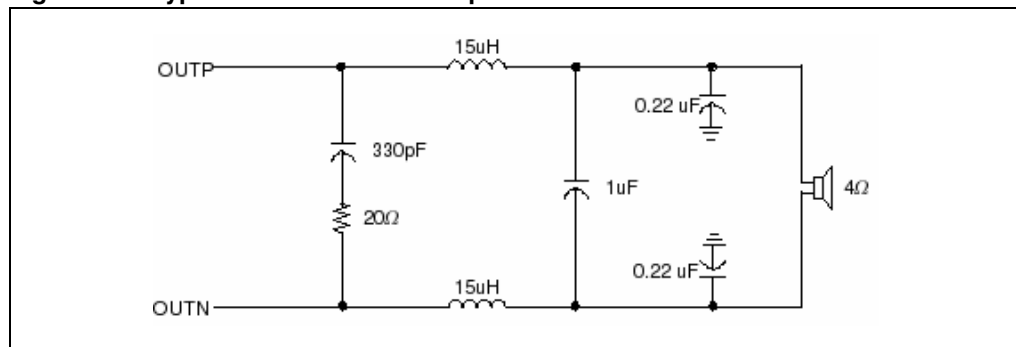
7.7 Protection function

The TDA7491P is fully protected against overvoltages, undervoltages, overcurrents and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for V_{OVP} given in *Table 5: Electrical specifications on page 10* the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for V_{UVP} given in *Table 5: Electrical specifications on page 10* the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for I_{OCP} given in *Table 5: Electrical specifications on page 10* the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC}, is determined by the R-C components connected to pin STBY.

Thermal protection (OTP)

If the junction temperature, T_j, reaches 145 °C (nominal), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for Tj given in *Table 5: Electrical specifications on page 10* the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

7.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<18 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 µA) of the pin.

Figure 57. Behavior of pin DIAG for various protection conditions
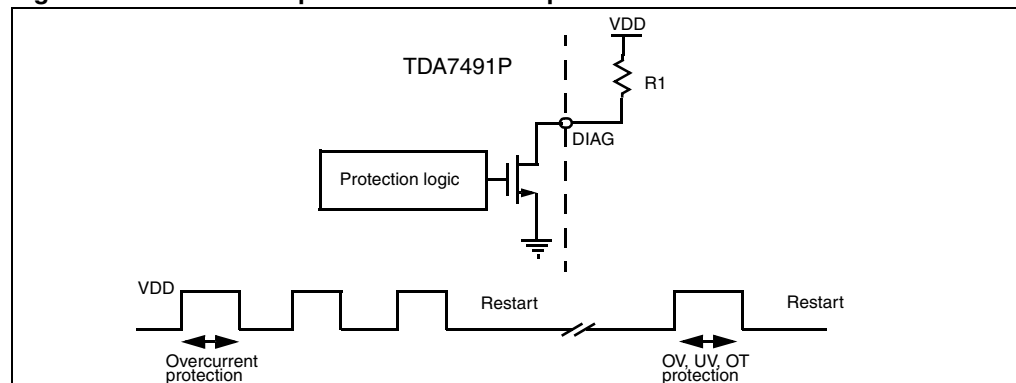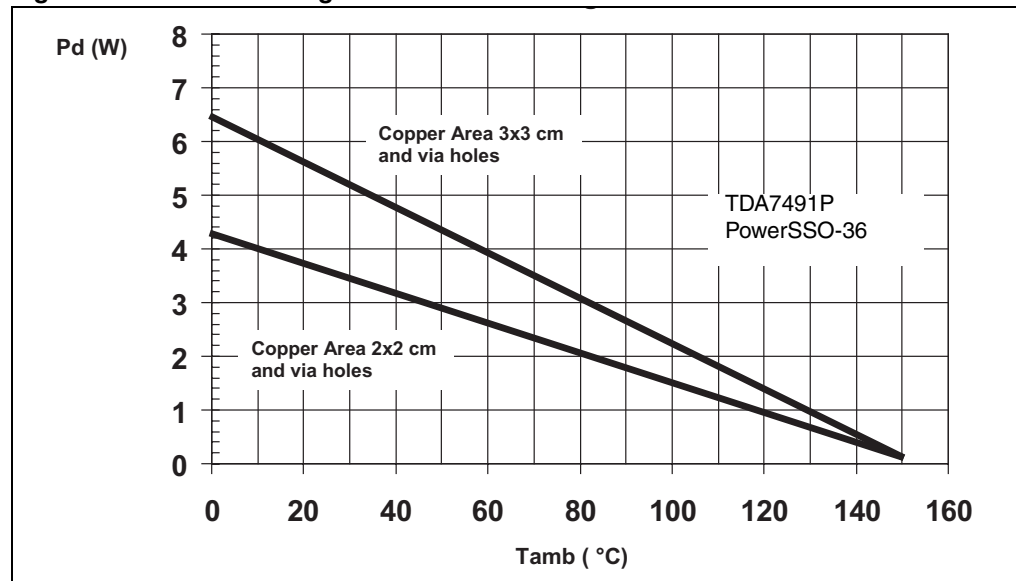
7.9 Heatsink requirements

A thermal resistance of 24 °C/W can be obtained using the PCB copper ground layer with 16 vias connecting it to the contact area for the exposed pad. Ensure that the copper ground area is a nominal 9 cm^2 for 24 °C/W.

Figure 58 shows the derating curves for copper areas of 4 cm^2 and 9 cm^2.

As with most amplifiers, the power dissipated within the device depends primarily on the supply voltage, the load impedance and the output modulation level.

The maximum estimated power dissipation for the TDA7491P is less than 2 W. When properly mounted on the above PCB the junction temperature could increase by 48 °C. However, with a musical program the dissipated power is about 40% less than this, leading to a temperature increase of around only 30 °C. So even at the maximum recommended ambient temperature for consumer applications of 50 °C there is still a clear safety margin before the maximum junction temperature (150 °C) is reached.

Figure 58. Power derating curves for PCB used as heatsink

8   Revision history

Table 10.   **Document revision history**

Date	Revision	Changes
02-Jul-2007	1	Initial release.
15-Oct-2008	2	Updated characterization curves.
23-Jun-2009	3	Updated text concerning oscillator R and C in *Section 3.3: Electrical specifications on page 10* Updated condition for Iq test, added V_{UVP} maximum value, updated THD maximum value, updated STBY and MUTE voltages in *Table 5: Electrical specifications on page 10* Updated equation for f_{SW} *on page 11* and *on page 34* Updated *Figure 49: Applications circuit for class-D amplifier on page 31* Updated *Section 7.7: Protection function on page 37*.
04-Sep-2009	4	Added text for exposed pad in *Figure 2 on page 8* Added text for exposed pad in *Table 2 on page 9* Updated exposed pad Y (Min) dimension in *Table 6 on page 30* Updated supply voltage for pin DIAG pull-up resistor in *Section 7.8 on page 37*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Doc ID 13540 Rev 4