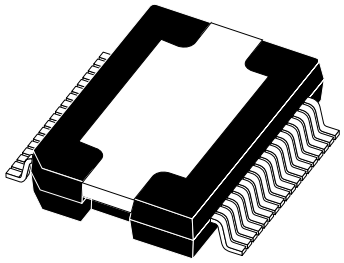
STA516B

60-V 6-A quad power half-bridge digital amplifier

Features

- Low input/output pulse width distortion
- 200 mΩ R_{dsON} complementary DMOS output stage
- CMOS-compatible logic inputs
- Thermal protection
- Thermal-warning output
- Undervoltage protection



PowerSO36 package
with exposed pad up

Description

STA516B is a monolithic quad half-bridge power amplifier in Multipower BCD Technology. The device can be used as a dual-bridge stage or reconfigured, by connecting pin CONFIG to pins VDD, as a single-bridge stage with double-current capability or as a half-bridge stage (binary mode) with half-current capability.

The device is designed, particularly, to be the output stage of a stereo all-digital high-efficiency amplifier. It is capable of delivering 160 W + 160 W into 8-Ω loads with THD = 10% at V_{CC} = 51 V or, in single-BTL configuration, 320 W into a 4-Ω load with THD = 10% at V_{CC} = 52 V.

The input pins have a threshold proportional to the voltage on pin VL.

The STA516B is aimed at audio amplifiers in Hi-Fi applications, such as home theatre systems, active speakers and docking stations.

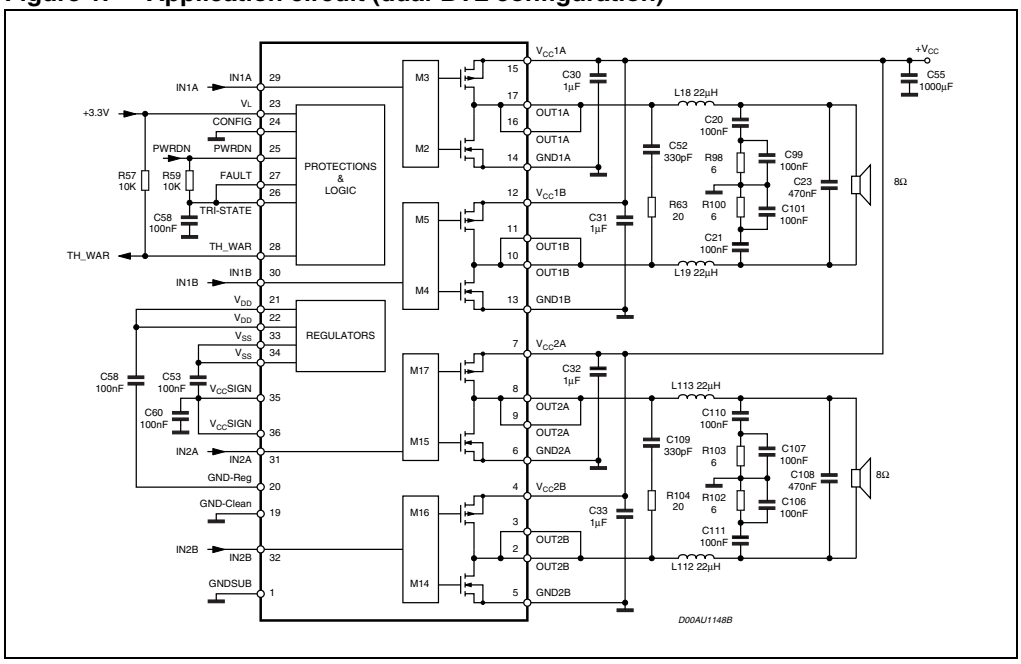
It comes in a 36-pin PowerSO package with exposed pad up (EPU).

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STA516B	0 to 70 °C	PowerSO36 EPU	Tube
STA516B13TR	0 to 70 °C	PowerSO36 EPU	Tape and reel

1 Introduction

Figure 1. Application circuit (dual-BTL configuration)



2 Pin description

Figure 2. Pin out

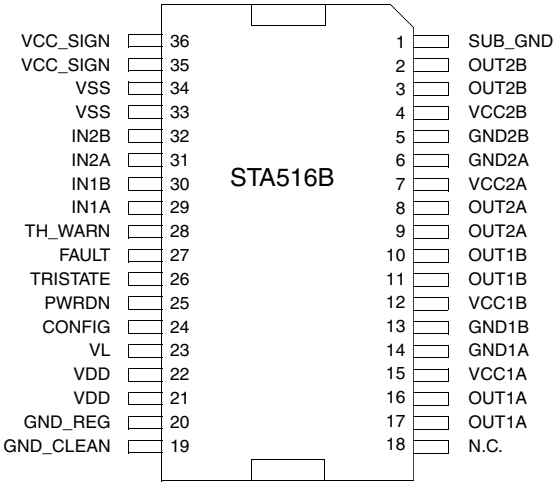


Table 2. Pin function

Pin	Name	Type	Description
1	GND_SUB	PWR	Substrate ground
2, 3	OUT2B	O	Half-bridge stage output 2B
4	VCC2B	PWR	Positive supply
5	GND2B	PWR	Negative supply
6	GND2A	PWR	Negative supply
7	VCC2A	PWR	Positive supply
8, 9	OUT2A	O	Half-bridge stage output 2A
10, 11	OUT1B	O	Half-bridge stage output 1B
12	VCC1B	PWR	Positive supply
13	GND1B	PWR	Negative supply
14	GND1A	PWR	Negative supply
15	VCC1A	PWR	Positive supply
16, 17	OUT1A	O	Half-bridge stage output 1A
18	N.C.	-	No internal connection
19	GND_CLEAN	PWR	Logical ground
20	GND_REG	PWR	Ground for regulator V_{DD}
21, 22	VDD	PWR	5-V regulator referred to ground
23	VL	PWR	High logical state setting voltage, V_L

Table 2. Pin function (continued)

Pin	Name	Type	Description
24	CONFIG	I	Configuration pin: 0: normal operation 1: bridges in parallel (OUT1A = OUT1B, OUT2A = OUT2B (If IN1A = IN1B, IN2A = IN2B))
25	PWRDN	I	Standby pin: 0: low-power mode 1: normal operation
26	TRISTATE	I	3-state pin: 0: all power amplifier outputs in high-impedance state 1: normal operation
27	FAULT	O	Fault advisor (open-drain device, needs pullup resistor): 0: fault detected (short circuit or thermal, for example) 1: normal operation
28	TH_WARN	O	Thermal-warning advisor (open-drain device, needs pullup resistor): 0: temperature of the IC >130 ^{o}C 1: normal operation
29	IN1A	I	Half-bridge stage input 1A
30	IN1B	I	Half-bridge stage input 1B
31	IN2A	I	Half-bridge stage input 2A
32	IN2B	I	Half-bridge stage input 2B
33, 34	VSS	PWR	5-V regulator referred to +V_{CC}
35, 36	VCC_SIGN	PWR	Signal positive supply

3 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (pins 4, 7, 12, 15)	60	V
V_{max}	Voltage on pins 23 to 32	5.5	V
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}, T_j	Storage and junction temperatures	-40 to 150	°C

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	1	2.5	°C/W
T_{jSD}	Thermal-shutdown junction temperature	-	150	-	°C
T_{warn}	Thermal-warning temperature	-	130	-	°C
t_{hSD}	Thermal-shutdown hysteresis	-	25	-	°C

Unless otherwise stated, the test conditions for *Table 5* below are V_L = 3.3 V, V_{CC} = 50 V and T_{amb} = 25 °C

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{dsON}	Power P-channel/N-channel MOSFET R_{dsON}	I_{dd} = 1 A	-	200	240	mΩ
I_{dss}	Power P-channel/N-channel leakage Idss	-	-	-	100	µA
g_N	Power P-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
g_P	Power N-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	see *Figure 3*	-	10	20	ns
Dt_d	High current dead time (dynamic)	L = 22 µH, C = 470 nF R_L = 8 Ω, I_{dd} = 4.5 A see *Figure 4*	-	-	50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	-	100	ns
t_r	Rise time	Resistive load see *Figure 3*	-	-	25	ns
t_f	Fall time	Resistive load see *Figure 3*	-	-	25	ns
V_{CC}	Supply operating voltage	-	10	-	56	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IN-High}$	High-level input voltage	-	-	-	V_L / 2 + 300 mV	V
V_{IN-Low}	Low-level input voltage	-	V_L / 2 - 300 mV	-	-	V
I_{IN-H}	High-level input current	$V_{IN} = V_L$	-	1	-	µA
I_{IN-L}	Low-level input current	V_{IN} = 0.3 V	-	1	-	µA
$I_{PWRDN-H}$	High-level PWRDN pin input current	V_L = 3.3 V	-	35	-	µA
V_{Low}	Logical low-state voltage (pins PWRDN, TRISTATE) (see *Table 6*)	V_L = 3.3 V	0.8	-		V
V_{High}	Logical high-state voltage (pins PWRDN, TRISTATE) (see *Table 6*)	V_L = 3.3 V		-	1.7	V
$I_{VCC-PWRDN}$	Supply current from V_{CC} in power down	V_{PWRDN} = 0 V	-	-	3	mA
I_{FAULT}	Output current on pins FAULT, TH_WARN with fault condition	V_{pin} = 3.3 V	-	1	-	mA
$I_{VCC-HiZ}$	Supply current from V_{CC} in 3-state	$V_{TRISTATE}$ = 0 V	-	22	-	mA
I_{VCC}	Supply current from V_{CC} in operation both channels switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	70	-	mA
I_{OCP}	Overcurrent protection threshold (short-circuit current limit) (1)	-	6	8	10	A
V_{UVP}	Undervoltage protection threshold	-	-	7	-	V
V_{OVP}	Overvoltage protection threshold	-	60	-	70	V
t_{pw_min}	Minimum output pulse width	No load	25	-	40	ns

1. See specific application note number: AN1994

Table 6. Threshold switching voltage variation with voltage on pin VL

Voltage on pin VL, V_L	V_{LOW} max	V_{HIGH} min	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5.0	0.85	1.85	V

Table 7. Logic truth table

Pin TRISTATE	Inputs as per *Figure 4*		Transistors as per *Figure 4*				Output mode
	INxA	INxB	Q1	Q2	Q3	Q4	
0	x	x	Off	Off	Off	Off	Hi Z
1	0	0	Off	Off	On	On	Dump
1	0	1	Off	On	On	Off	Negative
1	1	0	On	Off	Off	On	Positive
1	1	1	On	On	Off	Off	Not used

3.1 Test circuits

Figure 3. Test circuit

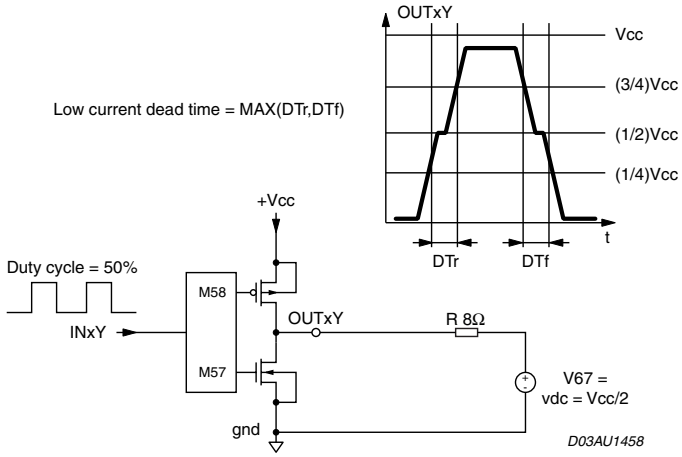
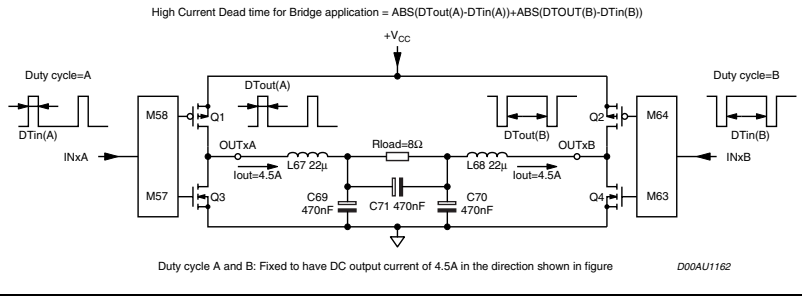


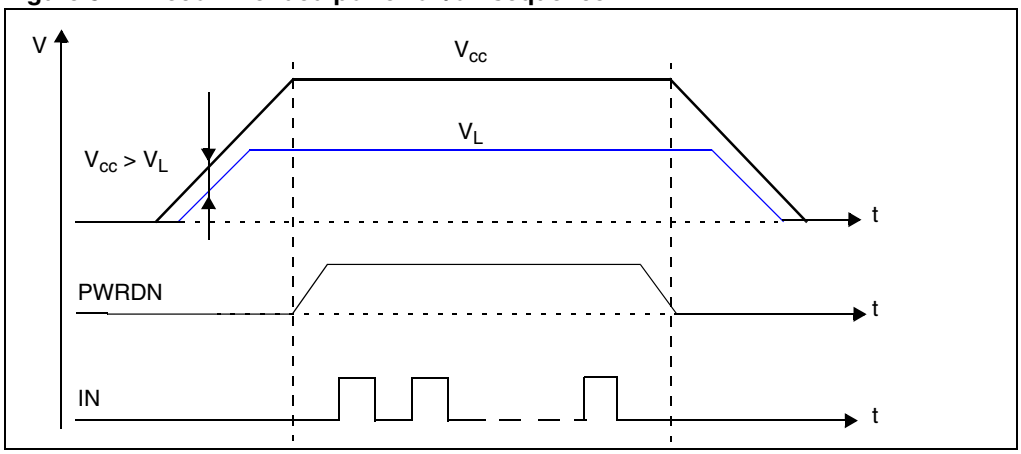
Figure 4. Current dead-time test circuit



4 Power supply and control sequencing

To guarantee correct operation and reliability, the recommended power-on/off sequence as shown in *Figure 5* must be followed.

Figure 5. Recommended power-on/off sequence



V_{CC} must turn on before V_L. This prevents uncontrolled current flowing through the internal protection diode connected between V_L (logic supply) and V_{CC} (high power supply) which could result in damage to the device.

PWRDN must be released after V_L is switched on. An input signal can then be applied to the power stage.

5 Applications

Figure 6 below shows a single-BLT configuration capable of giving 320 W into a 4-Ω load at 10% THD with V_{CC} = 52 V. This result was obtained using the STA30X+STA50X demonstration board. Note that a PWM modulator as driver is required.

Figure 6. Typical single-BTL configuration for 320 W

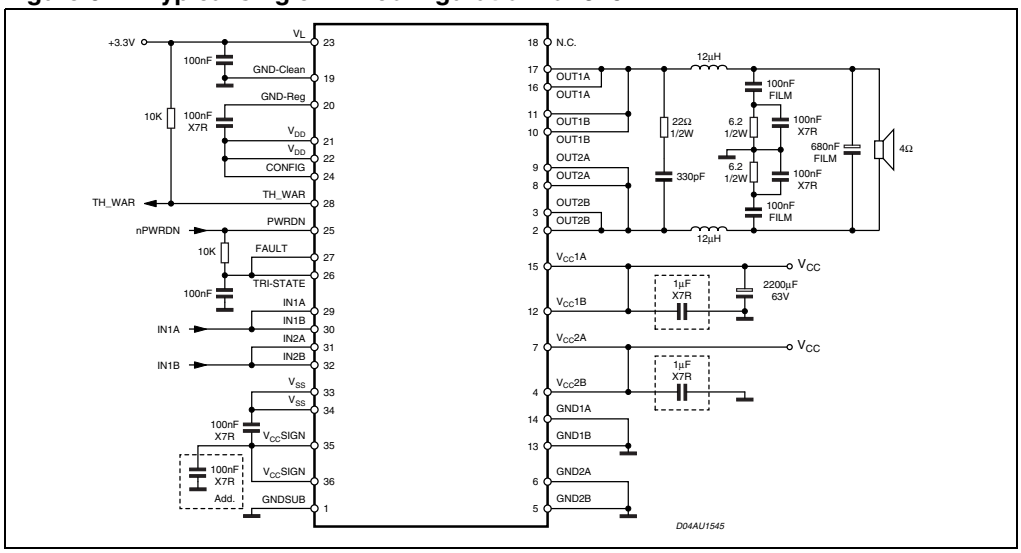
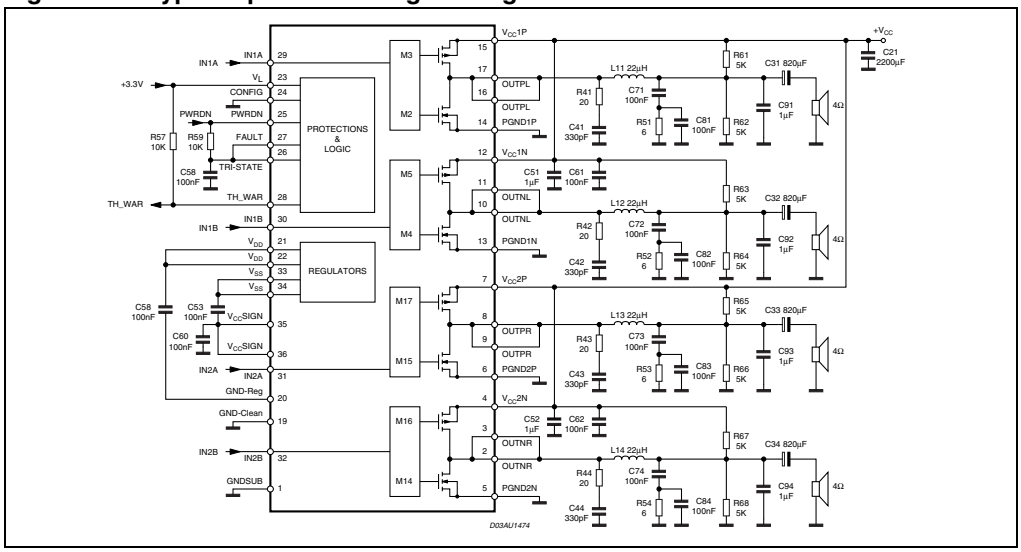


Figure 7. Typical quad half-bridge configuration



For more information, refer to the application note AN1994.

6 Package mechanical data

Figure 8. PowerSO36-EPU outline drawing

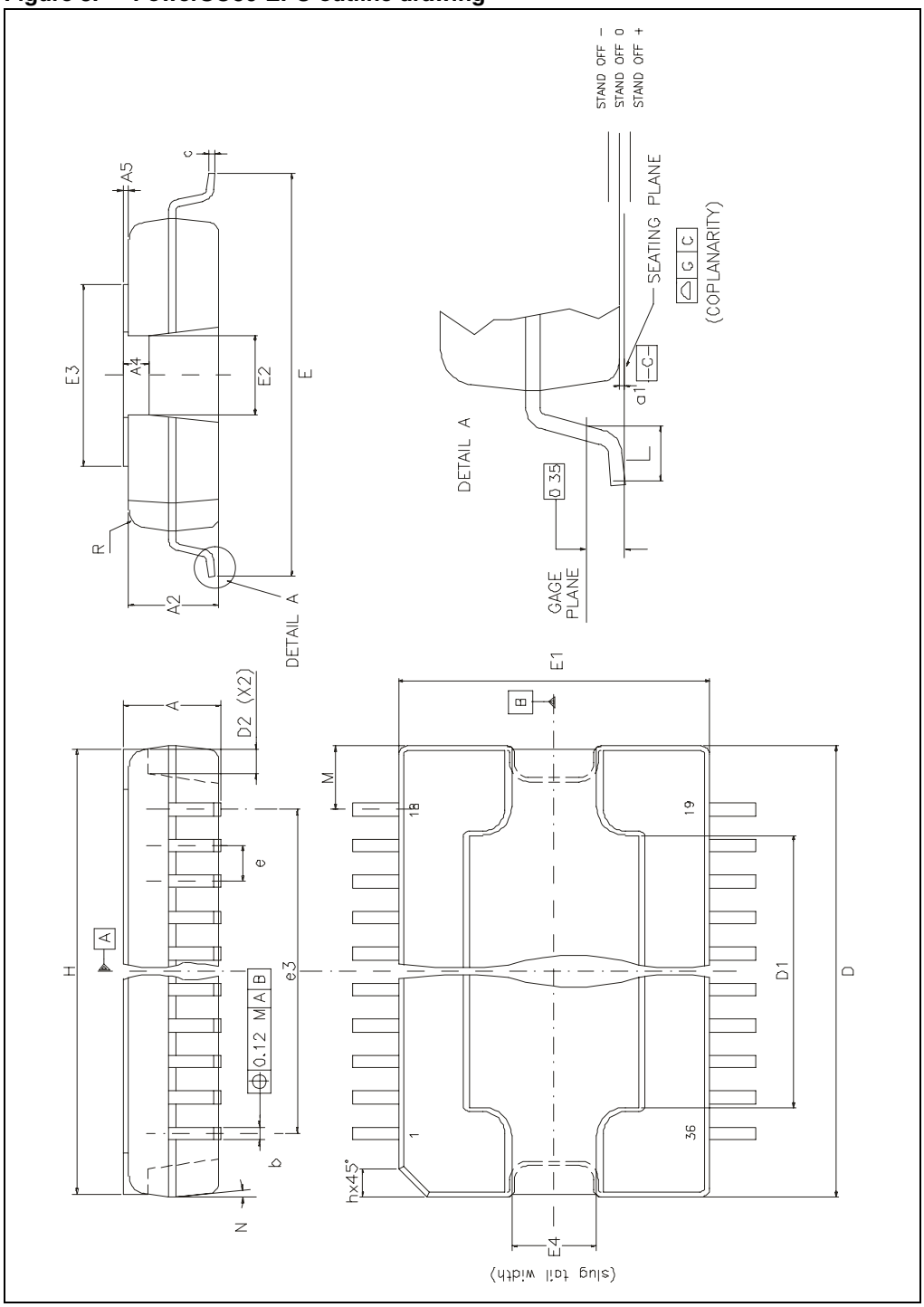


Table 8. PowerSO36-EPU dimensions

Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.25	-	3.43	0.128	-	0.135
A2	3.10	-	3.20	0.122	-	0.126
A4	0.80	-	1.00	0.031	-	0.039
A5	-	0.20	-	-	0.008	-
a1	0.03	-	-0.04	0.001	-	-0.002
b	0.22	-	0.38	0.009	-	0.015
c	0.23	-	0.32	0.009	-	0.013
D	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.386
D2	-	1.00	-	-	0.039	-
E	13.90	-	14.50	0.547	-	0.571
E1	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90	-	-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
e	-	0.65	-	-	0.026	-
e3	-	11.05	-	-	0.435	-
G	0	-	0.08	0	-	0.003
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10	-	-	0.043
L	0.80	-	1.10	0.031	-	0.043
M	2.25	-	2.60	0.089	-	0.102
N	-	-	10 degrees	-	-	10 degrees
R	-	0.6	-	-	0.024	-
s	-	-	8 degrees	-	-	8 degrees

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Feb-2007	1	Initial release.
19-Mar-2007	2	Update to reflect product maturity.
12-Aug-2009	3	Updated description section on cover page.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com