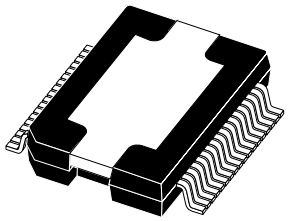
STA510A

44-volt, 5.5-amp, quad power half bridge

Features

- Multipower BCD technology
- Minimum input, output pulse width distortion
- 150-mΩ R_{dsON} complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal-warning output
- Undervoltage protection
- Short-circuit protection



PowerSO36
with exposed pad up (EPU)

Description

STA510A is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting pin CONFIG to V_{DD}, as a single bridge with double current capability, or as half bridges (Binary mode) with half current capability.

The device is intended for the output stage of a stereo all-digital high-efficiency (DDX®) amplifier which employs a pulse-width modulator driver.

The STA510A is capable of delivering an output power of 50 W into 3 Ω x 4 channels with THD = 10% at V_{CC} = 37 V in single ended configuration. It can also deliver 100 W + 100 W into 6-Ω loads with THD = 10% at V_{CC} = 36 V in BTL configuration and 200W into 3 Ω with THD = 10% at V_{CC} = 36 V in single paralleled BTL configuration.

The input pins have a threshold proportional to the voltage on pin VL.

Table 1. Device summary

Order code	Operating temp. range	Package	Packaging
STA510A	0 to 70 °C	PowerSO36 EPU	Tube
STA510A13TR	0 to 70 °C	PowerSO36 EPU	Tape and reel

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Contents

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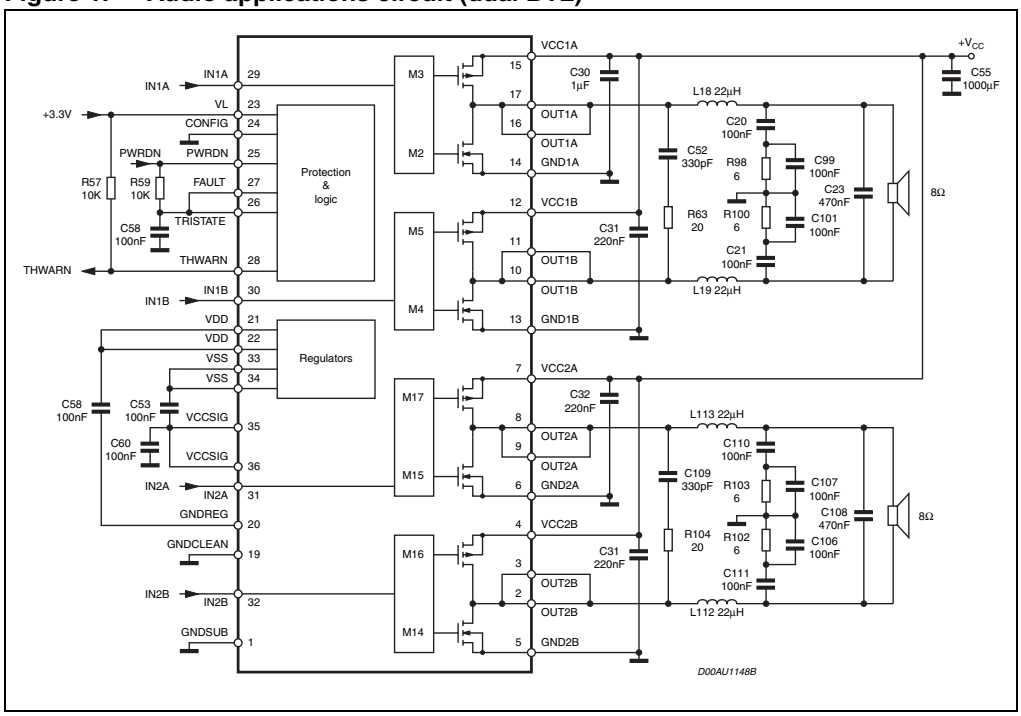
1 Audio applications circuit

Figure 1. Audio applications circuit (dual BTL)



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2 Pins description

Figure 2. Pin connection (top view)

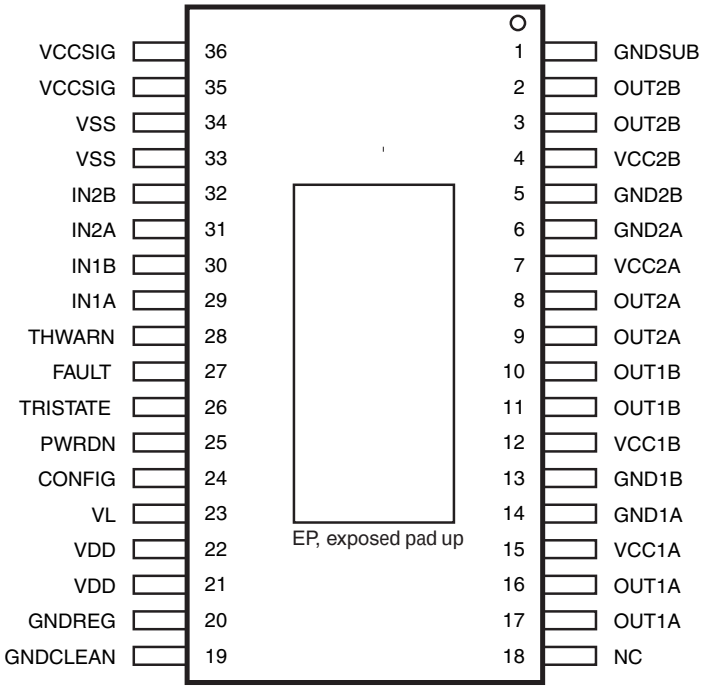

Table 2. Pin functions

Pin	Name	Description
1	GNDSUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	VCC2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	VCC2A	Positive supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	VCC1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	VCC1A	Positive supply
16, 17	OUT1A	Output half bridge 1A

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Table 2. Pin functions (continued)

Pin	Name	Description
18	NC	No internal connection
19	GNDCLEAN	Logical ground
20	GNDREG	Ground for regulator V_{DD}
21, 22	VDD	5-V regulator referred to ground
23	VL	Logic reference voltage
24	CONFIG	Configuration pin: 0: normal operation 1: single BTL (mono) mode, join the pins OUT1A to OUT1B and OUT2A to OUT2B (if IN1A is joined to IN1B and IN2A to IN2B)
25	PWRDN	Standby (power down): 0: low power consumption mode 1: normal operation
26	TRISTATE	High impedance control: 0: all power amplifiers in high-impedance state 1: normal operation
27	FAULT (1)	Fault advisor: 0: fault detected (short circuit or thermal) 1: normal operation
28	THWARN (1)	Thermal warning advisor: 0: junction temperature = 130 °C 1: normal operation
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	VSS	5-V regulator referred to $+V_{CC}$
35, 36	VCCSIG	Signal positive supply
-	EP	Exposed pad up

1. The pin is open collector. To have a high logic value it needs to be pulled up by a resistor.

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3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	DC supply voltage (pins 4,7,12,15)	-	-	44	V
V_{max}	Maximum voltage on pins 23 to 32	-	-	5.5	V
T_{op}	Operating temperature range	-	-	90	°C
P_{tot}	Power dissipation (T_{case} = 70 °C)	-	-	21	W
T_{stg}	Storage temperature	-40	-	150	°C
T_j	Junction operating temperature	-40	-	150	°C

3.2 Recommended operating conditions

Table 4. Recommended operating conditions (*)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	DC supply voltage	10	-	39.0	V
V_L	Input logic reference	2.7	3.3	5.0	V
T_{amb}	Ambient temperature	0	-	70	°C

(*) performances not guaranteed beyond recommended operating conditions

3.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	1	2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature	-	150	-	°C
T_{warn}	Thermal warning temperature	-	130	-	°C
t_{hSD}	Thermal shut-down hysteresis	-	25	-	°C

The power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. The PowerSO36 package of the STA510A includes an exposed pad or slug on the top of the device to provide a direct thermal path from the die to the heatsink.

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3.4 Electrical characteristics

The specifications given here were obtained with the conditions V_L = 3.3 V, V_{CC} = 36 V, R_L = 8 Ω, f_{sw} = 384 kHz and T_{amb} = 25 °C unless otherwise specified. See also *Figure 3*.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{dsON}	Power P-channel / N-channel MOSFET RdsON	I_d = 1 A	-	150	200	mΩ
I_{dss}	Power P-channel / N-channel leakage	-	-	-	100	µA
g_N	Power P-channel RdsON matching	I_d = 1 A	95	-	-	%
g_P	Power N-channel RdsON matching	I_d = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	See test circuit in *Figure 3*	-	10	20	ns
Dt_d	High current dead time (dynamic)	L = 22 µH, C = 470 nF, R_L = 8 Ω, I_d = 3 A, see *Figure 5*	-	-	50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load, V_{CC} = 30 V	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load, V_{CC} = 30 V	-	-	100	ns
t_r	Rise time	Resistive load, see *Figure 3*	-	-	25	ns
t_f	Fall time		-	-	25	ns
V_{INH}	High-level input voltage	-	-	-	V_L/2 + 300 mV	V
V_{INL}	Low-level input voltage	-	V_L/2 - 300 mV	-	-	V
I_{INH}	High-level Input current	Pin voltage = V_L	-	1	-	µA
I_{INL}	Low-level input current	Pin voltage = 0.3 V	-	1	-	µA
I_{PWRDNH}	High-level PWRDN pin input current	V_L = 3.3 V	-	35	-	µA
V_{LOW}	Low logical-state voltage (pins PWRDN, TRISTATE)	V_L = 2.7 V	-	-	0.70	V
		V_L = 3.3 V	-	-	0.80	V
		V_L = 5.0 V	-	-	0.85	V
V_{HIGH}	High logical-state voltage (pins PWRDN, TRISTATE)	V_L = 2.7 V	1.50	-	-	V
		V_L = 3.3 V	1.70	-	-	V
		V_L = 5.0 V	1.85	-	-	V
$I_{CCPWRDN}$	Supply current from V_{CC} in power down	V_{PWRDN} = 0 V	-	-	3	mA
I_{FAULT}	Output current on pins FAULT and THWARN with fault conditions	V_{pin} = 3.3 V	-	1	-	mA

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Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{VCCHIZ}	Supply current from V_{CC} in 3-state	V_{CC} = 30 V, $V_{TRISTATE}$ = 0 V	-	22	-	mA
I_{VCC}	Supply current from V_{CC} in operation (both channels switching)	V_{CC} = 30 V, Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	70	-	mA
I_{SCP}	Short-circuit current limit	-	5.5	6	-	A
V_{UVP}	Undervoltage protection threshold	-	-	7	-	V
t_{pw_min}	Output minimum pulse width	No load	25	-	40	ns
ESD	ESD maximum withstanding voltage range, test condition CDF-AEC-Q100-002- ”Human Body Model”		+/-1500V			V

Table 7. Logic truth table

TRISTATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	X	X	Off	Off	Off	Off	Hi-Z
1	0	0	Off	Off	On	On	Dump
1	0	1	Off	On	On	Off	Negative
1	1	0	On	Off	Off	On	Positive
1	1	1	On	On	Off	Off	Not used

Figure 3. Test circuit for low current dead time for single-ended applications

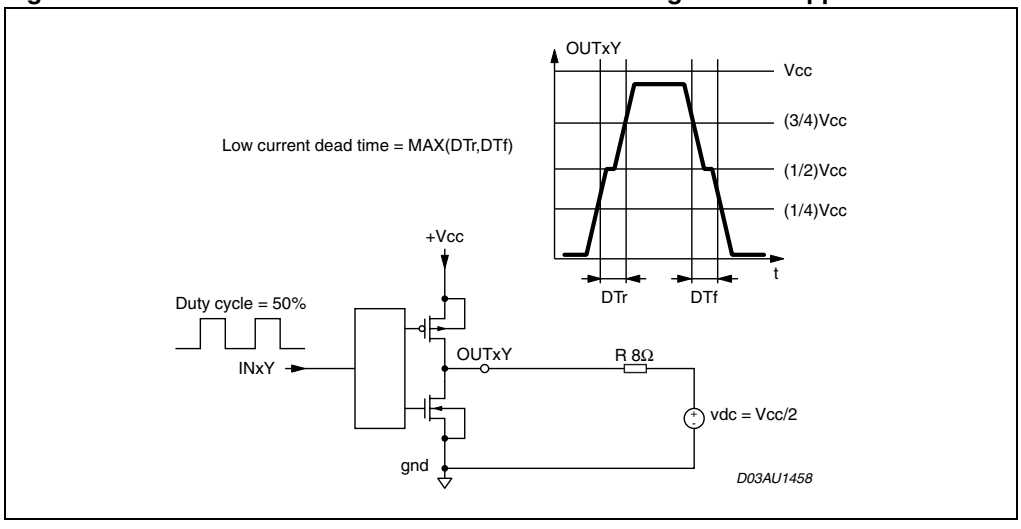

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Figure 4. Block diagram for high current dead time for bridge applications

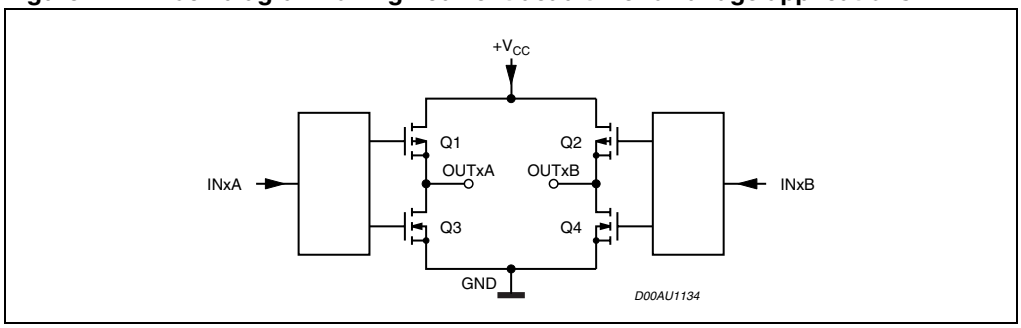
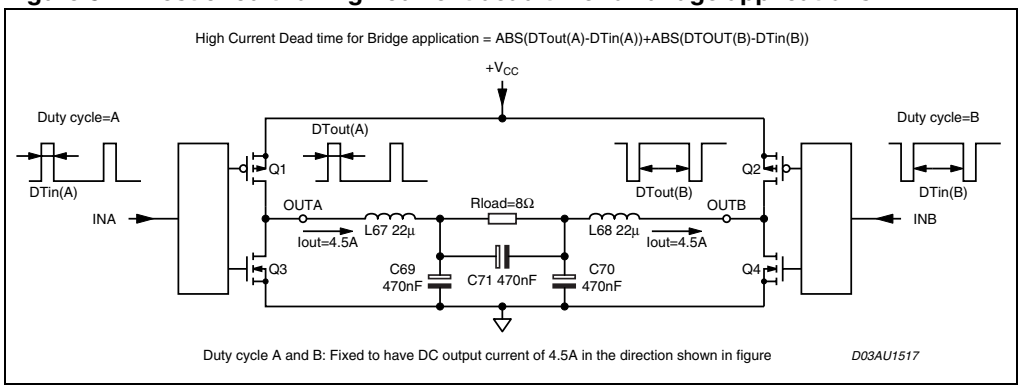


Figure 5. Test circuit for high current dead time for bridge applications



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4 Technical information

The STA510A is a dual channel H-bridge that is able to deliver 100 W per channel (into R_L = 6 Ω with THD = 10% and V_{CC} = 36 V) of audio output power very efficiently. It operates in conjunction with a pulse-width modulator driver such as the STA321 or STA309A.

The STA510A converts ternary-, phase-shift- or binary-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In differential mode (ternary, phase-shift or binary differential), two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to the damped ternary modulation operation.

In binary mode, both full bridge and half bridge modes are supported. The STA510A includes overcurrent and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 6. Block diagram of full-bridge DDX® or binary mode

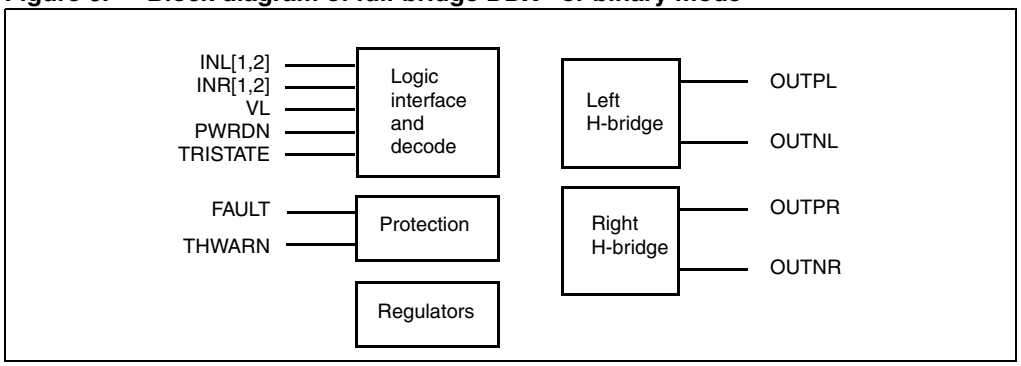
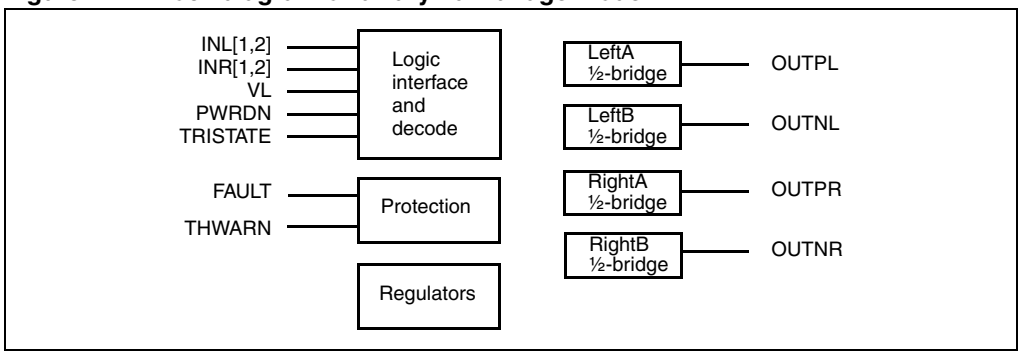


Figure 7. Block diagram of binary half-bridge mode



4.1 Logic interface and decode

The STA510A power outputs are controlled using one or two logic-level timing signals. In order to provide a proper logic interface, the VL input must operate at the same voltage as the DDX control logic supply.

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4.2 Protection circuitry

The STA510A includes protection circuitry for overcurrent and thermal overload conditions. A thermal warning pin (THWARN, pin 28, open drain MOSFET) is activated low when the IC temperature exceeds 130 °C, just in advance of thermal shutdown. When a fault condition is detected an internal fault signal immediately disables the output power MOSFETs, placing both H-bridges in a high-impedance state. At the same time the open-drain MOSFET of pin FAULT (pin 27) is switched on.

There are two possible modes subsequent to activating a fault.

- **Shutdown mode**: with pins FAULT (with pull-up resistor) and TRISTATE separate, an activated fault disables the device, signalling a low at pin FAULT output.
  The device may subsequently be reset to normal operation by toggling pin TRISTATE from high to low to high using an external logic signal.
- **Automatic recovery mode:** This is shown in the applications circuits below where pins FAULT and TRISTATE are connected together to a time-constant circuit (R59 and C58). An activated fault forces a reset on pin TRISTATE causing normal operation to resume following a delay determined by the time constant of the circuit.
  If the fault condition persists, the circuit operation repeats until the fault condition is cleared.
  An increase in the time constant of the circuit produces a longer recovery interval. Care must be taken in the overall system design not to exceed the protection thesholds under normal operation.

4.3 Power outputs

The STA510A power and output pins are duplicated to provide a low-impedance path for the device bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRISTATE pin should be used to set all power MOSFETs to the high-impedance state during power-up until the logic power supply, V_L, has settled.

4.4 Parallel output / high current operation

When using the DDX mode output, the STA510A outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA510A can provide up to 200 W into a 3-Ω load.

This mode of operation is enabled with the pin CONFIG (pin 24) connected to pin VDD. The inputs are joined so that IN1A = IN1B, IN2A = IN2B and similarly the outputs OUT1A = OUT1B, OUT2A = OUT2B as shown in *Figure 9 on page 12*

4.5 Output filtering

A passive 2nd-order filter is used on the STA510A power outputs to reconstruct the analog audio signal. System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6- or 8-Ω loads is shown in the application circuit of *Figure 8*, and for 4-Ω loads in *Figure 9* and *Figure 10*.

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4.6 Applications circuits

Figure 8. Typical stereo full bridge configuration for up to 2x 100 W

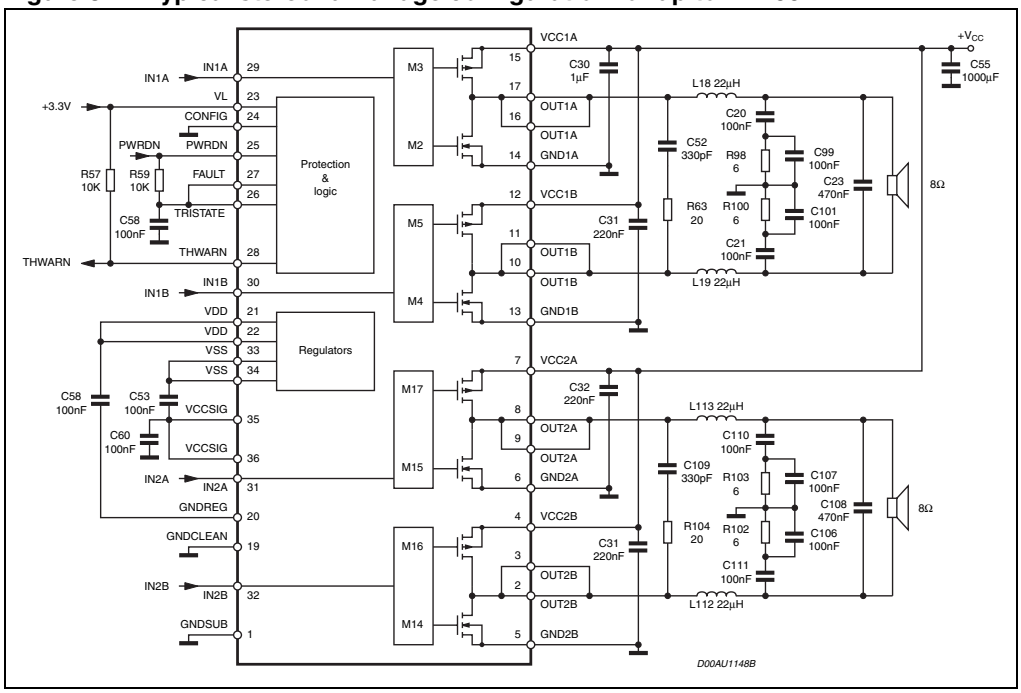

Figure 9. Typical single BTL configuration for up to 180 W

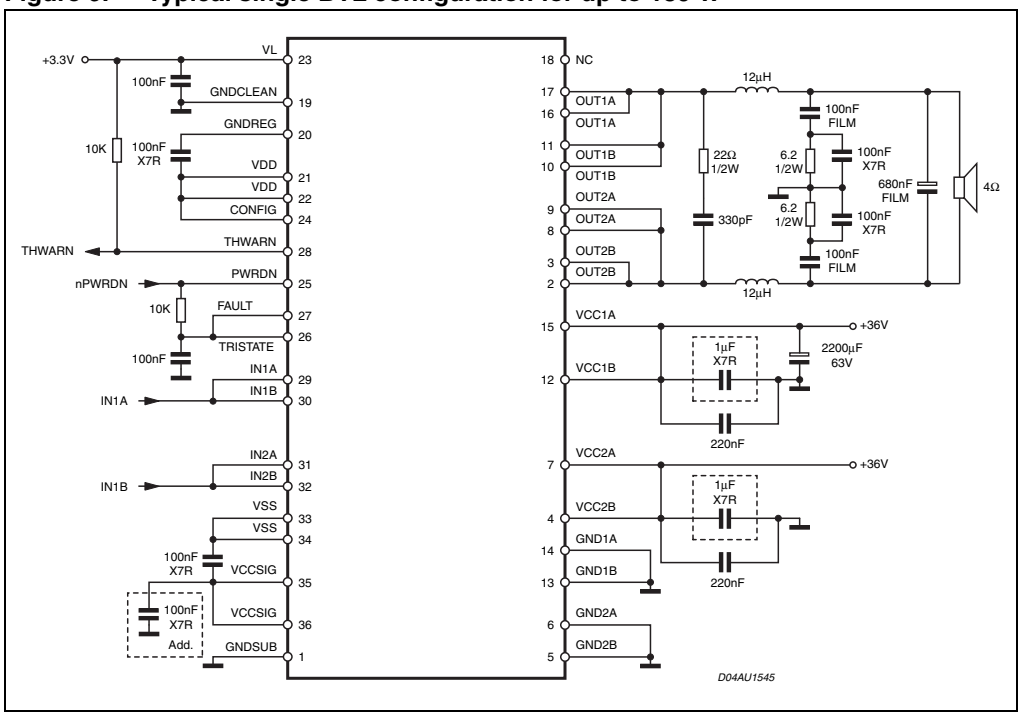

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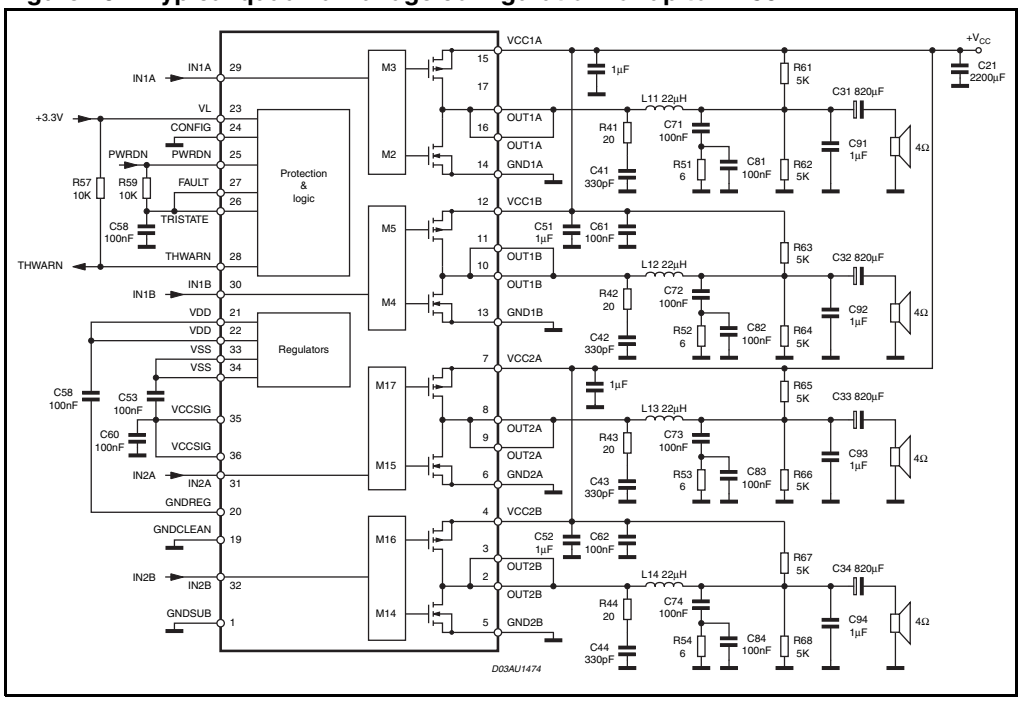
Figure 10. Typical quad half bridge configuration for up to 4x 50 W



Note: 1 In the above three circuits a PWM modulator as driver is needed.

2 The power estimations were made using the STA321+STA510A demo board. The peak power duration is for t ≤ 1 s.

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5 Package mechanical data

Figure 11. PowerSO36 EPU outline drawing package dimension

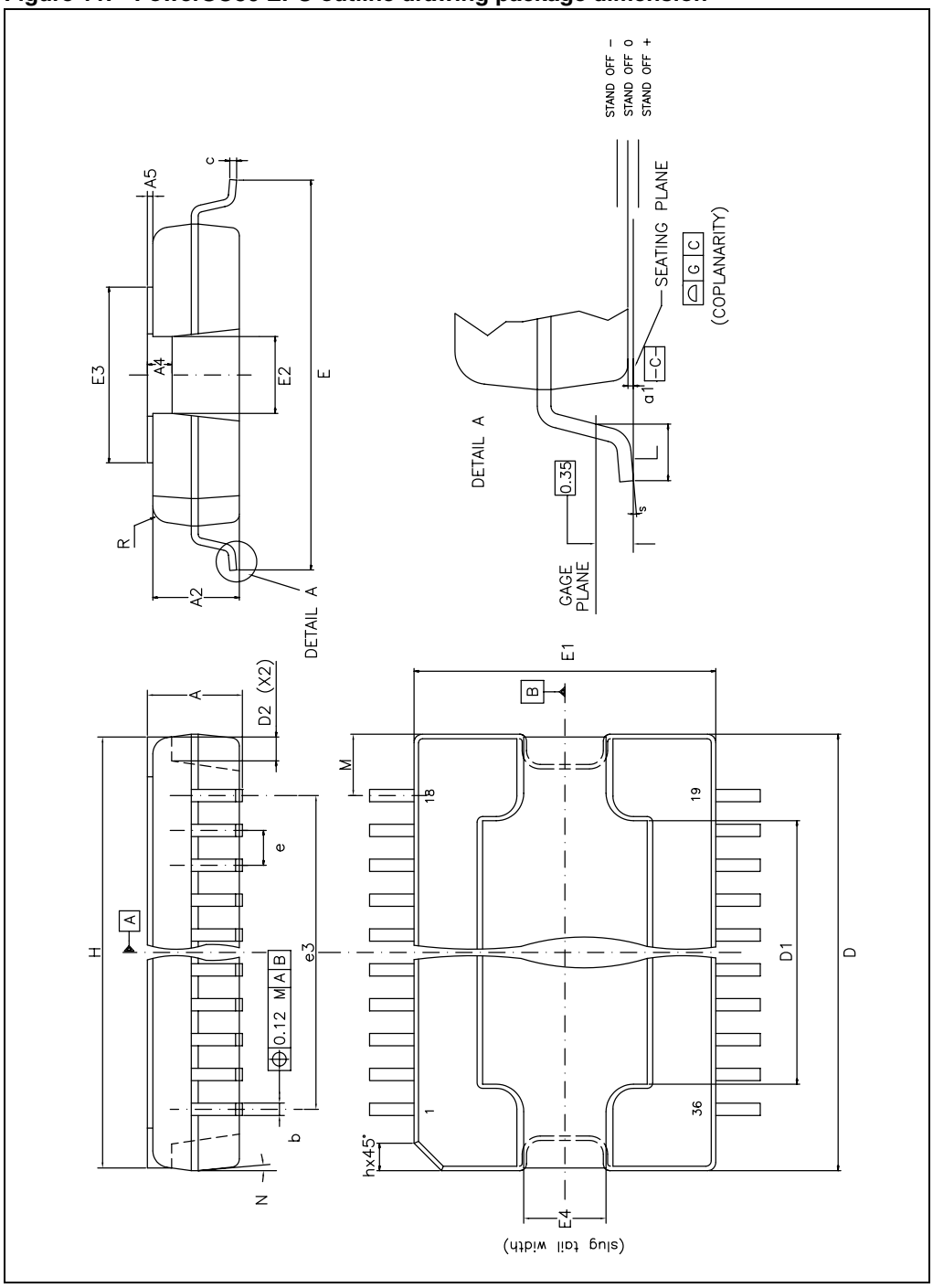

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Table 8. PowerSO36 EPU package dimension

Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.25	-	3.43	0.128	-	0.135
A2	3.10	-	3.20	0.122	-	0.126
A4	0.80	-	1.00	0.031	-	0.039
A5	-	0.20	-	-	0.008	-
a1	0.03	-	-0.04	0.001	-	-0.002
b	0.22	-	0.38	0.009	-	0.015
c	0.23	-	0.32	0.009	-	0.013
D	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.386
D2	-	1.00	-	-	0.039	-
E	13.90	-	14.50	0.547	-	0.571
E1	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90	-	-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
e	-	0.65	-	-	0.026	-
e3	-	11.05	-	-	0.435	-
G	0	-	0.08	0	-	0.003
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10	-	-	0.043
L	0.80	-	1.10	0.031	-	0.043
M	2.25	-	2.60	0.089	-	0.102
N	-	-	10 degrees	-	-	10 degrees
R	-	0.6	-	-	0.024	-
s	-	-	8 degrees	-	-	8 degrees

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6 Revision history

Table 9. Document revision history

Date	Revision	Changes
October 2004	1	Initial release.
11-Mar-2010	2	Updated description and applications circuits

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