

### FEATURES

- Complete single-chip JPEG2000 compression and decompression solution for video and still images
- Patented SURF™ (spatial ultraefficient recursive filtering) technology enables low power and low cost wavelet-based compression
- Supports both 9/7 and 5/3 wavelet transforms with up to 6 levels of transform
- Programmable tile/image size with widths up to 2048 pixels in 3-component 4:2:2 interleaved mode, and up to 4096 pixels in single-component mode
- Maximum tile/image height: 4096 pixels
- Video interface directly supporting ITU.R-BT656, SMPTE125M PAL/ NTSC, SMPTE274M, SMPTE293M (525p), ITU.R-BT1358 (625p) or any video format with a maximum input rate of 65 MSPS for irreversible mode or 40 MSPS for reversible mode
- Two or more ADV202s can be combined to support full-frame SMPTE274M HDTV (1080i) or SMPTE296M (720p)
- Interlaces temporally coherent frame-based SD video sources for improved performance
- Flexible asynchronous SRAM-style host interface allows glueless connection to most 16-/32-bit microcontrollers and ASICs
- 2.5 V to 3.3 V I/O and 1.5 V core supply
- 12 mm × 12 mm 121-lead CSPBGA, speed grade 115 MHz, or 13 mm × 13 mm 144-lead CSPBGA, speed grade 135 MHz, or 13 mm × 13 mm 144-lead CSPBGA, speed grade 150 MHz

### APPLICATIONS

- Networked video and image distribution systems
- Wireless video and image distribution
- Image archival/retrieval
- Digital CCTV and surveillance systems
- Digital cinema systems
- Professional video editing and recording
- Digital still cameras
- Digital camcorders

### GENERAL DESCRIPTION

The ADV202 is a single-chip JPEG2000 codec targeted for video and high bandwidth image compression applications that can benefit from the enhanced quality and feature set provided by the JPEG2000 (J2K)—ISO/IEC15444-1 image compression standard. The part implements the computationally intensive operations of the JPEG2000 image compression standard as well as providing fully compliant code-stream generation for most applications.

The ADV202's dedicated video port provides glueless connection to common digital video standards such as ITU.R-BT656, SMPTE125M, SMPTE293M (525p), ITU.R-BT1358 (625p), SMPTE274M(1080i), or SMPTE296M(720p). A variety of other high speed synchronous pixel and video formats can also be supported using the programmable framing and validation signals.

(continued on Page 3)

### FUNCTIONAL BLOCK DIAGRAM

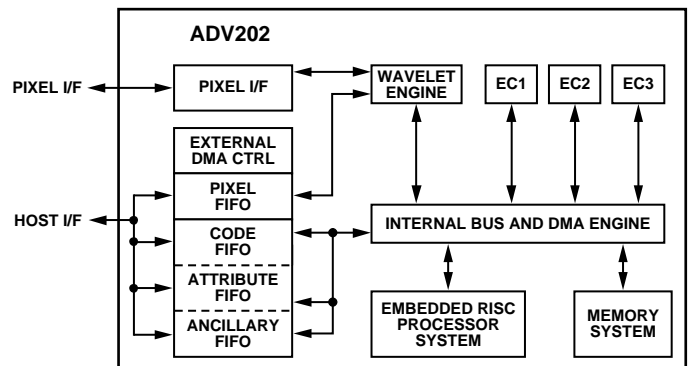


Figure 1.

### Rev. B

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## REVISION HISTORY

### 1/05—Rev. A to Rev. B

Updated Outline Dimensions .....

## GENERAL DESCRIPTION

(continued from Page 1)

The ADV202 can process images at a rate of 40 MSPS in reversible mode and at higher rates when used in irreversible mode. The ADV202 contains a dedicated wavelet transform engine, three entropy codecs, an on-board memory system, and an embedded RISC processor that can provide a complete JPEG2000 compression/decompression solution.

The wavelet processor supports the 9/7 irreversible wavelet transform and the 5/3 wavelet transform in reversible and irreversible modes. The entropy codecs support all features in the JPEG2000 Part 1 specification, except Maxshift ROI.

The ADV202 operates on a rectangular array of pixel samples called a tile. A tile can contain a complete image, up to the maximum supported size, or some portion of an image. The maximum horizontal tile size supported depends on the wavelet transform selected and the number of samples in the tile. Images larger than the ADV202's maximum tile size can be broken into individual tiles and then sent sequentially to the chip while still maintaining a single, fully compliant JPEG2000 code stream for the entire image.

### JPEG2000 FEATURE SUPPORT

The ADV202 supports a broad set of features that are included in Part 1 of the JPEG2000 standard (ISO/IEC 15444). See *Getting Started with ADV202* for information on the JPEG2000 features that the ADV202 currently supports.

Depending on the particular application requirements, the ADV202 can provide varying levels of JPEG2000 compression support. It can provide raw code-block and attribute data output, which allows the host software to have complete control over the generation of the JPEG2000 code stream and other aspects of the compression process such as bit-rate control. Otherwise, the ADV202 can create a complete, fully compliant JPEG2000 code stream (.j2c) and enhanced file formats such as .jp2, .jpx, and .mj2 (Motion JPEG2000). See *Getting Started with ADV202* for information on the formats that the ADV202 currently supports.

## SPECIFICATIONS

### SUPPLY VOLTAGES AND CURRENT

Table 1.

| Parameter          | Description   | Min   | Typ | Max                     | Unit |
|--------------------|---|-------|-----|-------------------------|------|
| VDD                | DC Supply Voltage, Core                                       | 1.425 | 1.5 | 1.575                   | V    |
| IOVDD              | DC Supply Voltage, I/O  | 2.375 | 3.3 | 3.63                    | V    |
| PLLVD              | DC Supply Voltage, PLL  | 1.425 | 1.5 | 1.575                   | V    |
| V <sub>input</sub> | Input Range   | -0.3  |     | V <sub>DDIO</sub> + 0.3 | V    |
| Temp               | Operating Ambient Temperature Range in Free Air               | -40   | +25 | +85                     | °C   |
| I <sub>DD</sub>    | Static Current <sup>1</sup>                                   |       |     | 300                     | mA   |
|                    | Dynamic Current, Core (JCLK Frequency = 150 MHz) <sup>2</sup> |       |     | 570                     | mA   |
|                    | Dynamic Current, Core (JCLK Frequency = 108 MHz)              |       |     | 420                     | mA   |
|                    | Dynamic Current, Core (JCLK Frequency = 81 MHz)               |       |     | 325                     | mA   |
|                    | Dynamic Current, I/O  |       |     | 20                      | mA   |
|                    | Dynamic Current, PLL  |       |     | 2.6                     | mA   |

<sup>1</sup> No clock or I/O activity.

<sup>2</sup> ADV202-150 only.

### INPUT/OUTPUT SPECIFICATIONS

Table 2.

| Parameter                      | Description                            | Test Conditions                             | Min | Typ | Max | Unit |
|--------------------------------|--|---|-----|-----|-----|------|
| V <sub>IH</sub> (3.3 V)        | High Level Input Voltage               | VDD = max                                   | 2.2 |     |     | V    |
| V <sub>IH</sub> (2.5 V)        | High Level Input Voltage               | VDD = max                                   | 1.9 |     |     | V    |
| V <sub>IL</sub> (3.3 V, 2.5 V) | Low Level Input Voltage                | VDD = min                                   |     |     | 0.6 | V    |
| V <sub>OH</sub> (3.3 V)        | High-Level Output Voltage              | VDD = min, I <sub>OH</sub> = -0.5 mA        | 2.4 |     |     | V    |
| V <sub>OH</sub> (2.5 V)        | High Level Output Voltage              | VDD = min, I <sub>OH</sub> = -0.5 mA        | 2.0 |     |     | V    |
| V <sub>OL</sub> (3.3 V, 2.5 V) | Low Level Output Voltage               | VDD = min, I <sub>OL</sub> = 2 mA           |     |     | 0.4 | V    |
| I <sub>IH</sub>                | High Level Input Current               | VDD = max, V <sub>IN</sub> = VDD            | 1.0 |     |     | μA   |
| I <sub>IL</sub>                | Low Level Input Current                | VDD = max, V <sub>IN</sub> = 0 <sub>V</sub> |     |     | 1   | μA   |
| I <sub>OZH</sub>               | High Level Three-State Leakage Current | VDD = max, V <sub>IN</sub> = VDD            | 1.0 |     |     | μA   |
| I <sub>OZL</sub>               | Low Level Three-State Leakage Current  | VDD = max, V <sub>IN</sub> = 0 <sub>V</sub> |     |     | 1.0 | μA   |
| C <sub>I</sub>                 | Input Pin Capacitance                  |   |     |     | 8   | pF   |
| C <sub>O</sub>                 | Output Pin Capacitance                 |   |     |     | 8   | pF   |

**CLOCK AND RESET SPECIFICATIONS**

Table 3.

| Parameter   | Description                  | Min  | Typ | Max | Unit                     |
|-------------|------------------------------|------|-----|-----|--------------------------|
| $t_{MCLK}$  | MCLK Period                  | 13.3 |     | 100 | ns                       |
| $t_{MCLKL}$ | MCLK Width Low               | 6    |     |     | ns                       |
| $t_{MCLKH}$ | MCLK Width High              | 6    |     |     | ns                       |
| $t_{VCLK}$  | VCLK Period                  | 13.4 |     | 50  | ns                       |
| $t_{VCLKL}$ | VCLK Width Low               | 5    |     |     | ns                       |
| $t_{VCLKH}$ | VCLK Width High              | 5    |     |     | ns                       |
| $t_{RST}$   | $\overline{RESET}$ Width Low | 5    |     |     | MCLK cycles <sup>1</sup> |

<sup>1</sup> For a definition of MCLK, see the PLL section.

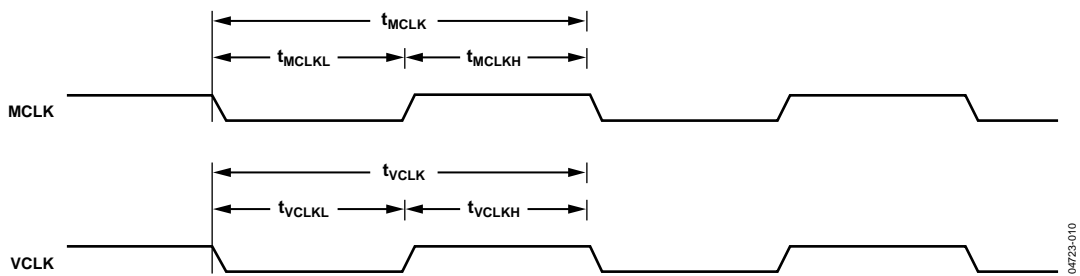


Figure 2. Input Clock

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## NORMAL HOST MODE—READ OPERATION

Table 4.

| Parameter                                  | Description  | Min                       | Typ | Max  | Unit              |
|--|--|---------------------------|-----|--|-------------------|
| $t_{\overline{\text{ACK}}} [\text{dir}]$   | $\overline{\text{RD}}$ to $\overline{\text{ACK}}$ , Direct Registers and FIFO Accesses | 5 ns                      |     | $1.5 \times \text{JCLK} + 7.0 \text{ ns}$  |                   |
| $t_{\overline{\text{ACK}}} [\text{indir}]$ | $\overline{\text{RD}}$ to $\overline{\text{ACK}}$ , Indirect Registers                 | $10.5 \times \text{JCLK}$ |     | $15.5 \times \text{JCLK} + 7.0 \text{ ns}$ |                   |
| $t_{\text{DRD}} [\text{dir}]$              | Read Access Time, Direct Registers   | 5 ns                      |     | $1.5 \times \text{JCLK} + 7.0 \text{ ns}$  |                   |
| $t_{\text{DRD}} [\text{indir}]$            | Read Access Time, Indirect Registers   | $10.5 \times \text{JCLK}$ |     | $15.5 \times \text{JCLK} + 7.0 \text{ ns}$ |                   |
| $t_{\text{HZRD}}$                          | Data Hold  | 2                         |     | 8.5  | ns                |
| $t_{\text{SC}}$                            | $\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup                                 | 0                         |     |  | ns                |
| $t_{\text{SA}}$                            | Address Setup  | 2                         |     |  | ns                |
| $t_{\text{HC}}$                            | $\overline{\text{CS}}$ Hold  | 0                         |     |  | ns                |
| $t_{\text{HA}}$                            | Address Hold   | 2                         |     |  | ns                |
| $t_{\text{RH}}$                            | Read Inactive Pulse Width  | 2.5                       |     |  | JCLK <sup>1</sup> |
| $t_{\text{RL}}$                            | Read Active Pulse Width  | 2.5                       |     |  | JCLK              |
| $t_{\text{RCYC}}$                          | Read Cycle Time, Direct Registers  | 5.0                       |     |  | JCLK              |

<sup>1</sup> For a definition of JCLK, see the PLL section.

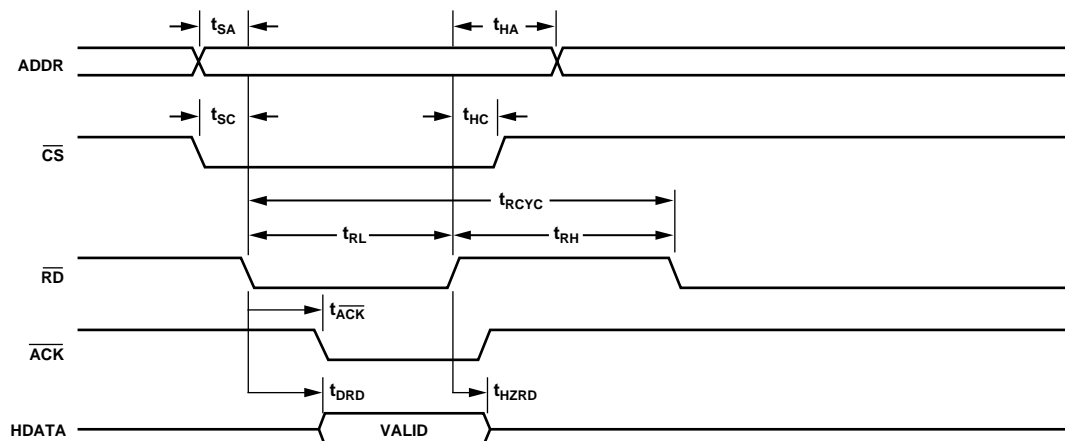


Figure 3. Normal Host Mode—Read Operation

**NORMAL HOST MODE—WRITE OPERATION**

Table 5.

| Parameter                       | Description  | Min | Typ | Max                        | Unit              |
|---------------------------------|--|-----|-----|----------------------------|-------------------|
| $t_{\overline{ACK}}$ (Direct)   | $\overline{WE}$ to $\overline{ACK}$ , Direct Registers and FIFO Accesses   | 5   |     | $1.5 \times JCLK + 7.0$ ns | ns                |
| $t_{\overline{ACK}}$ (Indirect) | $\overline{WE}$ to $\overline{ACK}$ , Indirect Registers                   | 5   |     | $2.5 \times JCLK + 7.0$ ns | ns                |
| $t_{SD}$                        | Data Setup   | 3.0 |     |                            | ns                |
| $t_{HD}$                        | Data Hold  | 1.5 |     |                            | ns                |
| $t_{SA}$                        | Address Setup  | 2   |     |                            | ns                |
| $t_{HA}$                        | Address Hold   | 2   |     |                            | ns                |
| $t_{SC}$                        | $\overline{CS}$ to $\overline{WE}$ Setup                                   | 0   |     |                            | ns                |
| $t_{HC}$                        | $\overline{CS}$ Hold   | 0   |     |                            | ns                |
| $t_{WH}$                        | Write Inactive Pulse Width (Minimum Time until Next $\overline{WE}$ Pulse) | 2.5 |     |                            | JCLK <sup>1</sup> |
| $t_{WL}$                        | Write Active Pulse Width   | 2.5 |     |                            | JCLK              |
| $t_{WCYC}$                      | Write Cycle Time   | 5   |     |                            | JCLK              |

<sup>1</sup> For a definition of JCLK, see the PLL section.

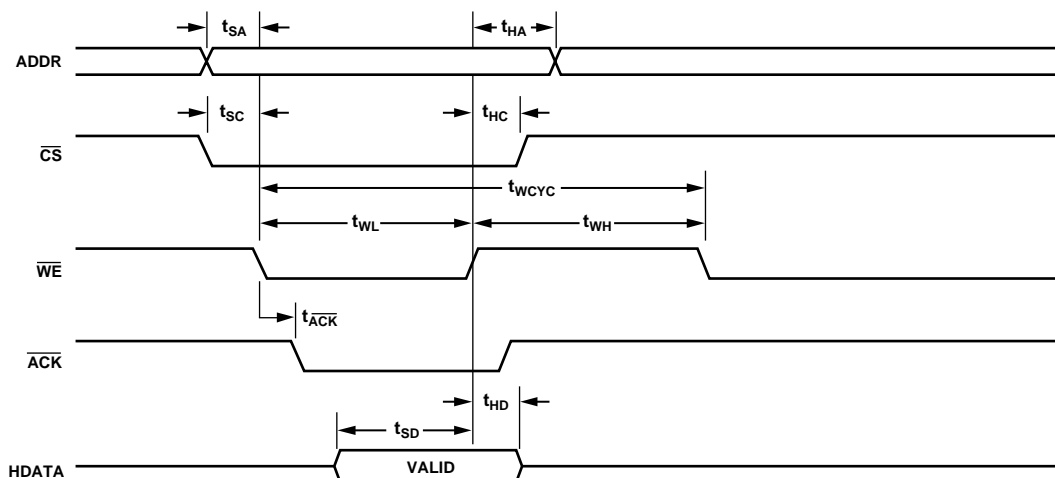


Figure 4. Normal Host Mode—Write Operation

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## DREQ/DACK DMA MODE—SINGLE FIFO WRITE OPERATION

Table 6.

| Parameter                   | Description  | Min | Typ | Max                                | Unit                     |
|-----------------------------|--|-----|-----|------------------------------------|--------------------------|
| $\overline{DREQ}_{PULSE}^1$ | $\overline{DREQ}$ Pulse Width  | 1   |     | 15                                 | JCLK cycles <sup>2</sup> |
| $t_{DREQ}$                  | $\overline{DACK}$ Assert to Subsequent $\overline{DREQ}$ Delay           | 2.5 |     | $3.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |
| $t_{WESU}$                  | $\overline{WE}$ to $\overline{DACK}$ Setup                               | 0   |     |                                    | ns                       |
| $t_{SU}$                    | Data to $\overline{DACK}$ Deassert Setup                                 | 2   |     |                                    | ns                       |
| $t_{HD}$                    | Data to $\overline{DACK}$ Deassert Hold                                  | 2   |     |                                    | ns                       |
| $\overline{DACK}_{LO}$      | $\overline{DACK}$ Assert Pulse Width                                     | 2   |     |                                    | JCLK cycles              |
| $\overline{DACK}_{HI}$      | $\overline{DACK}$ Deassert Pulse Width                                   | 2   |     |                                    | JCLK cycles              |
| $t_{WEHD}$                  | $\overline{WE}$ Hold after $\overline{DACK}$ Deassert                    | 0   |     |                                    | ns                       |
| $\overline{WFSRQ}$          | $\overline{WE}$ Assert to $\overline{FSRQ}$ Deassert (FIFO Full)         | 1.5 |     | $2.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |
| $t_{DREQRTN}$               | $\overline{DACK}$ to $\overline{DREQ}$ Deassert ( $DR \times PULS = 0$ ) | 2.5 |     | $3.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |

<sup>1</sup> Applies to assigned DMA channel, if EDMOD0 or EDMOD1 <14:11> is programmed to a value that is not 0. Pulse width depends on the value programmed.

<sup>2</sup> For a definition of JCLK, see the PLL section.

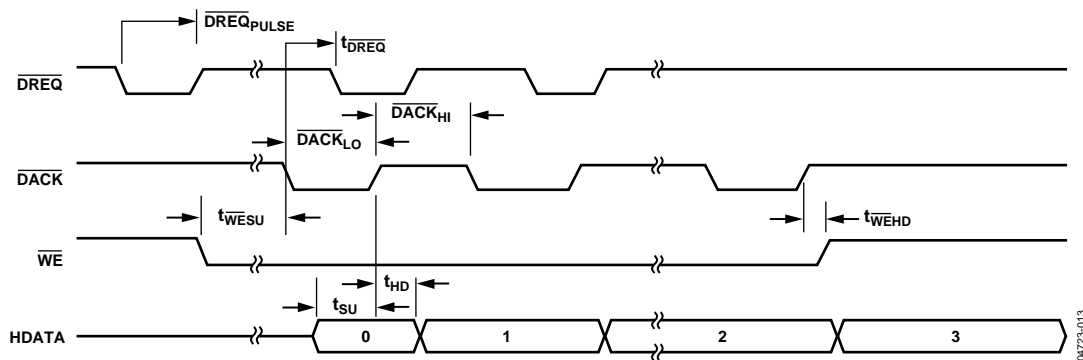


Figure 5. Single Write for  $\overline{DREQ}/\overline{DACK}$  DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> NOT Programmed to a Value of 0000)

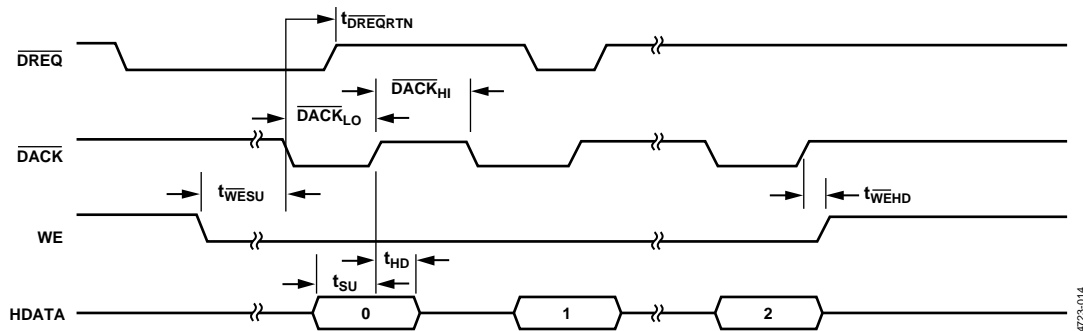


Figure 6. Single Write for  $\overline{DREQ}/\overline{DACK}$  DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> Programmed to a Value of 0000)



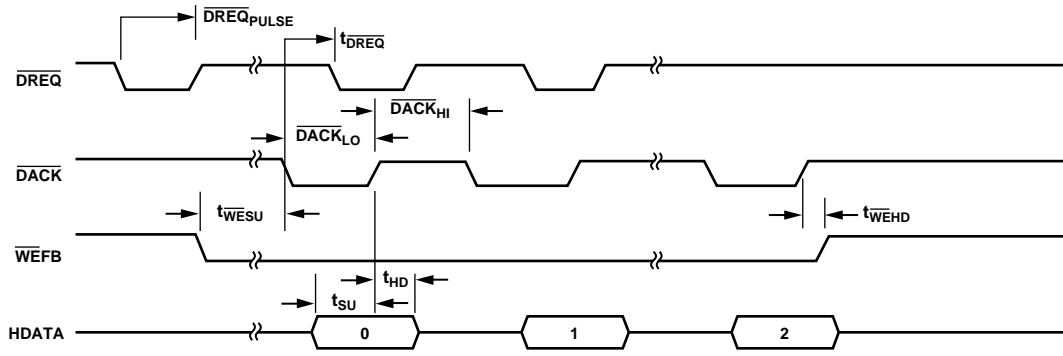


Figure 7. Fly-By DMA Mode—Single Write Cycle ( $\overline{DREQ}$  Pulse Width Is Programmable)

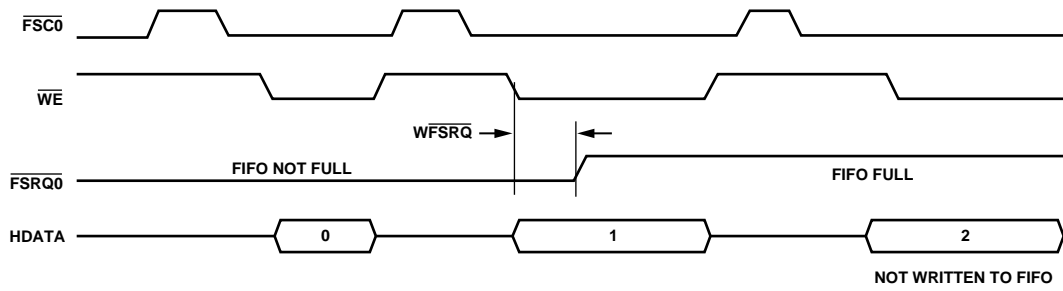


Figure 8. DCS DMA Mode—Single Write Access (Rev. 0.1 and Higher)

## DREQ/DACK DMA MODE—SINGLE FIFO READ OPERATION

Table 7.

| Parameter                 | Description  | Min | Typ | Max                                | Unit                     |
|---------------------------|--|-----|-----|------------------------------------|--------------------------|
| $\overline{DREQ}_{PULSE}$ | $\overline{DREQ}$ Pulse Width <sup>1</sup>                               | 1   |     | 15                                 | JCLK cycles <sup>2</sup> |
| $t_{\overline{DREQ}}$     | $\overline{DACK}$ Assert to Subsequent $\overline{DREQ}$ Delay           | 2.5 |     | $3.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |
| $t_{\overline{RD}SU}$     | $\overline{RD}$ to $\overline{DACK}$ Setup                               | 0   |     |                                    | ns                       |
| $t_{\overline{RD}}$       | $\overline{DACK}$ to Data Valid  | 2.5 |     | 11                                 | ns                       |
| $t_{HD}$                  | Data Hold  | 1.5 |     |                                    | ns                       |
| $\overline{DACK}_{LO}$    | $\overline{DACK}$ Assert Pulse Width                                     | 2   |     |                                    | JCLK cycles              |
| $\overline{DACK}_{HI}$    | $\overline{DACK}$ Deassert Pulse Width                                   | 2   |     |                                    | JCLK cycles              |
| $t_{\overline{RD}HD}$     | $\overline{RD}$ Hold after $\overline{DACK}$ Deassert                    | 0   |     |                                    | ns                       |
| $\overline{RD}_{FSRQ}$    | $\overline{RD}$ Assert to $\overline{FSRQ}$ Deassert (FIFO Empty)        | 1.5 |     | $2.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |
| $t_{\overline{DREQ}RTN}$  | $\overline{DACK}$ to $\overline{DREQ}$ Deassert ( $DR \times PULS = 0$ ) | 2.5 |     | $3.5 \times JCLK + 7.5 \text{ ns}$ | JCLK cycles              |

<sup>1</sup> Applies to assigned DMA channel, if EDMOD0 or EDMOD1 <14:11> is programmed to a nonzero value.

<sup>2</sup> For a definition of JCLK, see the PLL section.

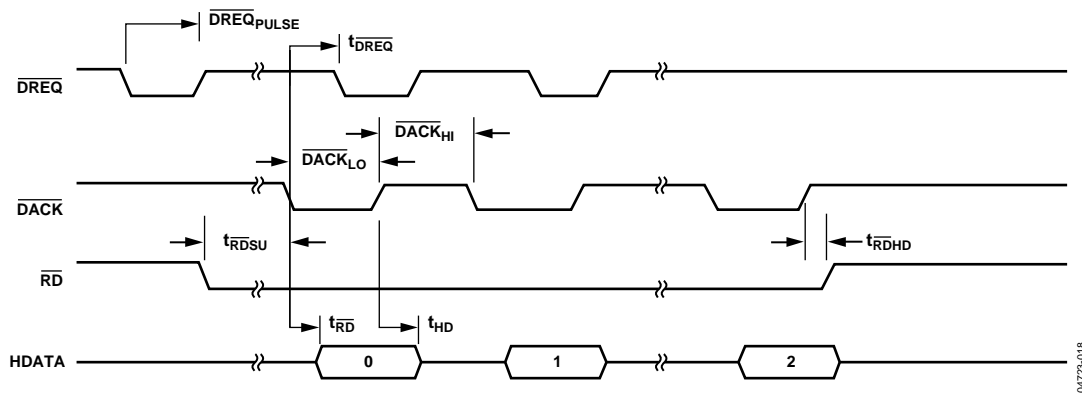


Figure 9. Single Read for  $\overline{DREQ}/\overline{DACK}$  DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> NOT Programmed to a Value of 0000)

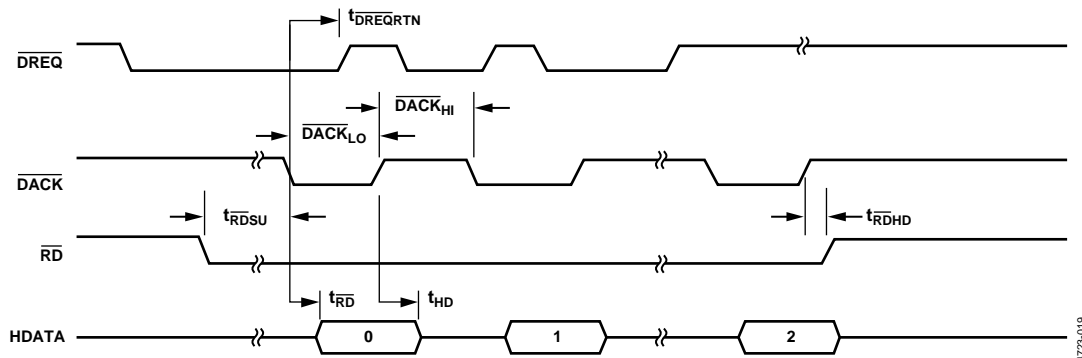


Figure 10. Single Read for  $\overline{DREQ}/\overline{DACK}$  DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> Programmed to a Value of 0000)

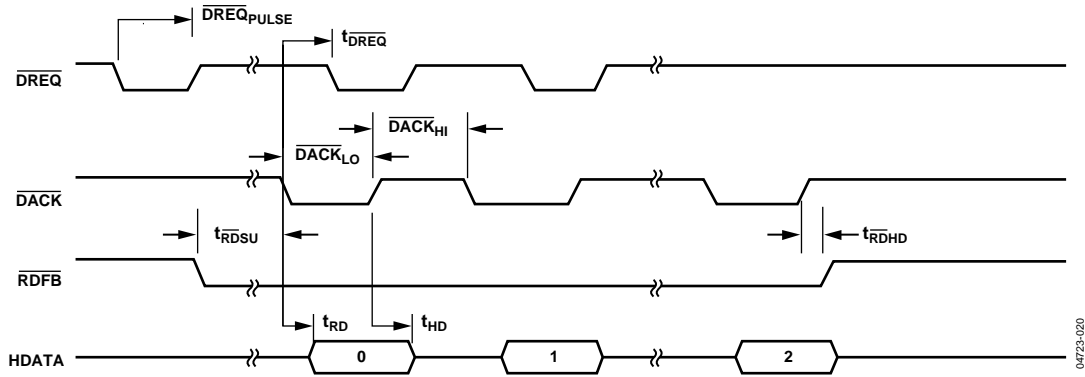


Figure 11. Fly-By DMA Mode—Single Read Cycle  
(DREQ Pulse Width Is Programmable)

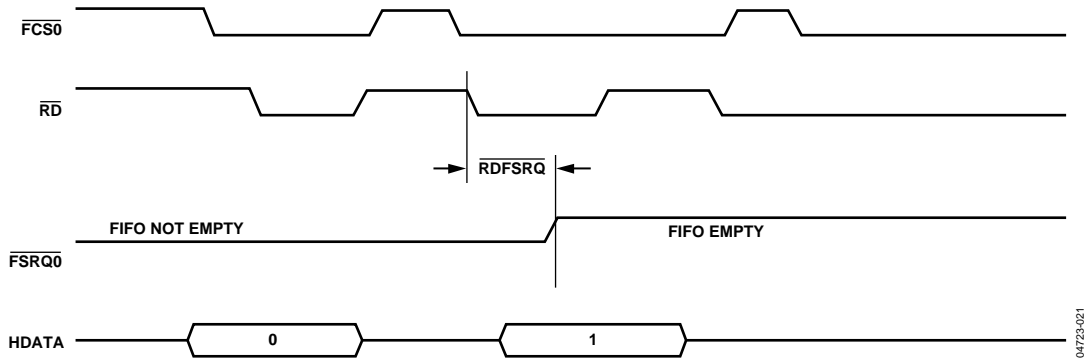


Figure 12. DCS DMA Mode—Single Read Access (Rev. 0.1 and Higher)

## EXTERNAL DMA MODE—FIFO WRITE, BURST MODE

Table 8.

| Parameter                               | Description   | Min | Typ | Max  | Unit                     |
|---|---|-----|-----|--|--------------------------|
| $\overline{\text{DREQ}}_{\text{PULSE}}$ | $\overline{\text{DREQ}}$ Pulse Width <sup>1</sup>   | 1   |     | 15   | JCLK cycles <sup>2</sup> |
| $t_{\overline{\text{DREQRTN}}}$         | $\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Deassert ( $\text{DR} \times \text{Pulse} = 0$ ) | 2.5 |     | $3.5 \times \text{JCLK} + 7.5 \text{ ns}$              | JCLK cycles              |
| $t_{\overline{\text{DACKSU}}}$          | $\overline{\text{DACK}}$ to $\overline{\text{WE}}$ Setup  | 0   |     |  | ns                       |
| $t_{\text{SU}}$                         | Data Setup  | 2.5 |     |  | ns                       |
| $t_{\text{HD}}$                         | Data Hold   | 2   |     |  | ns                       |
| $\overline{\text{WE}}_{\text{LO}}$      | $\overline{\text{WE}}$ Assert Pulse Width   | 1.5 |     |  | JCLK cycles              |
| $\overline{\text{WE}}_{\text{HI}}$      | $\overline{\text{WE}}$ Deassert Pulse Width   | 1.5 |     |  | JCLK cycles              |
| $t_{\overline{\text{DREQWAIT}}}$        | $\overline{\text{DACK}}$ Deassert to Next $\overline{\text{DREQ}}$                                    | 2.5 |     | $4.5 \times \text{JCLK} + 7.5 \text{ ns}$ <sup>3</sup> | JCLK cycles              |

<sup>1</sup> Applies to assigned DMA channel, if EDMOD0 or EDMOD1 <14:11> is programmed to a value that is not 0. Pulse width depends on the value programmed.

<sup>2</sup> For a definition of JCLK, see the PLL section.

<sup>3</sup> If sufficient space is available in FIFO.

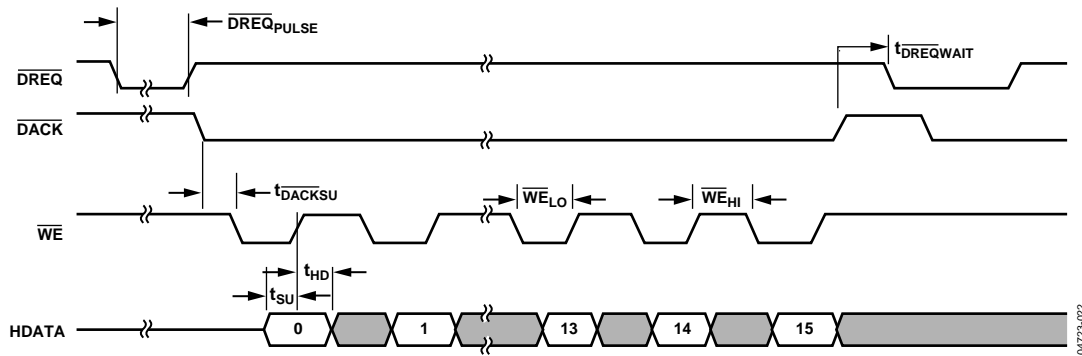


Figure 13. Burst Write Cycle for  $\overline{\text{DREQ}}$ /DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> NOT Programmed to a Value of 0000)

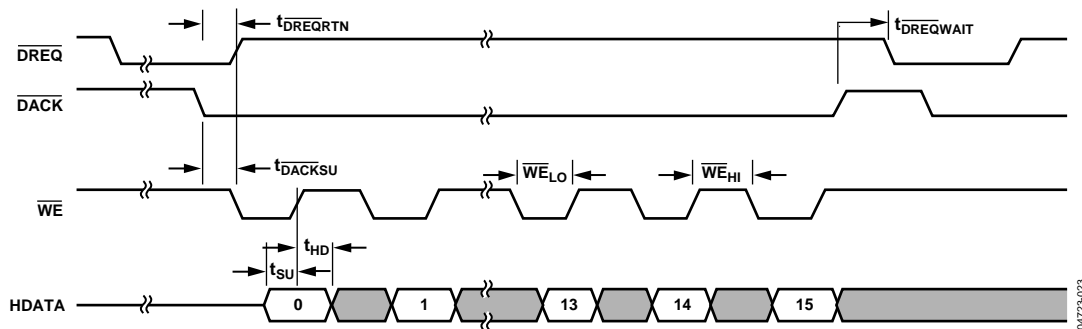


Figure 14. Burst Write Cycle for  $\overline{\text{DREQ}}$ /DMA Mode for Assigned DMA Channel (EDMOD0/EDMOD1 <14:11> Programmed to a Value of 0000)

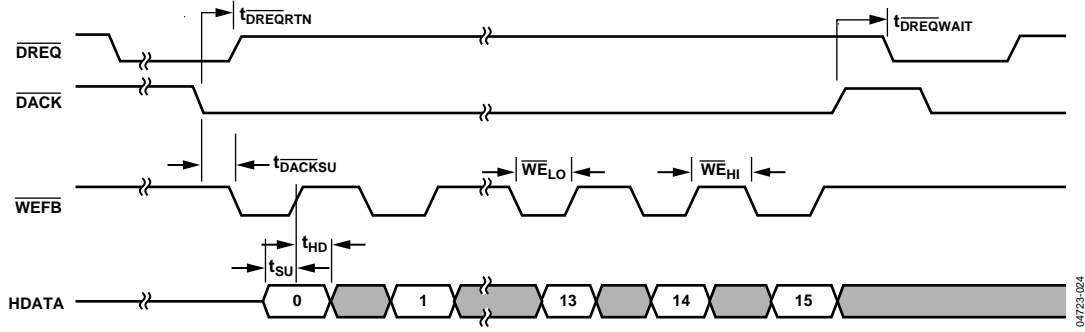


Figure 15. Burst Write Cycle for Fly-By DMA Mode  
(DREQ Pulse Width Is Programmable)

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**EXTERNAL DMA MODE—FIFO READ, BURST MODE**

Table 9.

| Parameter                      | Description                           | Min | Typ | Max                              | Unit                     |
|--------------------------------|---------------------------------------|-----|-----|----------------------------------|--------------------------|
| DREQ <sub>PULSE</sub>          | DREQ Pulse Width <sup>1</sup>         | 1   |     | 15                               | JCLK cycles <sup>2</sup> |
| t <sub>DREQRTN</sub>           | DACK to DREQ Deassert (DR × PULS = 0) | 2.5 |     | 3.5 × JCLK + 7.5 ns              | JCLK cycles              |
| t <sub>DACK<sup>SU</sup></sub> | DACK to RD Setup                      | 0   |     |                                  | ns                       |
| t <sub>RD</sub>                | DACK to Data Valid                    | 2.5 |     | 9.7                              | ns                       |
| t <sub>HD</sub>                | Data Hold                             | 2.5 |     |                                  | ns                       |
| RD <sub>LO</sub>               | RD Assert Pulse Width                 | 1.5 |     |                                  | JCLK cycles              |
| RD <sub>HI</sub>               | RD Deassert Pulse Width               | 1.5 |     |                                  | JCLK cycles              |
| t <sub>DREQWAIT</sub>          | DACK Deassert to Next DREQ            | 2.5 |     | 3.5 × JCLK + 7.5 ns <sup>3</sup> | JCLK cycles              |

<sup>1</sup> Applies to assigned DMA channel, if EDMOD0 or EDMOD1 <14:11> is programmed to a value that is not 0. Pulse width depends on the value programmed.

<sup>2</sup> For a definition of JCLK, see the PLL section.

<sup>3</sup> If sufficient data is available in FIFO.

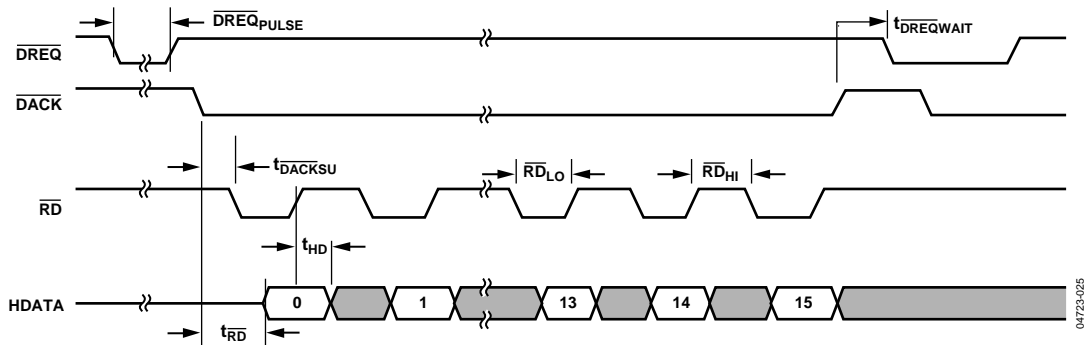


Figure 16. Burst Read Cycle for DREQ/DACK DMA Mode for Assigned DMA Channel  
(EMOD0/EDMOD1 <14:11> NOT Programmed to a Value of 0)

04723-025

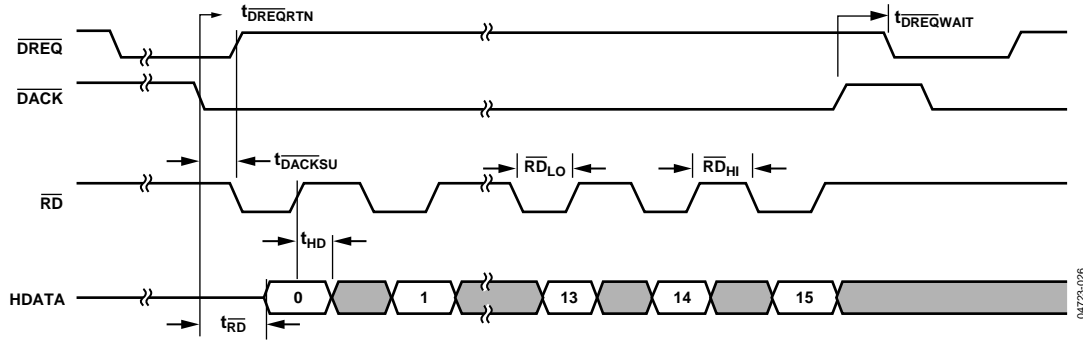


Figure 17. Burst Read Cycle for  $\overline{DREQ}/\overline{DACK}$  DMA Mode for Assigned DMA Channel  
(EMOD0/EDMOD1 <14:11> Programmed to a Value of 0000)

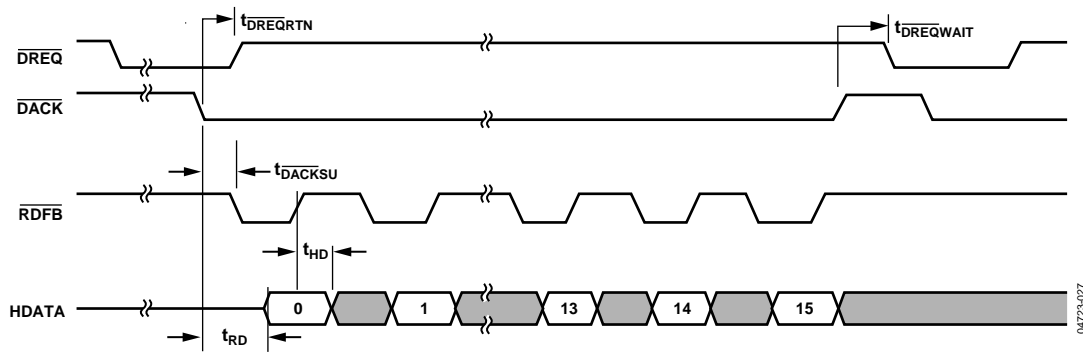


Figure 18. Burst Read Cycle, Fly-By DMA Mode  
(DREQ Pulse Width Is Programmable)

**STREAMING MODE (JDATA)—FIFO READ/WRITE**

Table 10.

| Parameter           | Description                    | Min | Typ | Max                  | Unit                     |
|---------------------|--------------------------------|-----|-----|----------------------|--------------------------|
| JDATA <sub>TD</sub> | MCLK to JDATA Valid            | 1.5 |     | 2.5 × JCLK + 7.0 ns  | JCLK cycles <sup>1</sup> |
| VALID <sub>TD</sub> | MCLK to VALID Assert/ Deassert | 1.5 |     | 2.5 × JCLK + .7.0 ns | JCLK cycles              |
| HOLD <sub>SU</sub>  | HOLD Setup to Rising MCLK      | 3   |     |                      | ns                       |
| HOLD <sub>HD</sub>  | HOLD Hold from Rising MCLK     | 3   |     |                      | ns                       |
| JDATA <sub>SU</sub> | JDATA Setup to Rising MCLK     | 3   |     |                      | ns                       |
| JDATA <sub>HD</sub> | JDATA Hold from Rising MCLK    | 3   |     |                      | ns                       |

<sup>1</sup> For a definition of JCLK, see the PLL section.

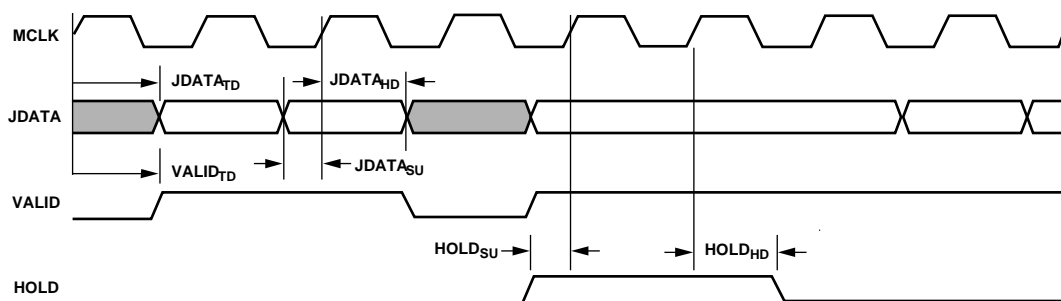


Figure 19. Streaming Mode Timing—Encode Mode JDATA Output

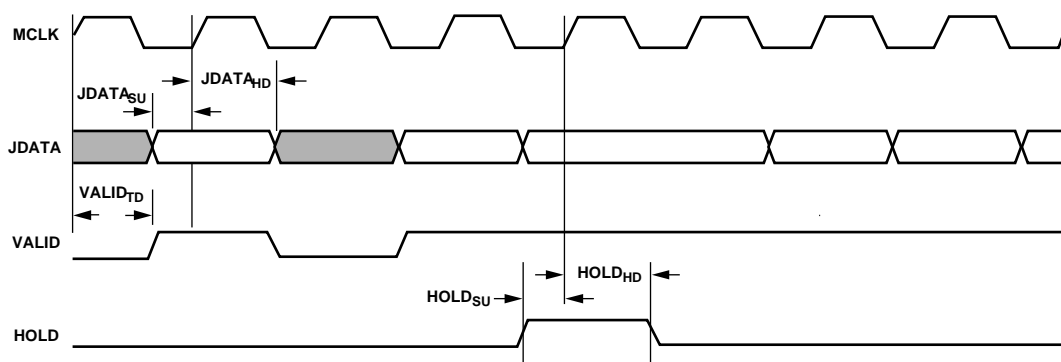


Figure 20. Streaming Mode Timing—Decode Mode JDATA Input

**VDATA MODE TIMING**

Table 11.

| Parameter           | Description                               | Min | Typ | Max | Unit |
|---------------------|---|-----|-----|-----|------|
| VDATA <sub>TD</sub> | VCLK to VDATA Valid Delay (VDATA Output)  |     |     | 12  | ns   |
| VDATA <sub>SU</sub> | VDATA Setup to Rising VCLK (VDATA Input)  | 4   |     |     | ns   |
| VDATA <sub>HD</sub> | VDATA Hold from Rising VCLK (VDATA Input) | 4   |     |     | ns   |
| HSYNC <sub>SU</sub> | HSYNC Setup to Rising VCLK                | 3   |     |     | ns   |
| HSYNC <sub>HD</sub> | HSYNC Hold from Rising VCLK               | 4   |     |     | ns   |
| HSYNC <sub>TD</sub> | VCLK to HSYNC Valid Delay                 |     |     | 12  | ns   |
| VSYNC <sub>SU</sub> | VSYNC Setup to Rising VCLK                | 3   |     |     | ns   |
| VSYNC <sub>HD</sub> | VSYNC Hold from Rising VCLK               | 4   |     |     | ns   |
| VSYNC <sub>TD</sub> | VCLK to VSYNC Valid Delay                 |     |     | 12  | ns   |
| FIELD <sub>SU</sub> | FIELD Setup to Rising VCLK                | 4   |     |     | ns   |

| Parameter           | Description  | Min | Typ | Max | Unit        |
|---------------------|--|-----|-----|-----|-------------|
| FIELD <sub>HD</sub> | FIELD Hold from Rising VCLK  | 3   |     |     | ns          |
| FIELD <sub>TD</sub> | VCLK to FIELD Valid  |     |     | 12  |             |
| SYNC DELAY          | Decode Data Sync Delay for HD Input with EAV/SAV Codes   |     | 7   |     | VCLK cycles |
|                     | Decode Data Sync Delay for SD Input with EAV/SAV Codes   |     | 9   |     | VCLK cycles |
|                     | Decode Data Sync Delay for DUAL_LANE (Extended) Input  |     | 7   |     | VCLK cycles |
|                     | Decode Data Sync Delay for HVF Input (from First Rising VCLK after HSYNC Low to First Data Sample) |     | 10  |     | VCLK cycles |

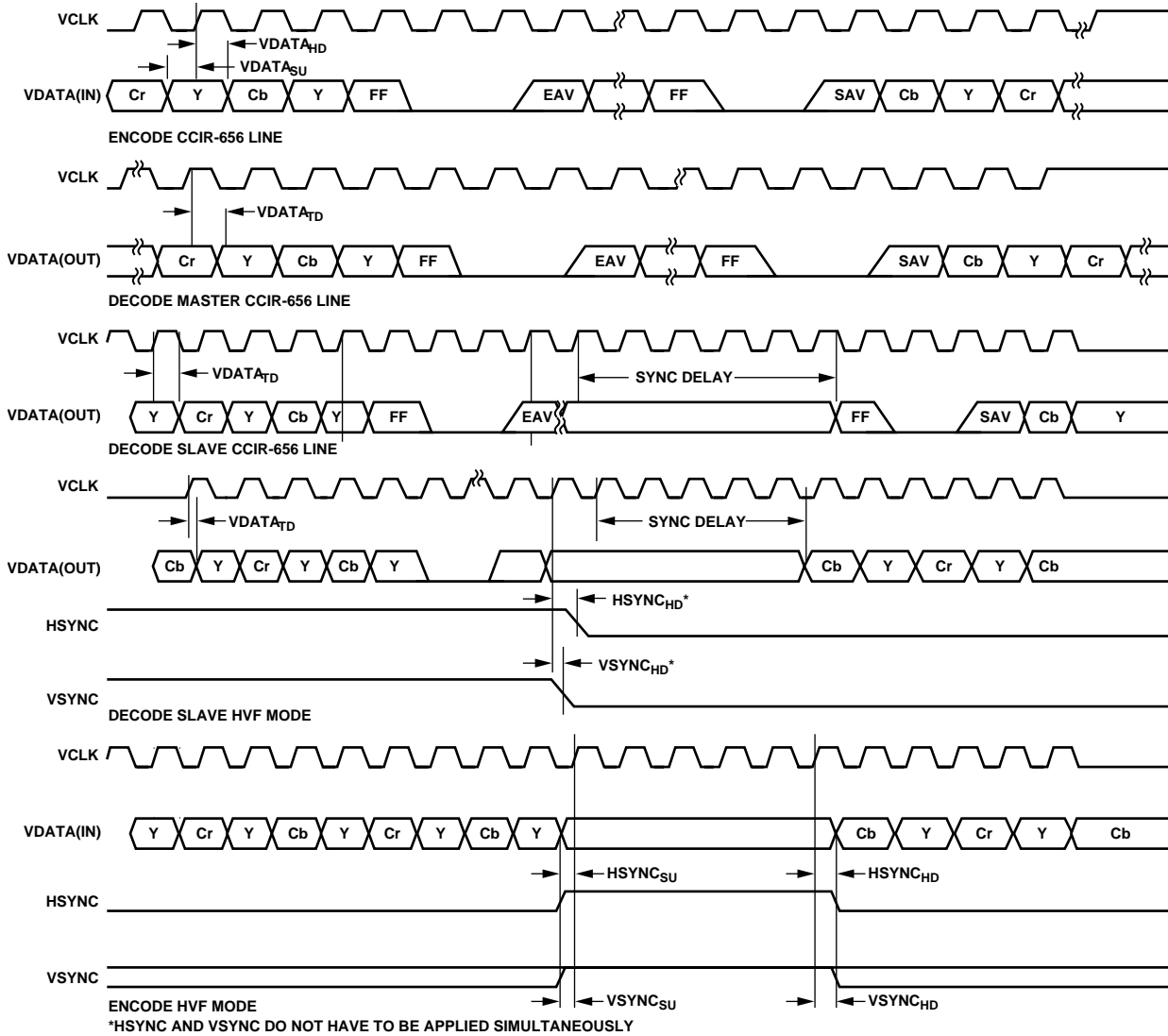


Figure 21. Video Mode Timing

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**RAW PIXEL MODE TIMING**

Table 12.

| Parameter           | Description                                       | Min | Typ | Max | Unit |
|---------------------|---|-----|-----|-----|------|
| VDATA <sub>TD</sub> | VCLK to PIXELDATA Valid Delay (PIXELDATA Output)  |     |     | 12  | ns   |
| VDATA <sub>SU</sub> | PIXELDATA Setup to Rising VCLK (PIXELDATA Input)  | 4   |     |     | ns   |
| VDATA <sub>HD</sub> | PIXELDATA Hold from Rising VCLK (PIXELDATA Input) | 4   |     |     | ns   |
| VRDY <sub>TD</sub>  | VCLK to VRDY Valid Delay                          |     |     | 12  | ns   |
| VFRM <sub>SU</sub>  | VFRM Setup to Rising VCLK (VFRAME Input)          | 3   |     |     | ns   |
| VFRM <sub>HD</sub>  | VFRM Hold from Rising VCLK (VFRAME Input)         | 4   |     |     | ns   |
| VFRM <sub>TD</sub>  | VCLK to VFRM Valid Delay (VFRAME Output)          |     |     | 12  | ns   |
| VSTRB <sub>SU</sub> | VSTRB Setup to Rising VCLK                        | 4   |     |     | ns   |
| VSTRB <sub>HD</sub> | VSTRB Hold from Rising VCLK                       | 3   |     |     | ns   |

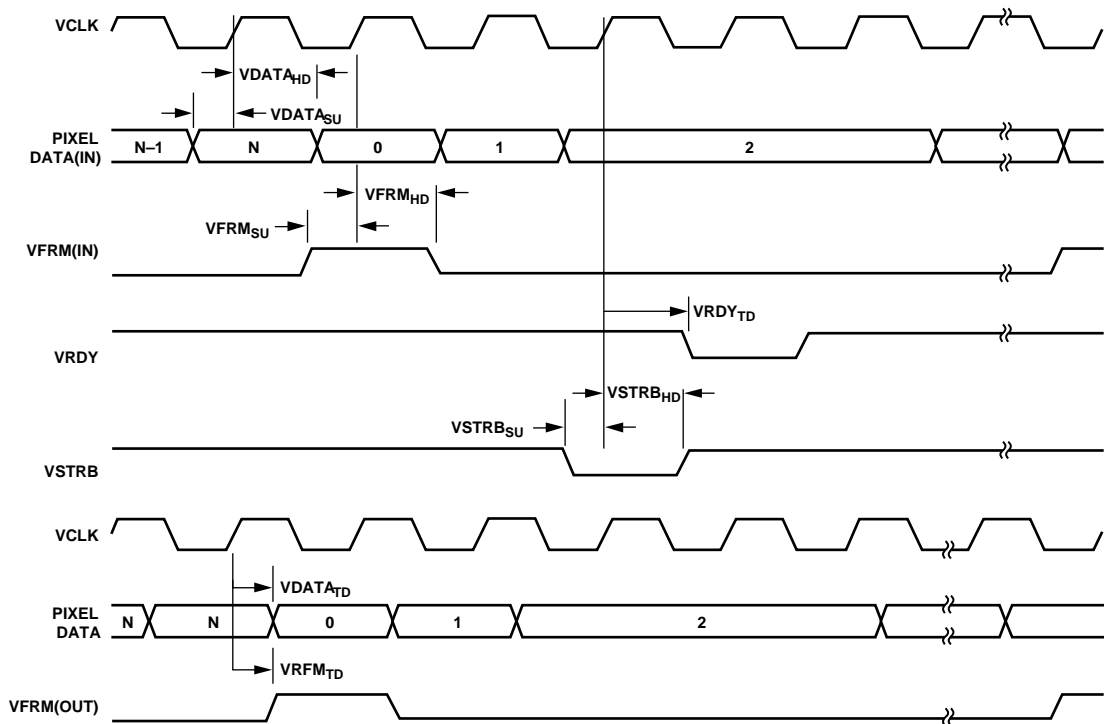


Figure 22. Raw Pixel Mode Timing

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## SPI PORT TIMING

Table 13.

| Parameter            | Description                                 | Min | Typ | Max | Unit |
|----------------------|---|-----|-----|-----|------|
| SCLK <sub>FALL</sub> | S_CLK Fall Time                             |     | 5   |     | ns   |
| SCLK <sub>RISE</sub> | S_CLK Rise Time                             |     | 5   |     | ns   |
| SCLK <sub>hi</sub>   | SCLK high time                              |     | 75  |     | ns   |
| SCLK <sub>lo</sub>   | SCLK Low Time                               |     | 75  |     | ns   |
| Data <sub>su</sub>   | Data Setup Time                             | 6.5 |     |     | ns   |
| Data <sub>hd</sub>   | Data Hold Time                              | 6.5 |     |     | ns   |
| CSEL <sub>SU</sub>   | Active Setup Time                           | 135 |     |     | ns   |
| CSEL <sub>HD</sub>   | Active Hold Time                            | 155 |     |     | ns   |
| DV_SCLK              | SCLK to Output Data Valid                   |     | 2   |     | ns   |
| DV_CS                | $\overline{\text{CS}}$ to Output Data Valid | 36  |     |     | ns   |
| SCLK                 | SCLK Period                                 |     | 150 |     | ns   |

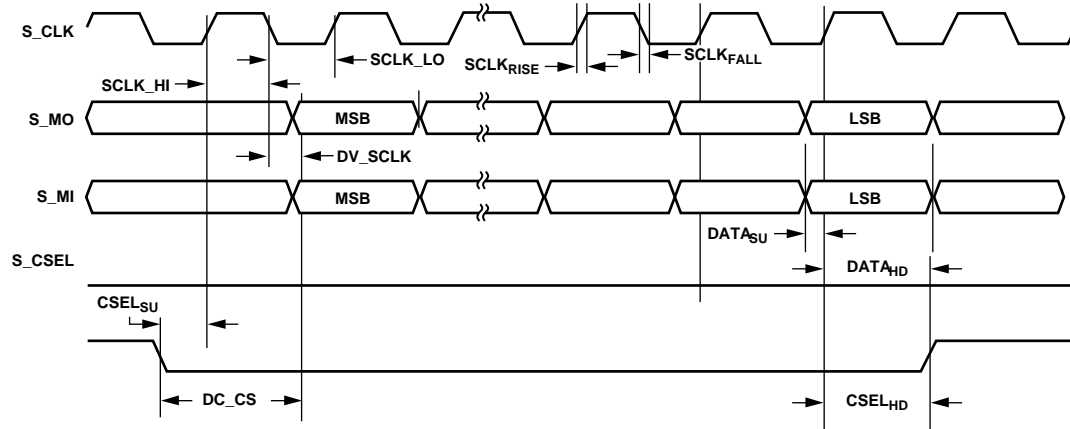


Figure 23. SPI Port—Input Timing

04723-032

## PIN BGA ASSIGNMENTS AND FUNCTION DESCRIPTIONS

### PIN BGA ASSIGNMENTS

Table 14. Pin BGA Assignments for 121-Lead Package

| Pin No. | Pin Location | Pin Description     | Pin No. | Pin Location | Pin Description              |
|---------|--------------|---------------------|---------|--------------|------------------------------|
| 1       | A1           | DGND                | 50      | E6           | DGND                         |
| 2       | A2           | HDATA[2]            | 51      | E7           | DGND                         |
| 3       | A3           | VDD                 | 52      | E8           | IOVDD                        |
| 4       | A4           | DGND                | 53      | E9           | VCLK                         |
| 5       | A5           | HDATA[0]            | 54      | E10          | FIELD                        |
| 6       | A6           | HDATA[1]            | 55      | E11          | DGND                         |
| 7       | A7           | VDATA[1]            | 56      | F1           | DGND                         |
| 8       | A8           | VDD                 | 57      | F2           | HDATA[19]_VDATA[15]          |
| 9       | A9           | DGND                | 58      | F3           | HDATA[20]_VDATA[16]          |
| 10      | A10          | VDATA[0]            | 59      | F4           | HDATA[21]_VDATA[17]          |
| 11      | A11          | DGND                | 60      | F5           | DGND                         |
| 12      | B1           | HDATA[3]            | 61      | F6           | DGND                         |
| 13      | B2           | HDATA[4]            | 62      | F7           | DGND                         |
| 14      | B3           | HDATA[5]            | 63      | F8           | $\overline{\text{DREQ0}}$    |
| 15      | B4           | HDATA[7]            | 64      | F9           | $\overline{\text{DACK0}}$    |
| 16      | B5           | HDATA[8]            | 65      | F10          | $\overline{\text{DREQ1}}$    |
| 17      | B6           | IOVDD               | 66      | F11          | DGND                         |
| 18      | B7           | VDATA[6]            | 67      | G1           | DGND                         |
| 19      | B8           | VDATA[5]            | 68      | G2           | HDATA[22]_VDATA[18]          |
| 20      | B9           | VDATA[4]            | 69      | G3           | HDATA[23]_VDATA[19]          |
| 21      | B10          | VDATA[2]            | 70      | G4           | HDATA[24]_VDATA[20]_JDATA[0] |
| 22      | B11          | VDATA[3]            | 71      | G5           | DGND                         |
| 23      | C1           | DGND                | 72      | G6           | DGND                         |
| 24      | C2           | HDATA[6]            | 73      | G7           | DGND                         |
| 25      | C3           | HDATA[9]            | 74      | G8           | IOVDD                        |
| 26      | C4           | HDATA[10]           | 75      | G9           | $\overline{\text{DACK1}}$    |
| 27      | C5           | HDATA[11]           | 76      | G10          | $\overline{\text{IRQ}}$      |
| 28      | C6           | IOVDD               | 77      | G11          | DGND                         |
| 29      | C7           | VDATA[9]            | 78      | H1           | HDATA[28]_JDATA[4]           |
| 30      | C8           | IOVDD               | 79      | H2           | HDATA[27]_VDATA[23]_JDATA[3] |
| 31      | C9           | VDATA[8]            | 80      | H3           | HDATA[26]_VDATA[22]_JDATA[2] |
| 32      | C10          | VDATA[7]            | 81      | H4           | HDATA[25]_VDATA[21]_JDATA[1] |
| 33      | C11          | DGND                | 82      | H5           | IOVDD                        |
| 34      | D1           | HDATA[12]           | 83      | H6           | DGND                         |
| 35      | D2           | HDATA[13]           | 84      | H7           | VDD                          |
| 36      | D3           | HDATA[14]           | 85      | H8           | $\overline{\text{ACK}}$      |
| 37      | D4           | HDATA[15]           | 86      | H9           | $\overline{\text{RD}}$       |
| 38      | D5           | IOVDD               | 87      | H10          | ADDR[1]                      |
| 39      | D6           | DGND                | 88      | H11          | ADDR[3]                      |
| 40      | D7           | VDD                 | 89      | J1           | DGND                         |
| 41      | D8           | VSYN                | 90      | J2           | HDATA[31]_JDATA[7]           |
| 42      | D9           | HSYN                | 91      | J3           | HDATA[30]_JDATA[6]           |
| 43      | D10          | VDATA[10]           | 92      | J4           | HDATA[29]_JDATA[5]           |
| 44      | D11          | VDATA[11]           | 93      | J5           | IOVDD                        |
| 45      | E1           | DGND                | 94      | J6           | TEST1                        |
| 46      | E2           | HDATA[18]_VDATA[14] | 95      | J7           | $\overline{\text{WE}}$       |
| 47      | E3           | HDATA[17]_VDATA[13] | 96      | J8           | $\overline{\text{CS}}$       |
| 48      | E4           | HDATA[16]_VDATA[12] | 97      | J9           | ADDR[0]                      |
| 49      | E5           | DGND                |         |              |                              |

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| Pin No. | Pin Location | Pin Description |
|---------|--------------|-----------------|
| 98      | J10          | TEST3           |
| 99      | J11          | DGND            |
| 100     | K1           | SCOMM[4]        |
| 101     | K2           | SCOMM[3]        |
| 102     | K3           | SCOMM[0]        |
| 103     | K4           | SCOMM[1]        |
| 104     | K5           | IOVDD           |
| 105     | K6           | IOVDD           |
| 106     | K7           | IOVDD           |
| 107     | K8           | ADDR[2]         |
| 108     | K9           | TEST2           |
| 109     | K10          | TEST5           |

| Pin No. | Pin Location | Pin Description |
|---------|--------------|-----------------|
| 110     | K11          | DGND            |
| 111     | L1           | DGND            |
| 112     | L2           | SCOMM[7]        |
| 113     | L3           | SCOMM[6]        |
| 114     | L4           | SCOMM[5]        |
| 115     | L5           | SCOMM[2]        |
| 116     | L6           | TEST4           |
| 117     | L7           | RESET           |
| 118     | L8           | DGND            |
| 119     | L9           | MCLK            |
| 120     | L10          | PLLVD           |
| 121     | L11          | DGND            |

Table 15. Pin BGA Assignments for 144-Lead Package

| Pin No. | Pin Location | Pin Description |
|---------|--------------|-----------------|
| 1       | A1           | DGND            |
| 2       | A2           | HDATA[2]        |
| 3       | A3           | HDATA[1]        |
| 4       | A4           | HDATA[0]        |
| 5       | A5           | DGND            |
| 6       | A6           | DGND            |
| 7       | A7           | DGND            |
| 8       | A8           | DGND            |
| 9       | A9           | VDATA[2]        |
| 10      | A10          | VDATA[1]        |
| 11      | A11          | VDATA[0]        |
| 12      | A12          | DGND            |
| 13      | B1           | HDATA[5]        |
| 14      | B2           | HDATA[4]        |
| 15      | B3           | HDATA[3]        |
| 16      | B4           | IOVDD           |
| 17      | B5           | DGND            |
| 18      | B6           | VDD             |
| 19      | B7           | VDD             |
| 20      | B8           | DGND            |
| 21      | B9           | IOVDD           |
| 22      | B10          | VDATA[5]        |
| 23      | B11          | VDATA[4]        |
| 24      | B12          | VDATA[3]        |
| 25      | C1           | HDATA[8]        |
| 26      | C2           | HDATA[7]        |
| 27      | C3           | HDATA[6]        |
| 28      | C4           | IOVDD           |
| 29      | C5           | DGND            |
| 30      | C6           | VDD             |
| 31      | C7           | VDD             |
| 32      | C8           | DGND            |
| 33      | C9           | IOVDD           |
| 34      | C10          | VDATA[8]        |
| 35      | C11          | VDATA[7]        |
| 36      | C12          | VDATA[6]        |
| 37      | D1           | HDATA[11]       |

| Pin No. | Pin Location | Pin Description     |
|---------|--------------|---------------------|
| 38      | D2           | HDATA[10]           |
| 39      | D3           | HDATA[9]            |
| 40      | D4           | IOVDD               |
| 41      | D5           | DGND                |
| 42      | D6           | VDD                 |
| 43      | D7           | VDD                 |
| 44      | D8           | DGND                |
| 45      | D9           | IOVDD               |
| 46      | D10          | VDATA[11]           |
| 47      | D11          | VDATA[10]           |
| 48      | D12          | VDATA[9]            |
| 49      | E1           | HDATA[14]           |
| 50      | E2           | HDATA[13]           |
| 51      | E3           | HDATA[12]           |
| 52      | E4           | DGND                |
| 53      | E5           | DGND                |
| 54      | E6           | DGND                |
| 55      | E7           | DGND                |
| 56      | E8           | DGND                |
| 57      | E9           | FIELD               |
| 58      | E10          | VSYNC               |
| 59      | E11          | HSYNC               |
| 60      | E12          | VCLK                |
| 61      | F1           | HDATA[18]_VDATA[14] |
| 62      | F2           | HDATA[17]_VDATA[13] |
| 63      | F3           | HDATA[16]_VDATA[12] |
| 64      | F4           | HDATA[15]           |
| 65      | F5           | DGND                |
| 66      | F6           | DGND                |
| 67      | F7           | DGND                |
| 68      | F8           | DGND                |
| 69      | F9           | DACK1               |
| 70      | F10          | DREQ1               |
| 71      | F11          | DACK0               |
| 72      | F12          | DREQ0               |
| 73      | G1           | HDATA[22]_VDATA[18] |

| Pin No. | Pin Location | Pin Description              |
|---------|--------------|------------------------------|
| 74      | G2           | HDATA[21]_VDATA[17]          |
| 75      | G3           | HDATA[20]_VDATA[16]          |
| 76      | G4           | HDATA[19]_VDATA[15]          |
| 77      | G5           | DGND                         |
| 78      | G6           | DGND                         |
| 79      | G7           | DGND                         |
| 80      | G8           | DGND                         |
| 81      | G9           | DGND                         |
| 82      | G10          | $\overline{\text{IRQ}}$      |
| 83      | G11          | $\overline{\text{ACK}}$      |
| 84      | G12          | $\overline{\text{RD}}$       |
| 85      | H1           | HDATA[26]_VDATA[22]_JDATA[2] |
| 86      | H2           | HDATA[25]_VDATA[21]_JDATA[1] |
| 87      | H3           | HDATA[24]_VDATA[20]_JDATA[0] |
| 88      | H4           | HDATA[23]_VDATA[19]          |
| 89      | H5           | DGND                         |
| 90      | H6           | DGND                         |
| 91      | H7           | DGND                         |
| 92      | H8           | DGND                         |
| 93      | H9           | DGND                         |
| 94      | H10          | $\overline{\text{WR}}$       |
| 95      | H11          | $\overline{\text{CS}}$       |
| 96      | H12          | ADDR[0]                      |
| 97      | J1           | HDATA[30]_JDATA[6]           |
| 98      | J2           | HDATA[29]_JDATA[5]           |
| 99      | J3           | HDATA[28]_JDATA[4]           |
| 100     | J4           | HDATA[27]_VDATA[23]_JDATA[3] |
| 101     | J5           | DGND                         |
| 102     | J6           | VDD                          |
| 103     | J7           | VDD                          |
| 104     | J8           | DGND                         |
| 105     | J9           | DGND                         |
| 106     | J10          | ADDR[1]                      |
| 107     | J11          | ADDR[2]                      |
| 108     | J12          | ADDR[3]                      |
| 109     | K1           | SCOMM[1]                     |

| Pin No. | Pin Location | Pin Description           |
|---------|--------------|---------------------------|
| 110     | K2           | SCOMM[0]                  |
| 111     | K3           | HDATA[31]_JDATA[7]        |
| 112     | K4           | IOVDD                     |
| 113     | K5           | DGND                      |
| 114     | K6           | VDD                       |
| 115     | K7           | VDD                       |
| 116     | K8           | DGND                      |
| 117     | K9           | IOVDD                     |
| 118     | K10          | TEST3                     |
| 119     | K11          | TEST2                     |
| 120     | K12          | TEST1                     |
| 121     | L1           | SCOMM[4]                  |
| 122     | L2           | SCOMM[3]                  |
| 123     | L3           | SCOMM[2]                  |
| 124     | L4           | IOVDD                     |
| 125     | L5           | DGND                      |
| 126     | L6           | VDD                       |
| 127     | L7           | VDD                       |
| 128     | L8           | DGND                      |
| 129     | L9           | IOVDD                     |
| 130     | L10          | TEST5                     |
| 131     | L11          | $\overline{\text{RESET}}$ |
| 132     | L12          | MCLK                      |
| 133     | M1           | DGND                      |
| 134     | M2           | SCOMM[7]                  |
| 135     | M3           | SCOMM[6]                  |
| 136     | M4           | SCOMM[5]                  |
| 137     | M5           | DGND                      |
| 138     | M6           | DGND                      |
| 139     | M7           | DGND                      |
| 140     | M8           | DGND                      |
| 141     | M9           | TEST4                     |
| 142     | M10          | PLLVD                     |
| 143     | M11          | DGND                      |
| 144     | M12          | DGND                      |

# ADV202

## PIN FUNCTION DESCRIPTIONS

Table 16.

| Mnemonic   | Pins Used | 121-Pin Package                            | 144-Pin Package                            | I/O              | Description   |
|--|-----------|--|--|------------------|---|
| MCLK   | 1         | L9   | L12  | I                | System Input Clock. For details, see the PLL section. Maximum input frequency on MCLK is 74.25 MHz.   |
| RESET  | 1         | L7   | L11  | I                | Reset. Causes the ADV202 to immediately reset. $\overline{CS}$ , $\overline{RD}$ , $\overline{WE}$ , $\overline{DACK0}$ , $\overline{DACK1}$ , $\overline{DREQ0}$ , and $\overline{DREQ1}$ must be held high when a RESET is applied.   |
| HDATA<15:0>  | 16        | D4–D1, C5–C3, B5, B4, C2, B3–B1, A2, A6–A5 | F4, E1–E3, D1–D3, C1–C3, B1–B3, A2, A3, A4 | I/O              | Host Data Bus. With HDATA<23:16>, <27:24>, <31:28>, these pins make up the 32-bit wide host data bus. The async host interface is interfaced together with ADDR<3:0>, $\overline{CS}$ , $\overline{WE}$ , $\overline{RD}$ , and ACK. Unused HDATA pins should be pulled down via a 10 k $\Omega$ resistor.  |
| ADDR<3:0>  | 4         | H11, K8, H10, J9                           | J12, J11, J10, H12                         | I                | Address Bus for the Host Interface.   |
| $\overline{CS}$  | 1         | J8   | H11  | I                | Chip Select. This signal is used to qualify addressed read and write access to the ADV202 using the host interface.   |
| $\overline{WE}$<br>$\overline{RDFB}$                                     | 1         | J7   | H10  | I                | Write Enable Used with the Host Interface.<br>Read Enable when Fly-By DMA Is Enabled.<br>Note: Simultaneous assertion of $\overline{WE}$ and $\overline{DACK}$ low activates the HDATA bus, even if the DMA channels are disabled.  |
| $\overline{RD}$<br>$\overline{WEFB}$                                     | 1         | H9   | G12  | I                | Read Enable Used with the Host Interface.<br>Write Enable when Fly-By DMA Is Enabled.<br>Note: Simultaneous assertion of $\overline{RD}$ and $\overline{DACK}$ low activates the HDATA bus, even if the DMA channels are disabled.  |
| ACK  | 1         | H8   | G11  | O                | Acknowledge. Used for direct register accesses. This signal indicates that the last register access was successful.<br>Note: Due to synchronization issues, control and status register accesses might incur an additional delay, so the host software should wait for acknowledgment from the ADV202.<br>Accesses to the FIFOs (external DMA modes), on the other hand, are guaranteed to occur immediately, provided that space is available, and should not wait for $\overline{ACK}$ , provided that the timing constraints are observed.<br>If $\overline{ACK}$ is shared with more than one device, $\overline{ACK}$ should be connected to a pull-up resistor (10 k $\Omega$ ) and the PLL_HI register, Bit 4, must be set to 1. |
| IRQ  | 1         | G10  | G10  | O                | Interrupt. This pin indicates that the ADV202 requires the attention of the host processor. This pin can be programmed to indicate the status of the internal interrupt conditions within the ADV202. The interrupt sources are enabled via bits in register EIRQIE.  |
| $\overline{DREQ0}$<br>$\overline{FSRQ0}$<br>$\overline{VALID}$<br>CFG<1> | 1         | F8   | F12  | O<br>O<br>O<br>I | Data Request for external DMA Interface. Indicates that the ADV202 is ready to send/receive data to/from the FIFO assigned to DMA Channel 0.<br>Used in DCS-DMA Mode. Service request from the FIFO assigned to Channel 0 (asynchronous mode).<br>Valid Indication for JDATA Input/Output Stream. Polarity of this pin is programmable in the EDMOD0 register. VALID is always an output.<br>Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to IOVDD or DGND through a 10 k $\Omega$ resistor.  |
| $\overline{DACK0}$   | 1         | F9   | F11  | I                | Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request ( $\overline{DREQ0}$ ) has been acknowledged and data transfer can proceed. This pin must be held high at all times, if the DMA interface is not used, even if the DMA channels are disabled.   |

| Mnemonic                                   | Pins Used | 121-Pin Package   | 144-Pin Package                            | I/O               | Description   |
|--|-----------|---|--|-------------------|---|
| HOLD                                       |           |   |  | I                 | External Hold Indication for JDATA Input/Output Stream. Polarity is programmable in the EDMOD0 register. This pin is always an input.   |
| $\overline{\text{FCS0}}$                   |           |   |  | I                 | Used in DCS-DMA Mode. Chip select for the FIFO assigned to Channel 0 (asynchronous mode).   |
| $\overline{\text{DREQ1}}$                  | 1         | F10   | F10  | O                 | Data Request for External DMA Interface. Indicates that the ADV202 is ready to send/receive data to/from the FIFO assigned to DMA Channel 1.  |
| $\overline{\text{FSRQ1}}$                  |           |   |  | O                 | Used in DCS-DMA Mode. Service request from the FIFO assigned to Channel 1 (asynchronous mode).  |
| CFG<2>                                     |           |   |  | I                 | Boot Mode Configuration. This pin is read on reset to determine the boot configuration of the on-board processor. The pin should be tied to IOVDD or DGND through a 10 k $\Omega$ resistor.   |
| $\overline{\text{DACK1}}$                  | 1         | G9  | F9   | I                 | Data Acknowledge for External DMA Interface. Signal from the host CPU, which indicates that the data transfer request (DREQ1) has been acknowledged and data transfer can proceed. This pin must be held high at all times unless a DMA or JDATA access is occurring. This pin must be held high at all times, if the DMA interface is not used, even if the DMA channels are disabled. |
| $\overline{\text{FCS1}}$                   |           |   |  | I                 | Used in DCS-DMA Mode. Chip select for the FIFO assigned to Channel 1 (asynchronous mode).   |
| HDATA<31:28><br>JDATA<7:4>                 | 4         | J2–J4, H1   | K3, J1–J3                                  | I/O<br>I/O        | Host Expansion Bus.<br>JDATA Bus (JDATA Mode).  |
| HDATA<27:24><br>JDATA<3:0><br>VDATA<23:20> | 4         | H2–H4, G4   | J4, H1–H3                                  | I/O<br>I/O<br>I/O | Host Expansion Bus.<br>JDATA Bus (JDATA Mode).<br>Video Data Expansion Bus.   |
| HDATA<23:16><br>VDATA<19:12>               | 8         | G3, G2, F4, F3,<br>F2 E2, E3, E4                              | H4, G1–G4,<br>F1–F3                        | I/O<br>I/O        | Host Expansion Bus.<br>Video Data Expansion Bus. Extended pixel interface mode. Used for video formats that use Y and CrCb on separate buses.   |
| SCOMM<7><br>SCOMM<6><br>SCOMM<5>           | 8         | L2<br>L3<br>L4  | M2<br>M3<br>M4                             | I/O<br>I/O<br>I/O | When not used, this pin should be tied low.<br>When not used, this pin should be tied low.<br>This pin must be used in multiple chip mode to align the outputs of two or more ADV202s. For details, see the Applications section and the <i>ADV202 Multichip Application</i> application note. When not used, this pin should be tied low.  |
| SCOMM<4>                                   |           | K1  | L1   | O                 | LCODE Output in Encode Mode. When LCODE is enabled, the output on this pin indicates on a high transition that the last data-word for a field has been read from the FIFO. For an 8-bit interface, such as JDATA, LCODE is asserted for four consecutive bytes and is enabled by default.   |
| SCOMM<3>                                   |           | K2  | L2   | O                 | SPI interface: S_CSEL. When not used, this pin should be tied low. Used only with boot mode 6.  |
| SCOMM<2>                                   |           | L5  | L3   | O                 | SPI interface: S_MO. When not used, this pin should be tied low. Used only with boot mode 6.  |
| SCOMM<1>                                   |           | K4  | K1   | I                 | SPI interface: S_MI. When not used, this pin should be tied low. Used only with boot mode 6.  |
| SCOMM<0>                                   |           | K3  | K2   | O                 | SPI interface: S_CLK. When not used, this pin should be tied low. Used only with boot mode 6.   |
| VCLK                                       | 1         | E9  | E12  | I                 | Video Data Clock. Must be supplied, if video data is input/output on the VDATA bus.   |
| VDATA<11:0>                                | 12        | D11, D10, C7,<br>C9, C10, B7,<br>B8, B9, B11,<br>B10, A7, A10 | D10–D12,<br>C10–C12,<br>B10–B12,<br>A9–A11 | I/O               | Video Data. Unused pins should be pulled down via a 10 k $\Omega$ resistor.   |

# ADV202

| Mnemonic       | Pins Used | 121-Pin Package   | 144-Pin Package  | I/O      | Description  |
|----------------|-----------|---|--|----------|--|
| VSYNC<br>VFRM  | 1         | D8  | E10  | I/O      | Vertical Sync for Video Mode.<br>Raw Pixel Mode Framing Signal. Indicates first sample of a tile when asserted high. |
| HSYNC<br>VRDY  | 1         | D9  | E11  | I/O<br>O | Horizontal Sync for Video Mode.<br>Raw Pixel Mode Ready Signal.  |
| FIELD<br>VSTRB | 1         | E10   | E9   | I/O<br>I | Field Sync for Video Mode.<br>Raw Pixel Mode Transfer Strobe.  |
| TEST1          | 1         | J6  | K12  | I        | This pin should be connected to ground via a pull-down resistor.   |
| TEST2          | 1         | K9  | K11  | I        | This pin should be connected to ground via a pull-down resistor.   |
| TEST3          | 1         | J10   | K10  | I        | This pin should be connected to ground via a pull-down resistor.   |
| TEST4          | 1         | L6  | M9   | I        | This pin should be connected to ground via a pull-down resistor.   |
| TEST5          | 1         | K10   | L10  | O        | No connect.  |
| VDD            |           | A3, A8, D7, H7  | B6, B7, C6, C7, D6, D7, J6, J7, K6, K7, L6, L7   | V        | Positive Supply for Core.  |
| DGND           |           | A1, A11, A4, A9, C1, C11, D6, E1, E5–E7, E11, F1, F5–F7, F11, G1, G5–G7, G11, H6, J1, J11, K11, L1, L8, L11 | A1, A5–A8, A12, B5, B8, C5, C8, D5, D8, E4–E8, F5–F8, G5–G9, H5–H9, J5, J8–J9, K5, K8, L5, L8, M1, M5–M8, M11, M12 | GND      | Ground.  |
| PLLVDD         | 1         | L10   | M10  | V        | Positive Supply for PLL.   |
| IOVDD          |           | B6, C6, C8, D5, E8, G8, H5, J5, K5, K6, K7  | B4, B9, C4, C9, D4, D9, K4, K9, L4, L9   | V        | Positive Supply for I/O.   |



## THEORY OF OPERATION

The input video or pixel data is passed on to the ADV202's pixel interface, where samples are de-interleaved and passed on to the wavelet engine, where each tile or frame is decomposed into subbands using the 5/3 or 9/7 filters. The resultant wavelet coefficients are then written to internal memory. The entropy codecs then code the image data so that it conforms to the JPEG2000 standard. An internal DMA provides high bandwidth memory-to-memory transfers, as well as high performance transfers between functional blocks and memory.

### WAVELET ENGINE

The ADV202 provides a dedicated wavelet transform processor based on the Analog Devices proven and patented SURF™ technology. This processor can perform up to six wavelet decomposition levels on a tile. In encode mode, the wavelet transform processor takes in uncompressed samples, performs the wavelet transform and quantization, and writes the wavelet coefficients in all frequency subbands to internal memory. Each of these subbands is then further broken down into code blocks. The code-block dimensions can be user-defined, and are used by the wavelet transform processor to organize the wavelet coefficients into code blocks when writing to internal memory. Each completed code block is then entropy coded by one of the entropy codecs.

In decode mode, wavelet coefficients are read from internal memory and recomposed into uncompressed samples.

### ENTROPY CODECS

The entropy codec block performs context modeling and arithmetic coding on a code block of the wavelet coefficients. Additionally, this block also performs the distortion metric calculations during compression that are required for optimal rate and distortion performance. Because the entropy coding process is the most computationally intensive operation in the JPEG2000 compression process, three dedicated hardware entropy codecs are provided on the ADV202.

### EMBEDDED PROCESSOR SYSTEM

The ADV202 incorporates an embedded 32-bit RISC processor. This processor is used for configuration, control, and management of the dedicated hardware functions, as well as for parsing and generation of the JPEG2000 code stream. The processor system includes ROM and RAM for both program and data memory, an interrupt controller, standard bus interfaces, and other hardware functions such as timers and counters.

### MEMORY SYSTEM

The memory system's main function is to manage wavelet coefficient data, interim code-block attribute data, and temporary work space for creating, parsing, and storing the JPEG2000 code stream. The memory system can also be used for program and data memory for the embedded processor.

### INTERNAL DMA ENGINE

The internal DMA engine provides high bandwidth memory-to-memory transfers, as well as high performance transfers between memory and functional blocks. This function is critical for high speed generation and parsing of the code stream.

## ADV202 INTERFACE

There are several possible modes to interface to the ADV202 using the VDATA bus and the HDATA bus or the HDATA bus alone.

### VIDEO INTERFACE (VDATA BUS)

The video interface can be used in applications in which uncompressed pixel data is on a separate bus from compressed data. For example, it is possible to use the VDATA bus to input uncompressed video while using the HDATA bus to output the compressed data. This interface is ideal for applications requiring very high throughput such as live video capture.

Optionally, the ADV202 interlaces ITU.R-BT656 resolution video on the fly prior to wavelet processing, which yields significantly better compression performance for temporally coherent frame-based video sources. Additionally, high definition digital video such as SMPTE274M (1080i) is supported using two or more ADV202 devices.

The video interface can support video data or still image data input/output, 8-, 10-, and 12-bit single or multiplexed components, and dual-lane 8-, 10-, and 12-bit components. The VDATA interface supports digital video in YCbCr format in single input mode or Y and CbCr in dual-lane input mode. YCbCr data must be in 4:2:2 format.

Video data can be input/output in several different modes on the VDATA bus, as described in Table 17. In all these modes, the pixel clock must be input on the VCLK pin.

**Table 17. Video Input/Output Modes**

| Mode      | Description   |
|-----------|---|
| EAV/SAV   | Accepts video with embedded EAV/SAV codes, where the YCbCr data is interleaved onto a single bus.                         |
| HVF       | Accepts video data accompanied with separate H, V, and F signals where YCbCr data is interleaved onto a single bus.       |
| Extended  | Y and CrCb are on separate buses accompanied by EAV/SAV codes.  |
| Raw video | Used for still picture data and nonstandard video. VFRM, VSTRB, and VRDY are used to program the dimensions of the image. |
| HDTV      | For applications in which video data is clocked into the part at higher rates than 27 MHz.                                |

### HOST INTERFACE (HDATA BUS)

The ADV202 can connect directly to a wide variety of host processors and ASICs using an asynchronous SRAM-style interface, DMA accesses, or streaming mode (JDATA) interface. The ADV202 supports 16- and 32-bit buses for control and 8-, 16-, and 32-bit buses for data transfer.

The control and data channel bus widths can be specified independently, which allows the ADV202 to support applications that require control and data buses of different widths.

The host interface is used for configuration, control, and status functions, as well as for transferring compressed data streams. It can be used for uncompressed data transfers in certain modes. The host interface can be shared by as many as four concurrent data streams in addition to control and status communications. The data streams are

- Uncompressed tile data (for example, still image data)
- Fully encoded JPEG2000 code stream (or unpackaged code blocks)
- Code-block attributes
- Ancillary data

The ADV202 uses big endian byte alignment for 16- and 32-bit transfers. All data is left-justified (MSB).

### Pixel Input on the Host Interface

Pixel input on the host interface supports 8-, 10-, 12-, 14-, and 16-bit raw pixel data formats. It can be used for pixel (still image) input/output or compressed video output. Because there are no timing codes or sync signals associated with the input data on the host interface, dimension registers and internal counters are used and must be programmed to indicate the start and end of the frame. See the *ADV202 in HIPI Mode* technical note for details on how to use the ADV202 in this mode.

### Host Bus Configuration

For maximum flexibility, the host interface provides several configurations to meet particular system requirements. The default bus mode uses the same pins to transfer control, status, and data to and from the ADV202. In this mode, the ADV202 can support 16- and 32-bit control transfers and 8-, 16-, and 32-bit data transfers. The size of these buses can be selected independently, allowing, for example, a 16-bit microcontroller to configure and control the ADV202 while still providing 32-bit data transfers to an ASIC or external memory system.

### DIRECT AND INDIRECT REGISTERS

To minimize pin count and cost, the number of address pins has been limited to four, which yields a total direct address space of 16 locations. These locations are most commonly used by the external controller and are, therefore, accessible directly. All other registers in the ADV202 can be accessed indirectly through the IADDR and IDATA registers.

## CONTROL ACCESS REGISTERS

With the exception of the indirect address and data registers (IADDR and IDATA), all control/status registers in the ADV202 are 16 bits wide and are half-word (16-bit) addressable only. When 32-bit host mode is enabled, the upper 16 bits of the HDATA bus are ignored on writes and return all zeros on reads of 16-bit registers.

## PIN CONFIGURATION AND BUS SIZES/MODES

The ADV202 provides a wide variety of control and data configurations, which allows it to be used in many applications with little or no glue logic. The following modes are configured using the BUSMODE register. In the following descriptions, *host* refers to normal addressed accesses ( $\overline{\text{CS}}/\overline{\text{RD}}/\overline{\text{WR}}/\overline{\text{ADDR}}$ ) and *data* refers to external DMA accesses ( $\overline{\text{DREQ}}/\overline{\text{DACK}}$ ).

### 32-Bit Host/32-Bit Data

In this mode, the HDATA<31:0> pins provide full 32-bit wide data access to PIXEL, CODE, ATTR, and ANCL FIFOs. The expanded video interface (VDATA) is not available in this mode.

### 16-Bit Host/32-Bit Data

This mode allows a 16-bit host to configure and communicate with the ADV202 while still allowing 32-bit accesses to the PIXEL, CODE, ATTR, and ANCL FIFOs using the external DMA capability.

All addressed host accesses are 16 bits and, therefore, use only the HDATA<15:0> pins. The HDATA<31:16> pins provide the additional 16 bits necessary to support the 32-bit external DMA transfers to and from the FIFOs only. The expanded video interface (VDATA) is not available in this mode.

### 16-Bit Host/16-Bit Data

This mode uses 16-bit transfers, if used for host or external DMA data transfers. This mode allows for the use of the extended pixel interface modes.

### 16-Bit Host/8-Bit Data (JDATA Bus Mode)

This mode provides separate data input/output and host control interface pins. Host control accesses are 16 bits and use HDATA<15:0>, while the dedicated data bus uses JDATA<7:0>.

JDATA uses a valid/hold synchronous transfer protocol. The direction of the JDATA bus is determined by the mode of the ADV202. If the ADV202 is encoding (compression), then JDATA<7:0> is an output. If the ADV202 is decoding (decompression), then JDATA<7:0> is an input. Host control accesses remain asynchronous. See also JDATA section below.

## STAGE REGISTER

Because the ADV202 contains both 16-bit and 32-bit registers and its internal memory is mapped as 32-bit data, a mechanism

has been provided to allow 16-bit hosts to access these registers and memory locations using the stage register (STAGE). STAGE is accessed as a 16-bit register using HDATA[15:0]. Prior to writing to the desired register, the stage register must be written with the upper (most significant) half-word.

When the host subsequently writes the lower half-word to the desired control register, HDATA is combined with the previously staged value to create the required 32-bit value that is written. When a register is read, the upper (most significant) half-word is returned immediately on HDATA and the lower half-word can be retrieved by reading the stage register on a subsequent access. For details on using the stage register, see the *ADV202 User's Guide*.

Note: The stage register does not apply to the four data channels (PIXEL, CODE, ATTR, or ANCL). These channels are always accessed at the specified data width and do not require the use of the stage register.

## JDATA MODE

JDATA mode is typically used only when the dedicated video interface (VDATA) is also enabled. This mode allows code stream data (compressed data compliant with JPEG2000) to be input or output on a single dedicated 8-bit bus (JDATA<7:0>). The bus is always an output during compression operations, and is an input during decompression.

A 2-pin handshake is used to transfer data over this synchronous interface. VALID is used to indicate that the ADV202 is ready to provide or accept data and is always an output. HOLD is always an input and is asserted by the host if it cannot accept/provide data. For example, JDATA mode allows real-time applications, in which pixel data is input over the VDATA bus while the compressed data stream is output over the JDATA bus.

## EXTERNAL DMA ENGINE

The external DMA interface is provided to enable high bandwidth data I/O between an external DMA controller and the ADV202 data FIFOs. Two independent DMA channels can each be assigned to any one of the four data stream FIFOs (PIXEL, CODE, ATTR, or ANCL).

The controller supports asynchronous DMA using a Data-Request/Data-Acknowledge ( $\overline{\text{DREQ}}/\overline{\text{DACK}}$ ) protocol in either single or burst access modes. Additional functionality is provided for single address compatibility (fly-by) and dedicated chip select (DCS) modes.

## SPI PORT

The SPI port provides serial communication to and from the ADV202. The ADV202 is always the SPI master.

## INTERNAL REGISTERS

This section describes the internal registers of the ADV202.

### DIRECT REGISTERS

The ADV202 has 16 direct registers, as listed in Table 18. The direct registers are accessed over the  $\overline{\text{ADDR}}$  [3–0],  $\overline{\text{HDATA}}$ [31...0],  $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ , and  $\overline{\text{ACK}}$  pins.

The host must first initialize the direct registers before any application-specific operation can be implemented.

For additional information on accessing and configuring these registers, see the *ADV202 User's Guide*.

**Table 18. Direct Registers**

| Address | Name    | Description                            |
|---------|---------|--|
| 0x00    | PIXEL   | Pixel FIFO Access Register             |
| 0x01    | CODE    | Compressed Code Stream Access Register |
| 0x02    | ATTR    | Attribute FIFO Access Register         |
| 0x03    | ANCL    | Ancillary FIFO Access Register         |
| 0x04    | CMDSTA  | Command Stack                          |
| 0x05    | EIRQIE  | External Interrupt Enabled             |
| 0x06    | EIRQFLG | External Interrupt Flags               |
| 0x07    | SWFLAG  | Software Flag Register                 |
| 0x08    | BUSMODE | Bus Mode Configuration Register        |
| 0x09    | MMODE   | Miscellaneous Mode Register            |
| 0x0A    | STAGE   | Staging Register                       |
| 0x0B    | IADDR   | Indirect Address Register              |
| 0x0C    | IDATA   | Indirect Data Register                 |
| 0x0D    | BOOT    | Boot Mode Register                     |
| 0x0E    | PLL_HI  | PLL Control Register—High Byte         |
| 0x0F    | PLL_LO  | PLL Control Register—Low Byte          |

## INDIRECT REGISTERS

The indirect registers, listed in Table 19, are accessed by both the host system and the internal 32-bit embedded processor, via the ESF or the firmware.

In certain modes, such as custom-specific input format or HIPI mode, indirect registers must be accessed by the user through the use of the IADDR and IDATA registers. The indirect register address space starts at Internal Address 0xFFFF0000.

Both 32-bit and 16-bit hosts can access the indirect registers. 32-bit hosts use the IADDR and IDATA registers, while the 16 bit hosts use IADDR, IDATA, and the stage register.

For additional information on accessing and configuring these registers, see the *ADV202 User's Guide*.

**Table 19. Indirect Registers**

| Address                  | Name               | Description                          |
|--------------------------|--------------------|--------------------------------------|
| 0xFFFF0400               | PMODE1             | Pixel/Video Format                   |
| 0xFFFF0404               | COMP_CNT_STATUS    | Horizontal Count                     |
| 0xFFFF0408               | LINE_CNT_STATUS    | Vertical Count                       |
| 0xFFFF040C               | XTOT               | Total Samples per Line               |
| 0xFFFF0410               | YTOT               | Total Lines per Frame                |
| 0xFFFF0414               | F0_START           | Start Line of Field 0 [F0]           |
| 0xFFFF0418               | F1_START           | Start Line of Field 1 [F1]           |
| 0xFFFF041C               | V0_START           | Start of Active Video Field 0 [F0]   |
| 0xFFFF0420               | V1_START           | Start of Active Video Field 1 [F1]   |
| 0xFFFF0424               | V0_END             | End of Active Video Field 0 [F0]     |
| 0xFFFF0428               | V1_END             | End of Active Video Field 1 [F1]     |
| 0xFFFF042C               | PIXEL_START        | Horizontal Start of Active Video     |
| 0xFFFF0430               | PIXEL_END          | Horizontal End of Active Video       |
| 0xFFFF0440               | MS_CNT_DEL         | Master/Slave Delay                   |
| 0xFFFF0444               | LINE_CNT_INTERRUPT | Line Count Interrupt                 |
| 0xFFFF0448               | PMODE2             | Pixel Mode 2                         |
| 0xFFFF044C               | VMODE              | Video Mode                           |
| 0xFFFF1408               | EDMOD0             | External DMA Mode Register 0         |
| 0xFFFF140C               | EDMOD1             | External DMA Mode Register 1         |
| 0xFFFF1410               | FFTHRP             | FIFO Threshold for Pixel FIFO        |
| 0xFFFF1414               | FFCNTP             | FIFO Full/Empty Count for Pixel FIFO |
| 0xFFFF1418               | FFMODE             | FIFO Mode Register                   |
| 0xFFFF141C               | FFTHRC             | FIFO Threshold for Code FIFO         |
| 0xFFFF1420               | FFTHRA             | FIFO Threshold for ATTR FIFO         |
| 0xFFFF1424               | FFTHRN             | FIFO Threshold for ANCL FIFO         |
| 0xFFFF1428               | FFCNTC             | FIFO Full/ Empty Count for CODE FIFO |
| 0xFFFF142C               | FFCNTA             | FIFO Full/Empty Count for ATTR FIFO  |
| 0xFFFF1430               | FFCNTN             | FIFO Full/Empty Count for ANCL FIFO  |
| 0xFFFF1434 to 0xFFFF14FC | Reserved           | Reserved                             |

## PLL

The ADV202 uses the PLL\_HI and PLL\_LO direct registers to configure the PLL. Any time the PLL\_LO register is modified, the host must wait at least 20  $\mu$ s before reading or writing any other register. If this delay is not implemented, erratic behavior might result.

The PLL can be programmed to have any possible final multiplier value as long as

- JCLK > 50 MHz and < 150 MHz (144-pin version).
- JCLK > 50 MHz and < 135 MHz (144-pin version).
- JCLK > 50 MHz and < 115 MHz (121-pin version).
- HCLK < 115 MHz.
- $JCLK \geq 2 \times VCLK$  for single-component input.
- $JCLK \geq 2 \times VCLK$  for YCrCb [4:2:2] input.
- In JDATA mode (JDATA), JCLK must be  $4 \times MCLK$  or higher.

- The maximum burst frequency for external DMA modes is  $\leq 0.36$  JCLK.
- For MCLK frequencies greater than 50 MHz, the input clock divider must be enabled, that is, IPD set to 1.
- IPD cannot be enabled for MCLK frequencies below 20 MHz.

To achieve the lowest power consumption, an MCLK frequency of 27 MHz is recommended for a standard definition CCIR656 input. The PLL circuit is recommended to have a multiplier of 3. This sets JCLK and HCLK to 81 MHz.

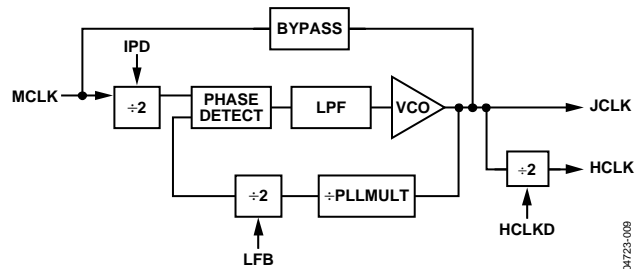


Figure 24. PLL Architecture and Control Functions

Table 20. Recommended PLL Register Settings

| IPD | LFB | PLLMULT | HCLKD | HCLK                     | JCLK                     |
|-----|-----|---------|-------|--------------------------|--------------------------|
| 0   | 0   | N       | 0     | $N \times MCLK$          | $N \times MCLK$          |
| 0   | 0   | N       | 1     | $N \times MCLK/2$        | $N \times MCLK$          |
| 0   | 1   | N       | 0     | $2 \times N \times MCLK$ | $2 \times N \times MCLK$ |
| 0   | 1   | N       | 1     | $N \times MCLK$          | $2 \times N \times MCLK$ |
| 1   | 0   | N       | 0     | $N \times MCLK/2$        | $N \times MCLK/2$        |
| 1   | 0   | N       | 1     | $N \times MCLK/4$        | $N \times MCLK/2$        |
| 1   | 1   | N       | 0     | $N \times MCLK$          | $N \times MCLK$          |
| 1   | 1   | N       | 1     | $N \times MCLK/2$        | $N \times MCLK$          |

Table 21. Recommended Values for PLL\_HI and PLL\_LO Registers

| Video Standard                         | CLKIN Frequency on MCLK | PLL_HI | PLL_LO |
|--|-------------------------|--------|--------|
| SMPTE125M or ITU-R.BT656 (NTSC or PAL) | 27 MHz                  | 0x0008 | 0x0004 |
| SMPTE293M (525p)                       | 27 MHz                  | 0x0008 | 0x0004 |
| ITU-R.BT1358 (625p)                    | 27 MHz                  | 0x0008 | 0x0004 |
| SMPTE274M (1080i)                      | 74.25 MHz               | 0x0008 | 0x0084 |

## HARDWARE BOOT

The boot mode can be configured via hardware using the CFG pins or via software (see the *ADV202 User's Guide*). The first boot mode after power-up is set by the CFG pins.

Only boot modes 2, 4, and 6, described in Table 22, are available via hardware.

**Table 22. Hardware Boot Modes**

| Boot Mode            | Settings                          | Description   |
|----------------------|-----------------------------------|---|
| Hardware Boot Mode 2 | CFG<1> tied high, CFG<2> tied low | No-Boot Host Mode. ADV202 does not boot, but all internal registers and memory are accessible through normal host I/O operations.<br>For details, see the <i>ADV202 User's Guide</i> and the <i>Getting Started with the ADV202</i> application note. |
| Hardware Boot Mode 4 | CFG<1> tied low, CFG<2> tied high | SoC boot mode. The embedded software framework (ESF) takes control and establishes communications with the host.  |
| Hardware Boot Mode 6 | CFG<1> and <2> tied high          | SPI boot mode. Boot firmware over SPI from external flash memory.   |

## VIDEO INPUT FORMATS

The ADV202 supports a wide variety of formats for uncompressed video and still image data. The actual interface and bus modes selected for transferring uncompressed data dictates the allowed size of the input data and the number of samples transferred with each access.

The host interface can support 8-, 10-, 12-, 14-, and 16-bit data formats. The video interface can support video data or still image data input/output. Supported formats are 8-, 10-, 12-, or 16-bit single or  $2 \times 8$ -bit,  $2 \times 10$ -bit,  $2 \times 12$ -bit multiplexed

formats. See the *ADV202 User's Guide* for details. All formats can support less precision than provided by specifying the actual data width/precision in the PMODE register.

The maximum allowable data input rate is limited by using irreversible or reversible compression modes and the data width (or precision) of the input samples. Use Table 23 and Table 24 to determine the maximum data input rate.

**Table 23. Maximum Pixel Data Input Rates**

| Interface              | Compression Mode | Input Format | Input Rate Limit Active Resolution (MSPS) <sup>1</sup> | Approx Min Peak Output Rate, Compressed Data <sup>2</sup> (Mbps) | Approx Max Output Rate, Compressed Data <sup>3</sup> (Mbps) |
|------------------------|------------------|--------------|--|--|---|
| <b>144-PIN PACKAGE</b> |                  |              |  |  |   |
| HDATA                  | Irreversible     | 8-bit data   | 45 [40]  | 130  | 200   |
|                        | Irreversible     | 10-bit data  | 45 [40]  | 130  | 200   |
|                        | Irreversible     | 12-bit data  | 45 [40]  | 130  | 200   |
|                        | Irreversible     | 16-bit data  | 45 [40]  | 130  | 200   |
|                        | Reversible       | 8-bit data   | 40 [36]  | 130  | 200   |
|                        | Reversible       | 10-bit data  | 32 [28]  | 130  | 200   |
|                        | Reversible       | 12-bit data  | 27 [24]  | 130  | 200   |
|                        | Reversible       | 14-bit data  | 23 [20]  | 130  | 200   |
| VDATA                  | Irreversible     | 8-bit data   | 65 [55]  | 130  | 200   |
|                        | Irreversible     | 10-bit data  | 65 [55]  | 130  | 200   |
|                        | Irreversible     | 12-bit data  | 65 [55]  | 130  | 200   |
|                        | Reversible       | 8-bit data   | 40 [34]  | 130  | 200   |
|                        | Reversible       | 10-bit data  | 32 [28]  | 130  | 200   |
|                        | Reversible       | 12-bit data  | 27 [23]  | 130  | 200   |
| <b>121-PIN PACKAGE</b> |                  |              |  |  |   |
| HDATA                  | Irreversible     | 8-bit data   | 34   | 98   | 150   |
|                        | Irreversible     | 10-bit data  | 34   | 98   | 150   |
|                        | Irreversible     | 12-bit data  | 34   | 98   | 150   |
|                        | Irreversible     | 16-bit data  | 34   | 98   | 150   |
|                        | Reversible       | 8-bit data   | 30   | 98   | 150   |
|                        | Reversible       | 10-bit data  | 24   | 98   | 150   |
|                        | Reversible       | 12-bit data  | 20   | 98   | 150   |
|                        | Reversible       | 14-bit data  | 17   | 98   | 150   |
| VDATA                  | Irreversible     | 8-bit data   | 48   | 98   | 150   |
|                        | Irreversible     | 10-bit data  | 48   | 98   | 150   |
|                        | Irreversible     | 12-bit data  | 48   | 98   | 150   |
|                        | Reversible       | 8-bit data   | 30   | 98   | 150   |
|                        | Reversible       | 10-bit data  | 24   | 98   | 150   |
|                        | Reversible       | 12-bit data  | 20   | 98   | 150   |

<sup>1</sup> Input rate limits for HDATA might be less for certain applications depending on input picture size and content, host interface settings, and DMA transfer settings. Values in brackets refer to the 135 MHz speed grade version of the ADV202.

<sup>2</sup> Minimum peak output rate or guaranteed sustained output rate.

<sup>3</sup> Maximum output rate, or output rate above this value is not possible.



Table 24. Maximum Supported Tile Width for Data Input on HDATA and VDATA Buses

| Compression Mode | Input Format     | Tile/Precinct Maximum Width |
|------------------|------------------|-----------------------------|
| 9/7i             | Single-component | 2048                        |
| 9/7i             | Two-component    | 1024 each                   |
| 9/7i             | Three-component  | 1024 (Y)                    |
| 5/3i             | Single-component | 4096                        |
| 5/3i             | Two-component    | 2048 (each)                 |
| 5/3i             | Three-component  | 2048 (Y)                    |
| 5/3r             | Single-component | 4096                        |
| 5/3r             | Two-component    | 2048                        |
| 5/3r             | Three-component  | 1024                        |

## APPLICATIONS

This section describes typical video applications for the ADV202 JPEG2000 video processor.

### ENCODE—MULTICHIP MODE

Due to the data input rate limitation (see Table 23), an 1080i application requires at least two ADV202s to encode or decode full-resolution 1080i video. In encode mode, the ADV202 accepts Y and CbCr data on separate buses. The input data must be in EAV/SAV format. An encode example is shown in Figure 25.

In decode mode, a master/slave configuration (as shown in Figure 26) or a slave/slave configuration can be used to synchronize the outputs of the two ADV202s. See the *ADV202 Multichip Application* application note for details on how to configure the ADV202s in a multichip application.

Applications that have two separate VDATA outputs sent to an FPGA or buffer before they are sent to an encoder do not require synchronization at the ADV202 outputs.

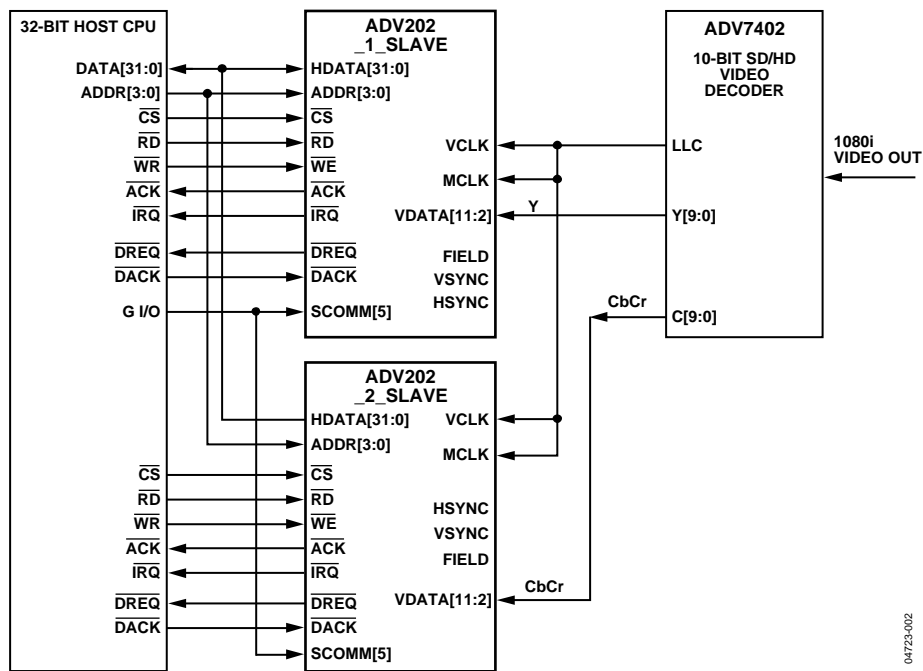


Figure 25. Encode—Multichip Application

04723-002

## DECODE—MULTICHIP MASTER/SLAVE

In a master/slave configuration, it is expected that the master HVF outputs are connected to the slave HVF inputs and that each SCOMM[5] pin is connected to the same GPIO on the host.

In a slave/slave configuration, the common HVF for both ADV202s is generated by an external house sync and each SCOMM[5] is connected to the same GPIO output on the host.

SWIRQ1, Software Interrupt 1 in the EIRQIE register, must be unmasked on both devices to enable multichip mode.

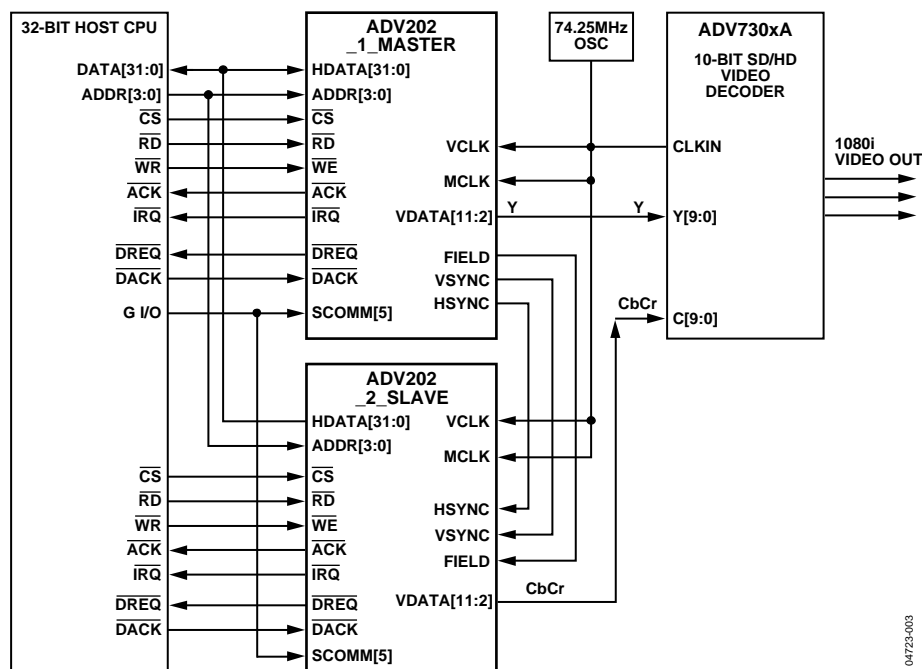


Figure 26. Decode—Multichip Master/Slave Application

## DIGITAL STILL CAMERA/CAMCORDER

Figure 27 is a typical configuration for a digital camera or camcorder.

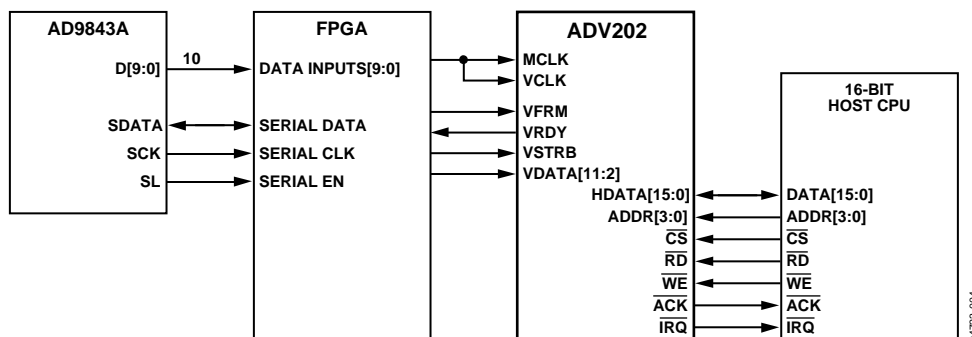
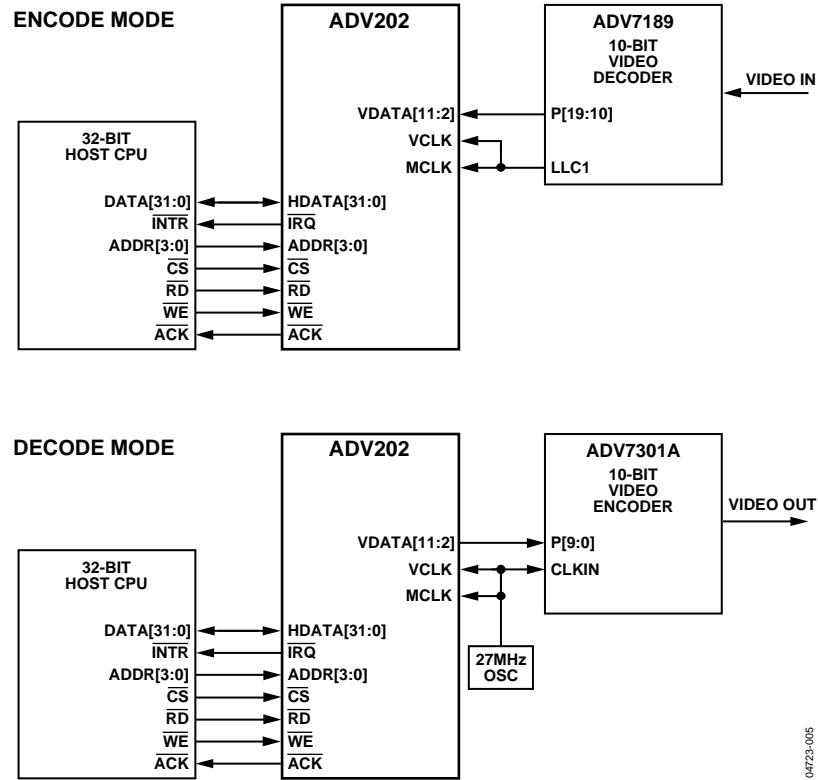


Figure 27. Digital Still Camera/Camcorder Application

# ADV202

## ENCODE/DECODE SDTV VIDEO APPLICATION

Figure 28 shows two ADV202 chips using 10-bit CCIR656 in normal host mode.



04723-005

Figure 28. Encode/Decode—SDTV Video Application

**ASIC APPLICATION (32-BIT HOST/32-BIT ASIC)**

Figure 29 shows two ADV202 chips using 10-bit CCIR656 in normal host mode.

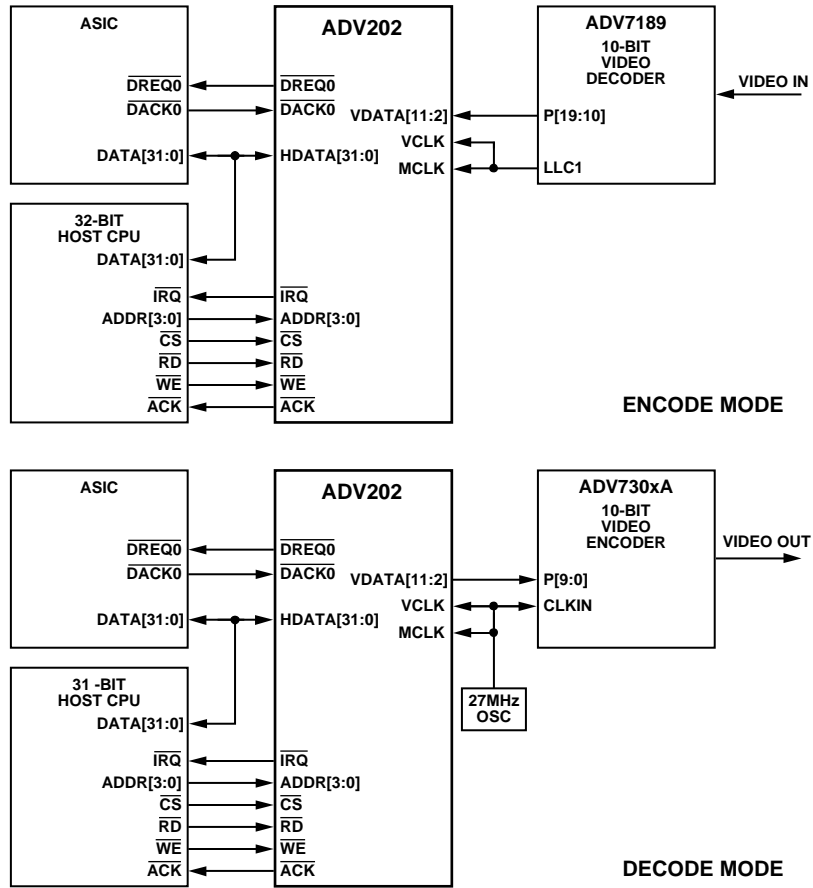


Figure 29. Encode/Decode ASIC Application

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# ADV202

## HIPI (HOST INTERFACE—PIXEL INTERFACE)

Figure 30 is a typical configuration using HIPI mode.

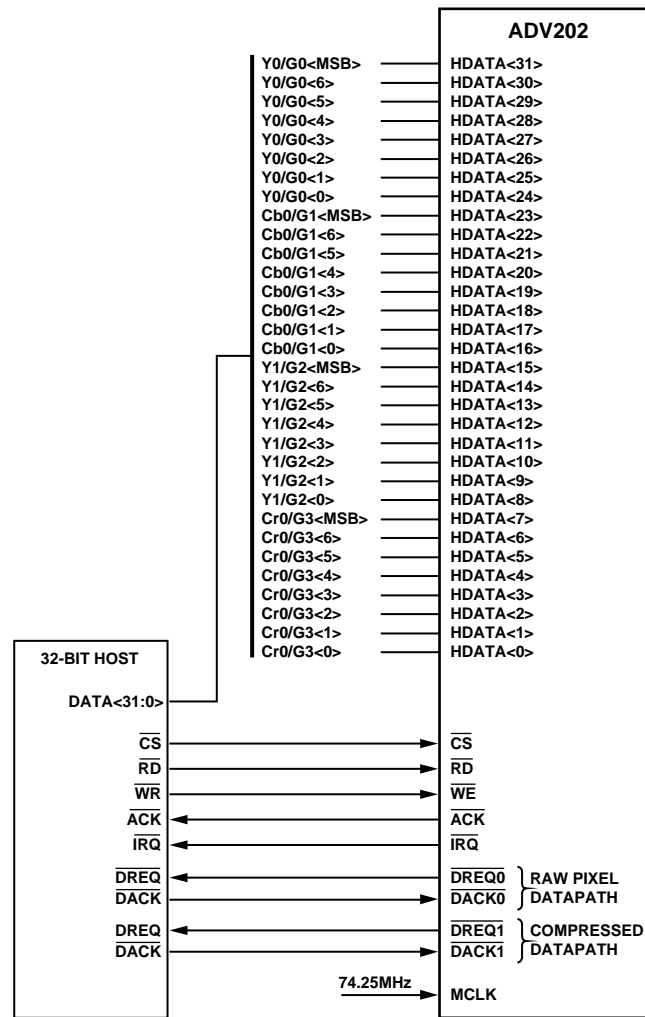


Figure 30. Host Interface—Pixel Interface mode

## JDATA INTERFACE

Figure 31 shows a typical configuration using JDATA with a dedicated JDATA output, 16-bit host, and 10-bit CCIR656.

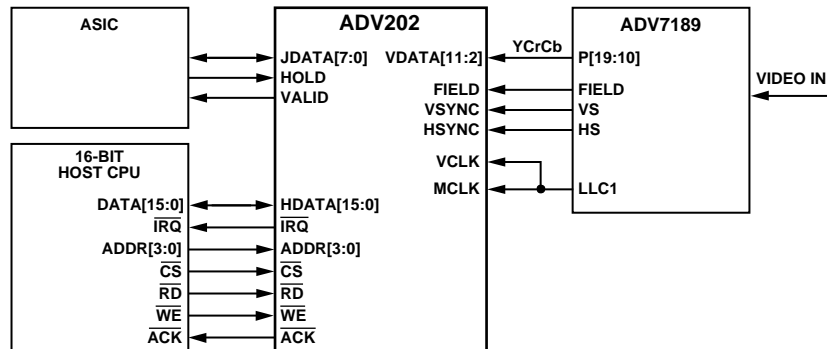
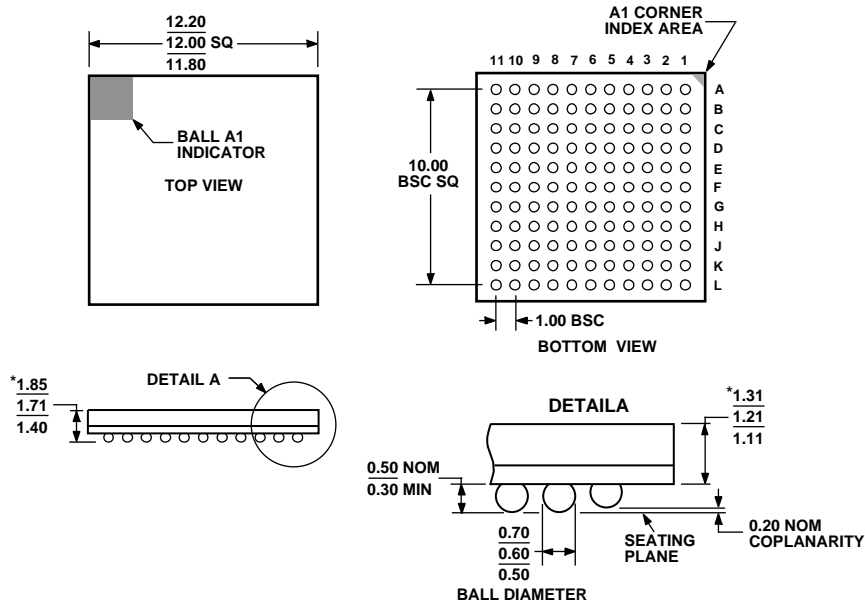


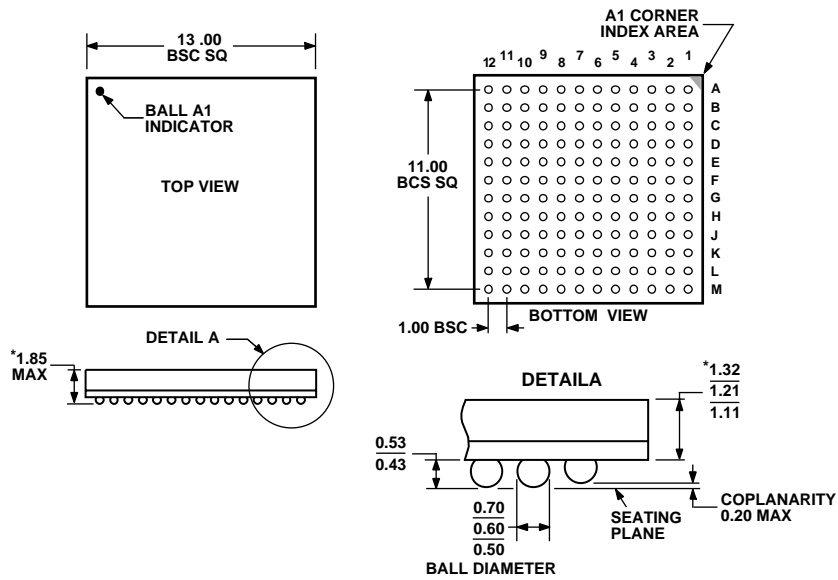
Figure 31. JDATA Application

# OUTLINE DIMENSIONS



\*COMPLIANT WITH JEDEC STANDARDS MO-192-ABD-1 WITH EXCEPTION TO PACKAGE HEIGHT AND PACKAGE THICKNESS.

Figure 32. 121-Lead Chip Scale Package Ball Grid Array [CSPBGA] (BC-121)  
Dimensions shown in millimeters



\*COMPLIANT WITH JEDEC STANDARDS MO-192-AAD-1 WITH EXCEPTION TO PACKAGE HEIGHT AND PACKAGE THICKNESS.

Figure 33. 144-Lead Chip Scale Package Ball Grid Array [CSPBGA] (BC-144-3)  
Dimensions shown in millimeters

# ADV202

## ORDERING GUIDE

| Model                       | Temperature Range | Speed Grade | Operating Voltage                  | Package Description                  | Package Option |
|-----------------------------|-------------------|-------------|------------------------------------|--------------------------------------|----------------|
| ADV202BBC-115               | -40°C to +85°C    | 115 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 121-Lead CSPBGA                      | BC-121         |
| ADV202BBCZ-115 <sup>1</sup> | -40°C to +85°C    | 115 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 121-Lead CSPBGA                      | BC-121         |
| ADV202BBC-135               | -40°C to +85°C    | 135 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 144-Lead CSPBGA                      | BC-144-3       |
| ADV202BBCZ-135 <sup>1</sup> | -40°C to +85°C    | 135 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 144-Lead CSPBGA                      | BC-144-3       |
| ADV202BBC-150               | -40°C to +85°C    | 150 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 144-Lead CSPBGA                      | BC-144-3       |
| ADV202BBCZ-150 <sup>1</sup> | -40°C to +85°C    | 150 MHz     | 1.5 V internal, 2.5 V or 3.3 V I/O | 144-Lead CSPBGA                      | BC-144-3       |
| ADV202-HD-EB                |                   |             |                                    | High Definition Evaluation Board     |                |
| ADV202-SD-EB                |                   |             |                                    | Standard Definition Evaluation Board |                |

<sup>1</sup> Z = Pb-free part.