Micro PMU with 0.8 A Buck, Two 300 mA LDOs Supervisory, Watchdog and Manual Reset

Data Sheet

ADP5042

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- One 0.8 A buck regulator
- Two 300 mA LDOs
- 20-lead, 4 mm × 4 mm LFCSP package
- Initial regulator accuracy: ±1%
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Open drain processor reset with threshold monitoring
- ±1.5% threshold accuracy over the full temperate range
- Guaranteed reset output valid to V_{CC} = 1 V
- Dual watchdog for secure systems
  - Watchdog 1 controls reset
  - Watchdog 2 controls reset and regulators power cycle
- Buck key specifications
  - Current mode topology for excellent transient response
  - 3 MHz operating frequency
  - Uses tiny multilayer inductors and capacitors
  - Mode pin selects forced PWM or auto PFM/PSM modes
  - 100% duty cycle low dropout mode
- LDOs key specifications
  - Low V_{IN} from 1.7 V to 5.5 V
  - Stable with1 µF ceramic output capacitors
  - High PSRR, 60 dB PSRR up to 1 kHz/10 kHz
  - Low output noise
    - 110 µV rms typical output noise at V_{OUT} = 2.8 V
  - Low dropout voltage: 150 mV at 300 mA load
  - –40°C to +125°C junction temperature range

HIGH LEVEL BLOCK DIAGRAM

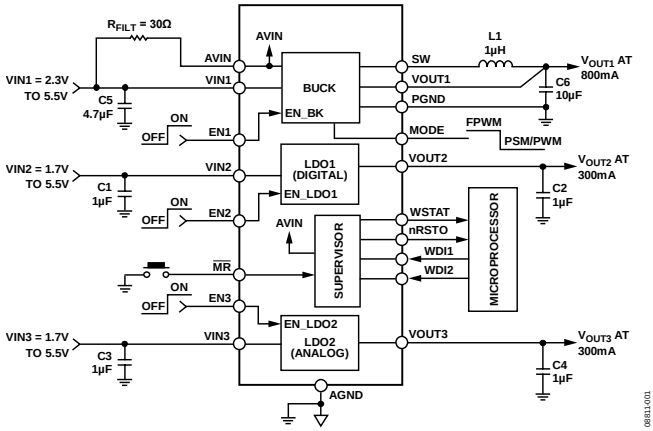

Figure 1.

GENERAL DESCRIPTION

The ADP5042 combines one high performance buck regulator and two low dropout regulators (LDO) in a small 20-lead LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulator enables use of tiny multilayer external components and minimizes the board space.

The MODE pin selects the buck mode of operation. When set to logic high, the buck regulators operate in forced PWM mode. When the MODE pin is set to logic low, the buck regulators operate in PWM mode when the load is around the nominal value. When the load current falls below a predefined threshold the regulator operates in power save mode (PSM) improving the light-load efficiency.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5042 LDOs extend the battery life of portable devices. The two LDOs maintain power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator is activated by a high level on the respective enable pin. The ADP5042 is available with factory programmable default output voltages and can be set to a wide range of options.

The ADP5042 contains supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. They also provide power-on reset signals. An on-chip dual watchdog timer can reset the microprocessor or power cycle the system (Watchdog 2) if it fails to strobe within a preset timeout period.

Rev. A

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12/10—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATION

AVIN, VIN1 = (V_{OUT1}+ 0.5 V) or 2.3 V, whichever is greater, AVIN, VIN1 ≥ VIN2, VIN3, T_A = 25°C, unless otherwise noted. Regulators are enabled.

Table 1.

Parameter	Symbol	Description	Min	Typ	Max	Unit
AVIN UNDERVOLTAGE LOCKOUT	$UVLO_{AVIN}$	T_J = −40°C to +125°C				
Input Voltage Rising	$UVLO_{AVINRISE}$				2.25	V
Input Voltage Falling	$UVLO_{AVINFALL}$		1.95			V
SHUTDOWN CURRENT	I_{GND-SD}	ENx = GND		0.1		µA
		ENx = GND, T_J = −40°C to +125°C			2	µA
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			20		°C
ENx, WDIx, MODE, WMOD, $\overline{MR}$ INPUTS						
Input Logic High	V_{IH}	2.5 V ≤ AVIN ≤ 5.5 V	1.2			V
Input Logic Low	V_{IL}	2.5 V ≤ AVIN ≤ 5.5 V			0.4	V
Input Leakage Current (WMOD Excluded)	$V_{I-LEAKAGE}$	ENx = AVIN or GND		0.05		µA
		ENx = AVIN or GND, T_J = −40°C to +125°C			1	µA
WMOD Input Leakage Current	$V_{I-LKG-WMOD}$	VWMOD = 3.6 V, T_J = −40°C to +125°C			50	µA
OPEN-DRAIN OUTPUTS						
nRSTO, WSTAT Output Voltage	V_{OL}	AVIN = 2.3 V to 5.5 V, $I_{nRSTO/WSTAT}$ = 3 mA		30		mV
Open-Drain Reset Output Leakage Current					1	µA

SUPERVISORY SPECIFICATION

AVIN, VIN1 = full operating range, T_J = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Supply Current (Supervisory Circuit Only)		45	55	µA	AVIN = 5.5 V, EN1 = EN2 = EN3 = VIN
		43	52	µA	AVIN = 3.6 V, EN1 = EN2 = EN3 = VIN
RESET THRESHOLD ACCURACY	VTH − 0.8%	VTH	VTH + 0.8%	V	T_A = 25°C, sensed on VOUTx
	VTH − 1.5%	VTH	VTH + 1.5%	V	T_J = −40°C to +125°C, sensed on V_{OUTx}
RESET THRESHOLD TO OUTPUT DELAY GLITCH IMMUNITY (t_{UOD})	50	125	400	µs	$V_{TH} = V_{UOT}$ − 50 mV
RESET TIMEOUT PERIOD WATCHDOG1 (t_{RP1})					
Option A	24	30	36	ms	
Option B	160	200	240	ms	
RESET TIMEOUT PERIOD WATCHDOG2 (t_{RP2})					
	3.5	5	7	ms	
V_{CC} TO RESET DELAY (t_{RD})		150		µs	VIN1 falling at 1 mV/µs
REGULATORS SEQUENCING DELAY (t_{D1}, t_{D2})		2		ms	
WATCHDOG INPUTS					
Watchdog 1 Timeout Period (t_{WD1})					
Option A	81.6	102	122.4	ms	
Option B	1.28	1.6	1.92	sec	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Watchdog 2 Timeout Period (t_{WD2})					
Option A	6	7.5	9	sec	
Option B		Watchdog 2 disabled			
Option C	3.2	4	4.8	min	
Option D	6.4	8	9.6	min	
Option E	11.2	16	19.2	min	
Option F	25.6	32	38.4	min	
Option G	51.2	64	76.8	min	
Option H	102.4	128	153.8	min	
Watchdog 2 Power Off Period (t_{POFF})					
Option A		210		ms	
Option B		400		ms	
WDI1 Pulse Width	80			ns	V_{IL} = 0.4 V, V_{IH} = 1.2 V
WDI2 Pulse Width	8			µs	V_{IL} = 0.4 V, V_{IH} = 1.2 V
Watchdog Status Timeout Period ($t_{WDCLEAR}$)		11.2		sec	
WDI1 Input Current (Source)	8	15	20	µA	$V_{WDI1} = V_{CC}$, time average
WDI1 Input Current (Sink)	−30	−25	−14	µA	V_{WDI1} = 0, time average
WDI2 Internal Pull-Down		45		kΩ	
MANUAL RESET INPUT					
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		220		ns	
$\overline{MR}$ Pull-Up Resistance	25	52	80	kΩ	
$\overline{MR}$ to Reset Delay		280		ns	V_{CC} = 5 V

BUCK SPECIFICATIONS

AVIN, VIN1 = 3.6 V, V_{OUT1} = 1.8 V, T_J= −40°C to +125°C for minimum/maximum specifications, L = 1 µH, C_{OUT} = 10 µF, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range (VIN1)		2.3		5.5	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy	PWM mode, T_A= 25 °C , I_{LOAD} = 100 mA	−1		+1	%
	PWM mode	−2		+2	%
	VIN1 = 2.3 V to 5.5 V, PWM mode, I_{LOAD} = 1 to 800 mA	−3		+3	%
PWM TO POWER SAVE MODE CURRENT THRESHOLD			100		mA
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	I_{LOAD} = 0 mA, device not switching		21	35	µA
Shutdown Current	ENx = 0 V, T_A = T_J = −40°C to +125°C		0.2	1.0	µA
SW CHARACTERISTICS					
SW On Resistance	PFET		180	240	mΩ
	PFET, AVIN = VIN1 = 5 V		140	190	mΩ
	NFET		170	235	mΩ
	NFET, AVIN = VIN1 = 5 V		150	210	mΩ
Current Limit	PFET switch peak current limit	1100	1360	1600	mA
ACTIVE PULL-DOWN	EN1 = 0 V		75		Ω
OSCILLATOR FREQUENCY		2.5	3.0	3.5	MHz
START-UP TIME			250		µs

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO1, LDO2 SPECIFICATIONS

AVIN = 3.6 V, V_{IN2}, V_{IN3} = (V_{OUT3} + 0.2 V) or 2.3 V, whichever is greater; AVIN, VIN1 ≥ VIN2, VIN3; I_{OUT} = 10 mA; C_{IN} = C_{OUT} = 1 µF; T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN2}, V_{IN3}	T_J = −40°C to +125°C	1.7		5.5	V
OPERATING SUPPLY CURRENT (per LDO)	I_{GND}	I_{OUT} = 0 µA, V_{OUT} = 3.3 V		15		µA
		I_{OUT} = 0 µA, V_{OUT} = 3.3 V, T_J = −40°C to +125°C			50	µA
		I_{OUT} = 10 mA		67		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			105	µA
		I_{OUT} = 200 mA		100		µA
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			245	µA
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT2}, V_{OUT3}	I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 300 mA	−2		+2	%
		V_{IN2}, V_{IN3} = (V_{OUT2}, V_{OUT3} + 0.5 V) to 5.5 V				
		100 µA < I_{OUT} < 300 mA	−3		+3	%
		V_{IN2}, V_{IN3} = (V_{OUT2}, V_{OUT3} + 0.5 V) to 5.5 V				
		T_J = −40°C to +125°C				
REGULATION						
Line Regulation	$\Delta V_{OUT2}/\Delta V_{IN2}$ $\Delta V_{OUT3}/\Delta V_{IN3}$	V_{IN2}, V_{IN3} = (V_{OUT2}, V_{OUT3} + 0.5 V) to 5.5 V	−0.03		+0.03	%/V
		I_{OUT3} = 1 mA				
		T_J = −40°C to +125°C				

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load Regulation[1]	$\Delta V_{OUT2}/\Delta I_{OUT2}$ $\Delta V_{OUT3}/\Delta I_{OUT3}$	I_{OUT2}, V_{OUT3} = 1 mA to 200 mA		0.002		%/mA
		I_{OUT2}, V_{OUT3} = 1 mA to 200 mA T_J = −40°C to +125°C			0.0075	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	V_{OUT2}, V_{OUT3} = 3.3 V				
		I_{OUT2}, I_{OUT3} = 10 mA		4		mV
		I_{OUT2}, I_{OUT3} = 10 mA, T_J = −40°C to +125°C			5	mV
		I_{OUT2}, I_{OUT3} = 200 mA		60		mV
		I_{OUT2}, I_{OUT3} = 200 mA, T_J = −40°C to +125°C			100	mV
ACTIVE PULL-DOWN	R_{PDLDO}	EN2/EN3 = 0 V		600		Ω
START-UP TIME	$T_{START-UP}$	V_{OUT2}, V_{OUT3} = 3.3 V		85		µs
CURRENT-LIMIT THRESHOLD[3]	I_{LIMIT}	T_J = −40°C to +125°C	335	470		mA
OUTPUT NOISE	$OUT_{LDO2NOISE}$	10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 3.3 V		123		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 2.8 V		110		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 1.5 V		59		µV rms
	$OUT_{LDO1NOISE}$	10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 3.3 V		140		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 2.8 V		129		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 1.5 V		66		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{IN2}, V_{IN3} = 3.3 V, $V_{OUT2, OUT3}$ = 2.8 V, I_{OUT} = 100 mA		66		dB
		100 kHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		57		dB
		1 MHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		60		dB

[1] Based on an end-point calculation using 1 mA and 100 mA loads.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.3 V.
[3] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM OUTPUT CAPACITANCE (BUCK)[1]	C_{MIN1}	T_J = −40°C to +125°C	7		40	µF
MINIMUM INPUT AND OUTPUT CAPACITANCE[2] (LDO1, LDO2)	C_{MIN23}	T_J = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_J = −40°C to +125°C	0.001		1	Ω

[1] The minimum output capacitance should be greater than 4.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met.
[2] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, Y5V and Z5U capacitors are not recommended for use with LDOs or the buck.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVIN, VINx, VOUTx, ENx, MODE, $\overline{MR}$, WDIx, WMOD, WSTAT, nRSTO to GND	−0.3 V to +6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	3000 V
ESD Charged Device Model	1500 V
ESD Machine Model	100 V

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP5042 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a four-layer, 4" × 3", 2.5 oz copper board, as per JEDEC standard. For additional information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale (LFCSP)*.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead, 0.5 mm pitch LFCSP	38	4.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

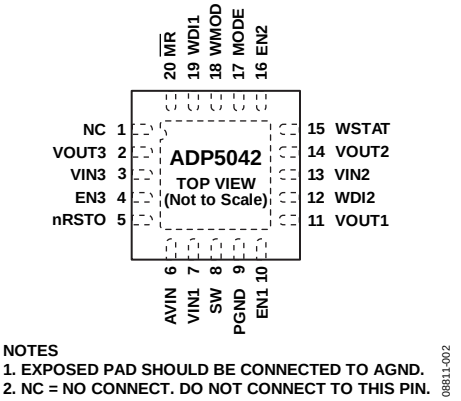

Figure 2. Pin Configuration—View from Top of the Die

Table 8. Preliminary Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	Do not connect to this pin.
2	VOUT3	LDO2 Output Voltage and Sensing Input.
3	VIN3	LDO2 Input Supply (1.7 V to 5.5 V).
4	EN3	Enable LDO2. EN3 = high: turn on LDO2; EN3 = low: turn off LDO2.
5	nRSTO	Open-Drain Reset Output, Active Low.
6	AVIN	Regulators Housekeeping and Supervisory Input Supply (2.3 V to 5.5 V).
7	VIN1	Buck Input Supply (2.3 V to 5.5 V).
8	SW	Buck Switching Node.
9	PGND	Dedicated Power Ground for Buck Regulator.
10	EN1	Enable Buck. EN1 = high: turn on buck; EN1 = low: turn off buck.
11	VOUT1	Buck Sensing Node.
12	WDI2	Watchdog 2 (Long Timeout) Refresh Input from Processor. Can be disabled only by factory option.
13	VIN2	LDO1 Input Supply (1.7 V to 5.5 V).
14	VOUT2	LDO1 Output Voltage and Sensing Input.
15	WSTAT	Open-Drain Watchdog Timeout Status. WSTAT = high: Watchdog 1 timeout or power-on reset; WSTAT = low: Watchdog 2 timeout. Auto cleared after one second.
16	EN2	Enable LDO1. EN2 = high: turn on LDO1. EN2 = low: turn off LDO1.
17	MODE	Buck Mode. MODE = high: buck regulator operates in fixed PWM mode; MODE = low: buck regulator operates in pulse skipping mode (PSM) at light load and in constant PWM at higher load.
18	WMOD	Watchdog Mode. WMOD = low: Watchdog 1 normal mode; WMOD = high: Watchdog 1 cannot be disabled by a three-state condition applied on WDI1.
19	WDI1	Watchdog 1 Refresh Input from Processor. If WDI1 is in high-Z and WMOD is low, Watchdog 1 is disabled.
20	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
TP	AGND	Analog Ground (TP = Thermal Pad). Exposed pad should be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = VIN3 = AVIN = 5.0 V, T_A = 25°C, unless otherwise noted.

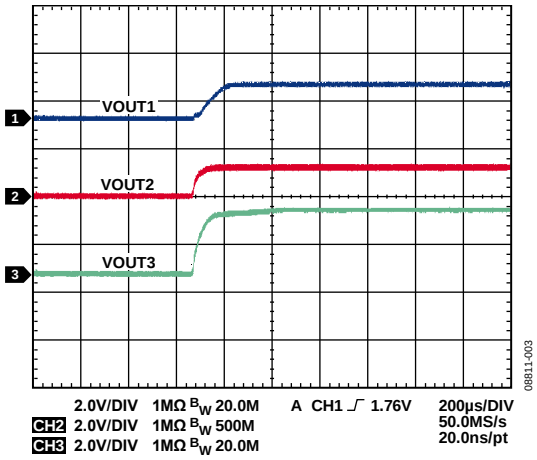

Figure 3. 3-Channel Start-Up Waveforms

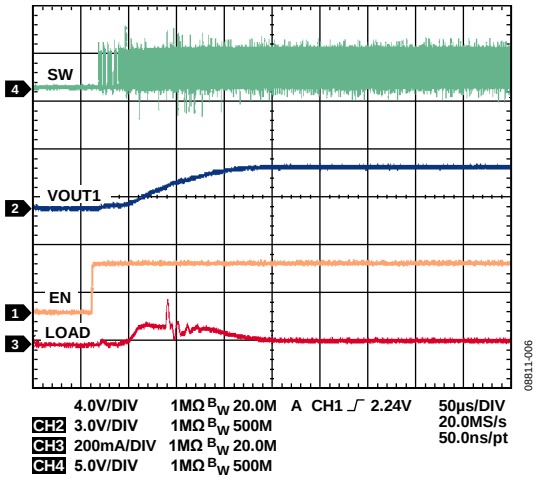

Figure 6. Buck Startup, VOUT1 = 1.8 V, I_{OUT2} = 20 mA

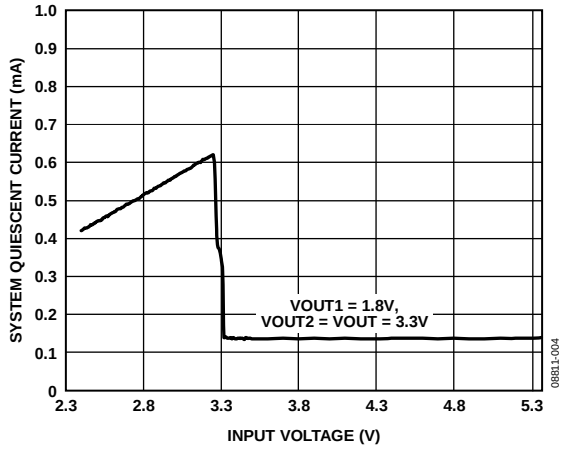

Figure 4. System Quiescent Current (Sum of All the Input Currents) vs. Input Voltage, VOUT1 = 1.8 V, VOUT2 = VOUT3 = 3.3 V

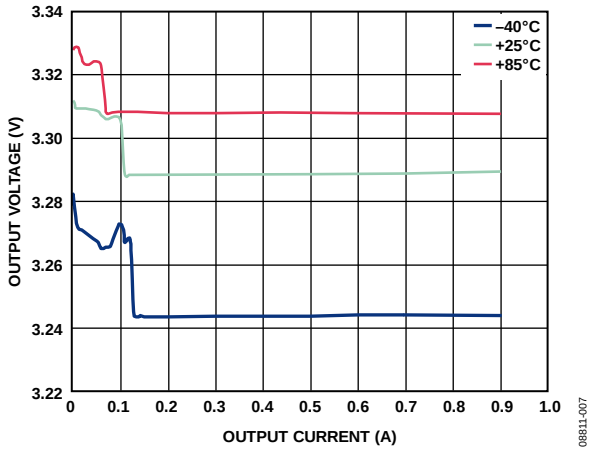

Figure 7. Buck Load Regulation Across Temperature, VOUT1 = 3.3 V, Auto Mode

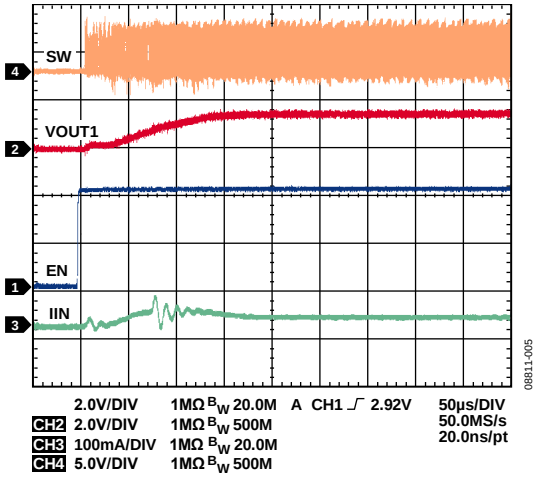

Figure 5. Buck Startup, VOUT1 = 1.8 V, I_{OUT1} = 20 mA

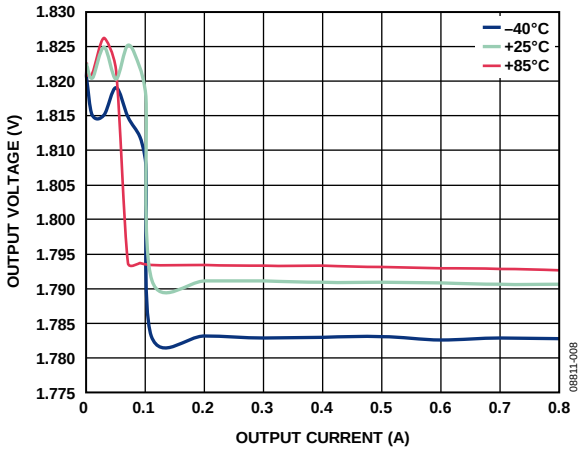

Figure 8. Buck Load Regulation Across Temperature, VOUT1 = 1.8 V, Auto Mode

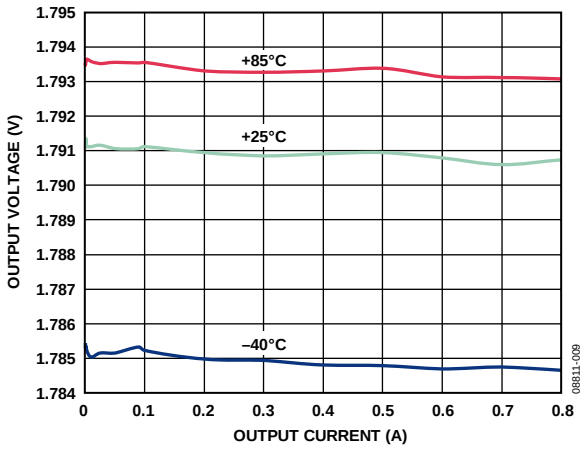

Figure 9. Buck Load Regulation Across Temperature, VOUT1 = 1.8 V, PWM Mode

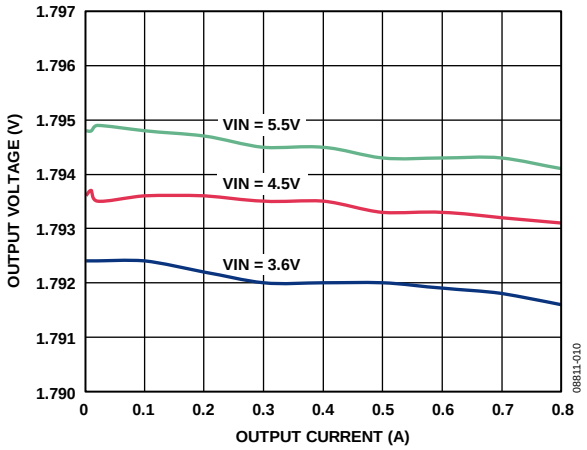

Figure 10. Buck Load Regulation Across Input Voltage, VOUT1 = 1.8 V, PWM Mode

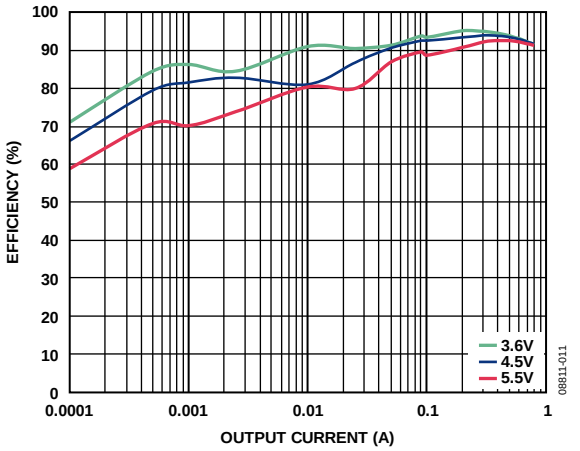

Figure 11. Buck Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 3.3 V, Auto Mode

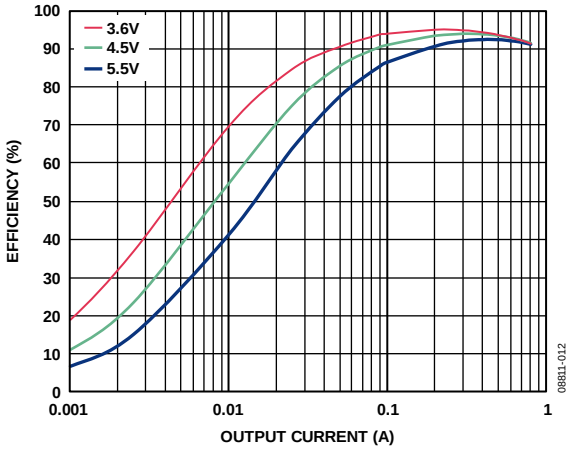

Figure 12. Buck Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 3.3 V, PWM Mode

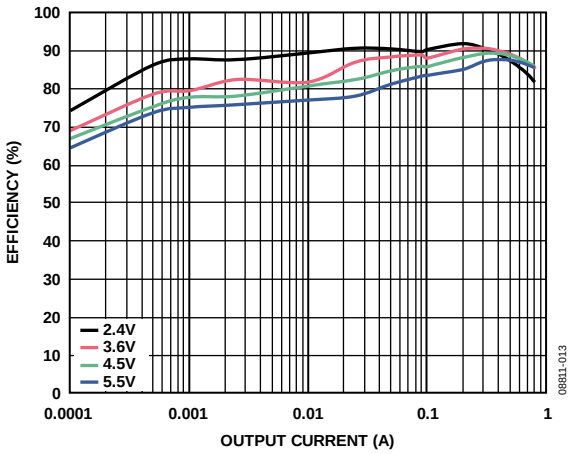

Figure 13. Buck Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 1.8 V, Auto Mode

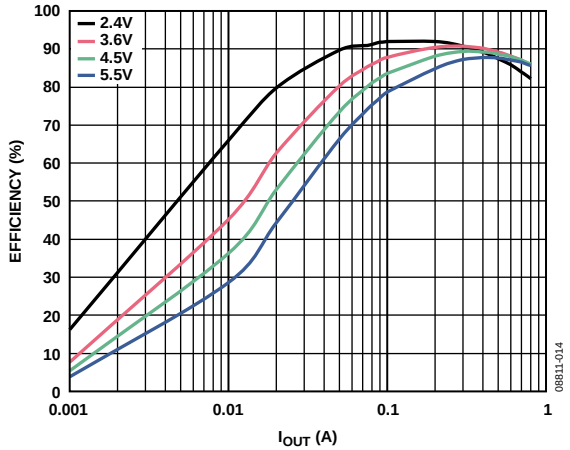

Figure 14. Buck Efficiency vs. Load Current, Across Input Voltage, VOUT2 = 1.8 V, PWM Mode

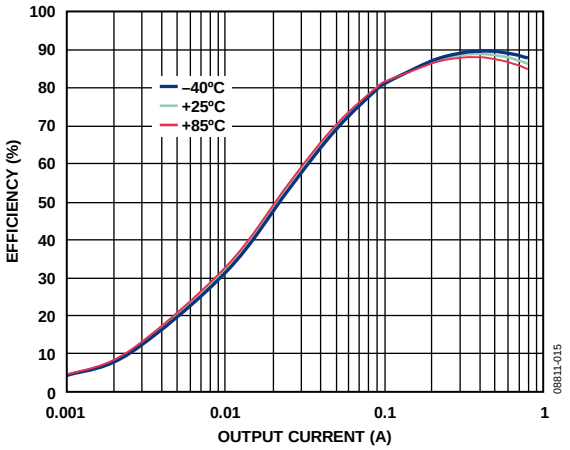

Figure 15. Buck Efficiency vs. Load Current, Across Temperature, VOUT1 = 1.8 V, PWM Mode

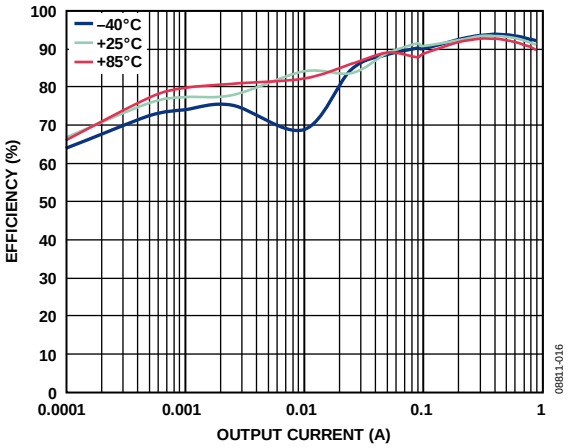

Figure 16. Buck Efficiency vs. Load Current, Across Temperature, VOUT1 = 3.3 V, Auto Mode

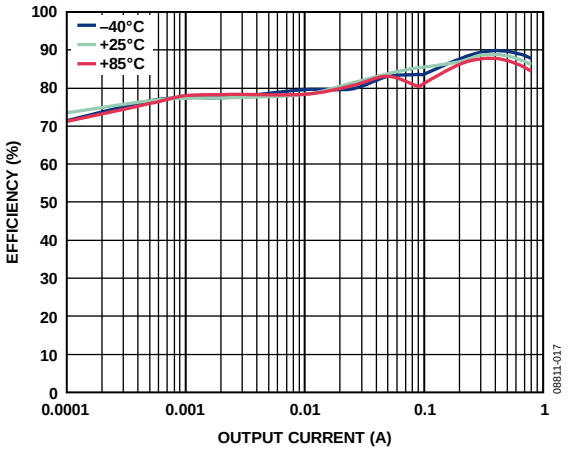

Figure 17. Buck Efficiency vs. Load Current, Across Temperature, VOUT1 = 1.8 V, Auto Mode

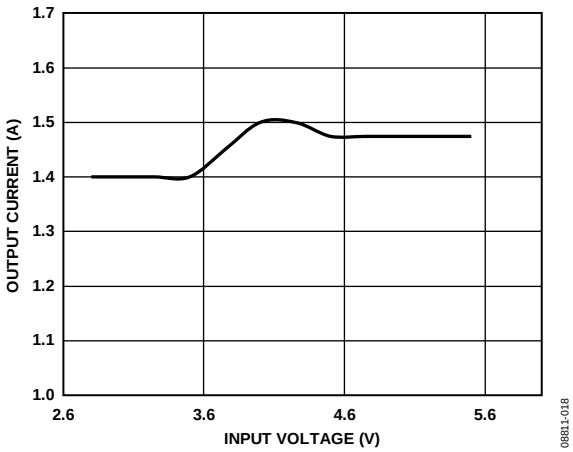

Figure 18. Buck DC Current Capability vs. Input Voltage, VOUT1 = 1.8 V

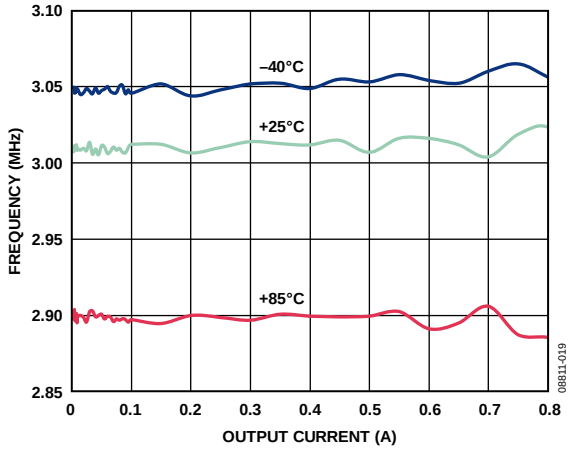

Figure 19. Buck Switching Frequency vs. Output Current, Across Temperature, VOUT1 = 1.8 V, PWM Mode

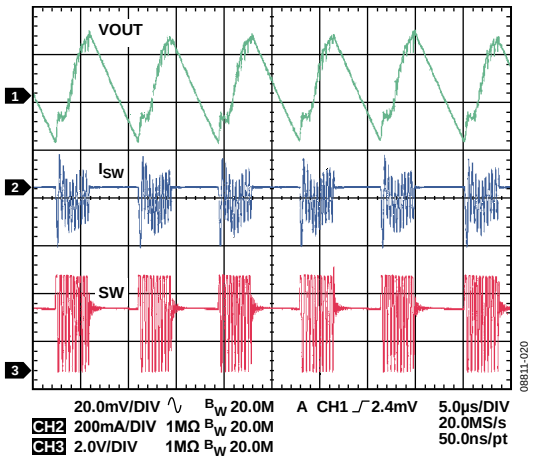

Figure 20. Typical Waveforms, VOUT1 = 3.3 V, I_{OUT1} = 30 mA, Auto Mode

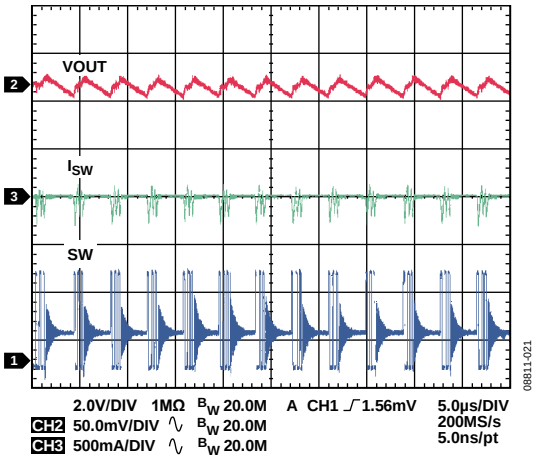

Figure 21. Typical Waveforms, VOUT1 = 1.8 V, IOUT2 = 30 mA, Auto Mode

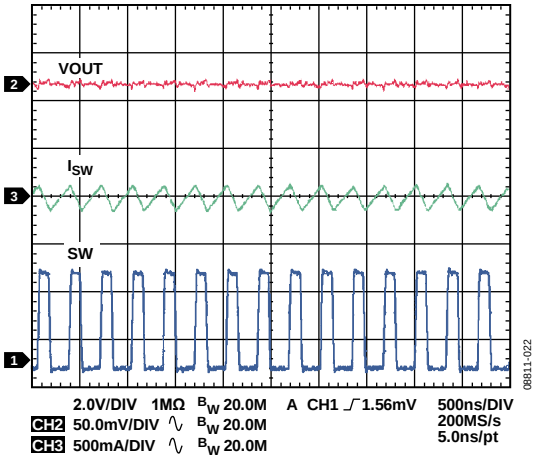

Figure 22. Typical Waveforms, VOUT1 = 1.8 V, IOUT1 = 30 mA, PWM Mode

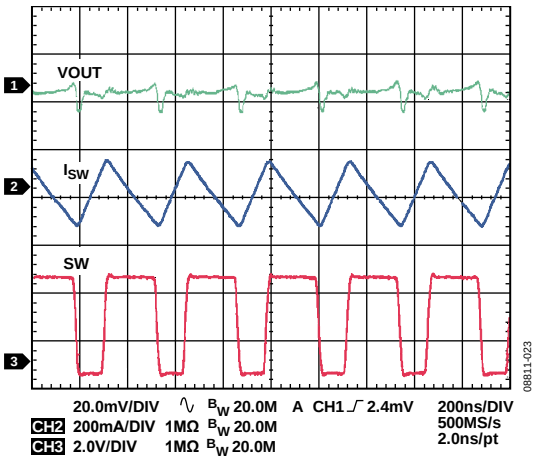

Figure 23. Typical Waveforms, VOUT1 = 3.3 V, IOUT2 = 30 mA, PWM Mode

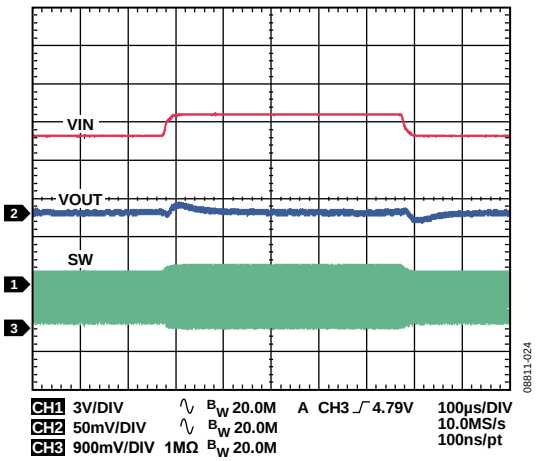

Figure 24. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, VOUT1 = 3.3 V, PWM Mode

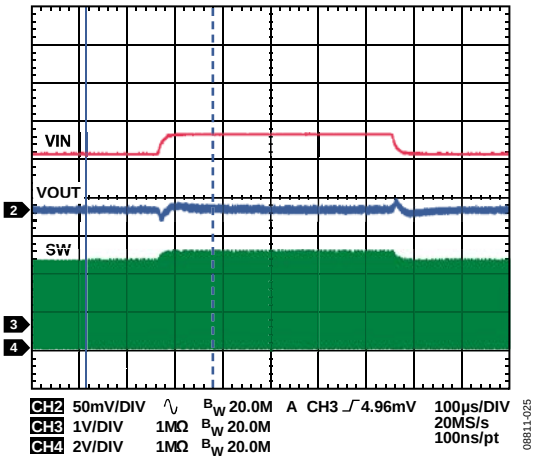

Figure 25. Buck Response to Line Transient, V_{IN} = 4.5 V to 5.0 V, VOUT1 = 1.8 V, PWM Mode

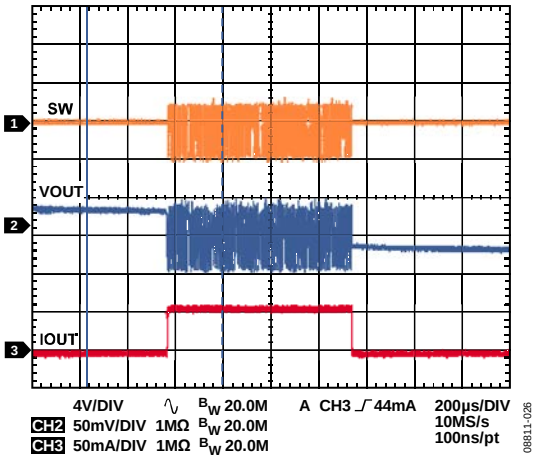

Figure 26. Buck Response to Load Transient, IOUT1 from 1 mA to 50 mA, VOUT1 = 3.3 V, Auto Mode

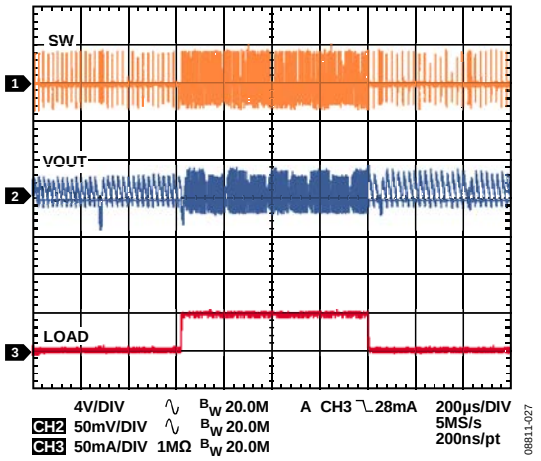

Figure 27. Buck Response to Load Transient, IOUT2 from 1 mA to 50 mA, VOUT2 = 1.8 V, Auto Mode

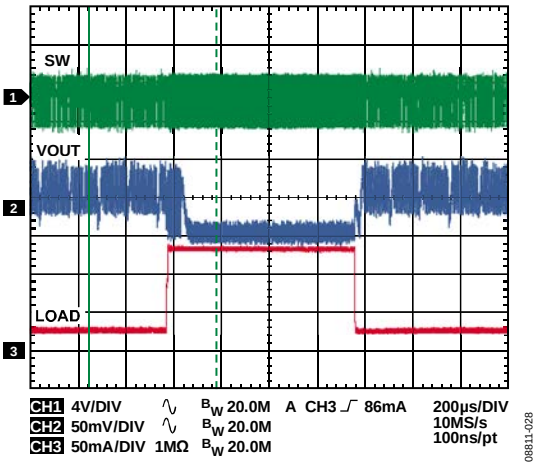

Figure 28. Buck Response to Load Transient, IOUT1 from 20 mA to 140 mA, VOUT1 = 3.3 V, Auto Mode

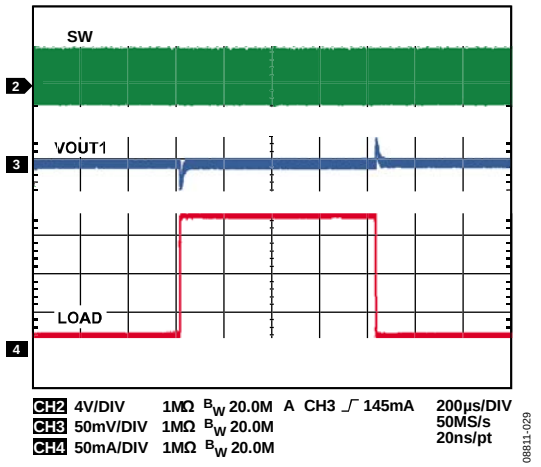

Figure 29. Buck Response to Load Transient, IOUT2 from 20 mA to 180 mA, VOUT1 = 1.8 V, PWM Mode

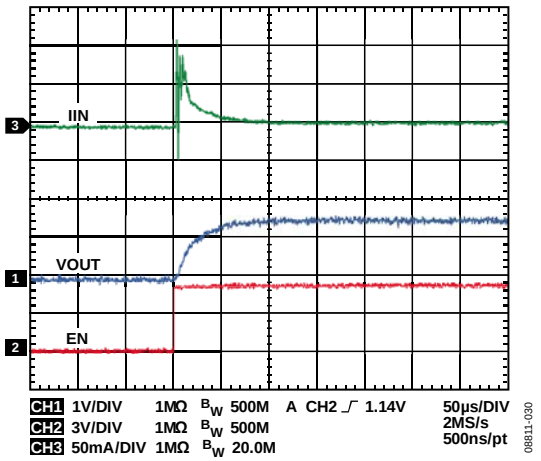

Figure 30. LDO1 Startup, VOUT3=1.5 V, IOUT3 = 5 mA

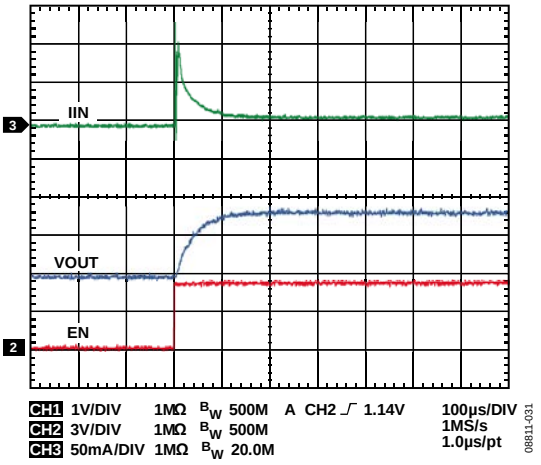

Figure 31. LDO2 Startup, VOUT3=3.3 V, IOUT3 = 5 mA

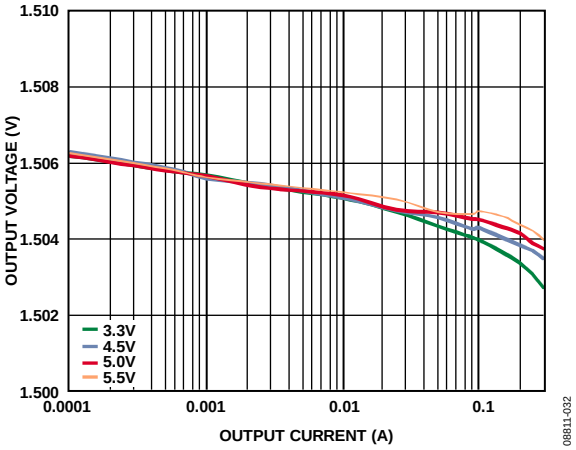

Figure 32. LDO1 Load Regulation Across Input Voltage, VOUT2 = 1.5 V

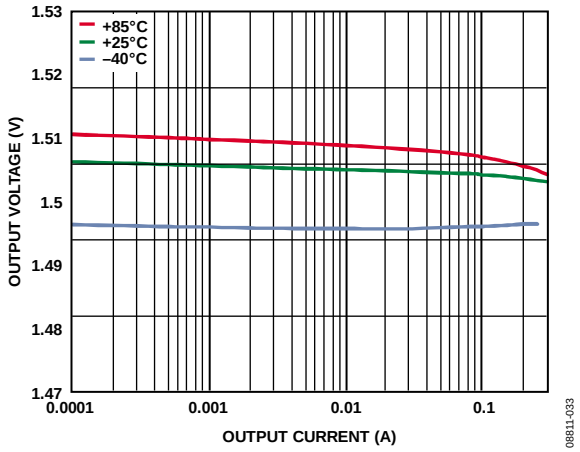

Figure 33. LDO1 Load Regulation Across Temperature, VIN2 = 3.3 V, VOUT2 = 1.5 V

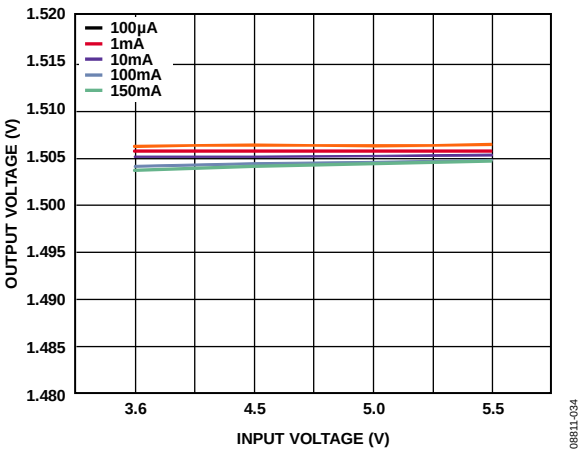

Figure 34. LDO1 Line Regulation Across Output Load, VOUT2 = 1.5 V

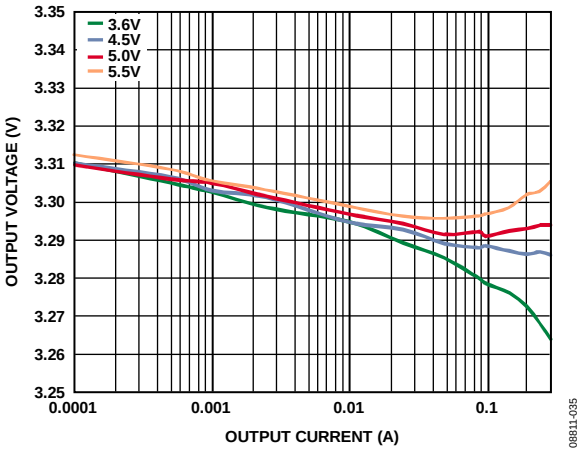

Figure 35. LDO2 Load Regulation Across Input Voltage, VOUT3 = 3.3 V

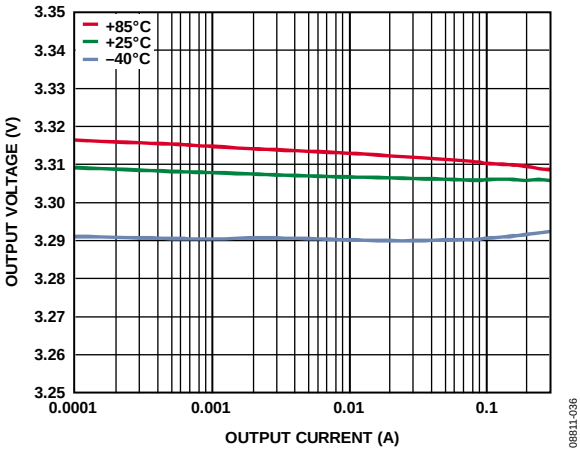

Figure 36. LDO2 Load Regulation Across Temperature, VIN3 = 3.6 V, VOUT3 = 3.3 V

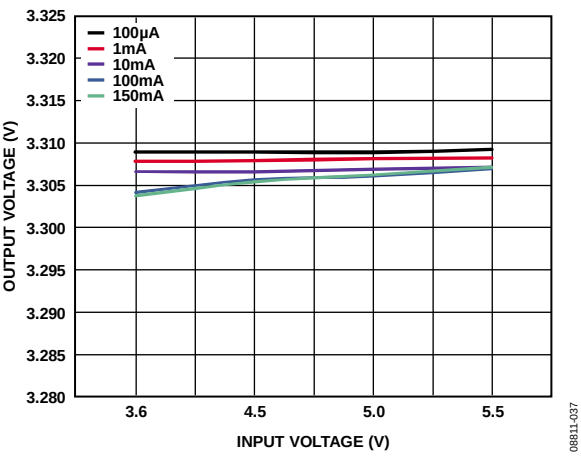

Figure 37. LDO2 Line Regulation Across Output Load, VOUT3 = 3.3 V

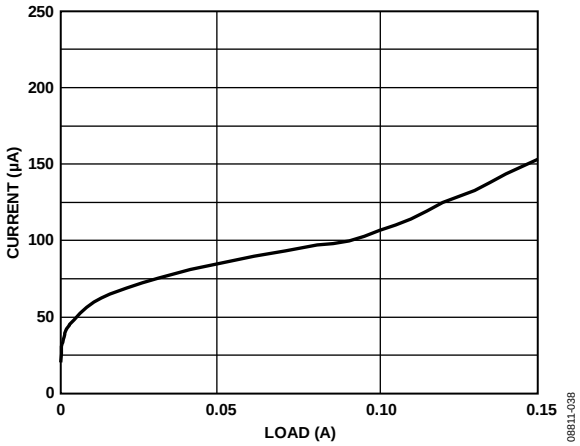

Figure 38. LDO2 Ground Current vs. Output Load, VOUT3 = 2.8 V

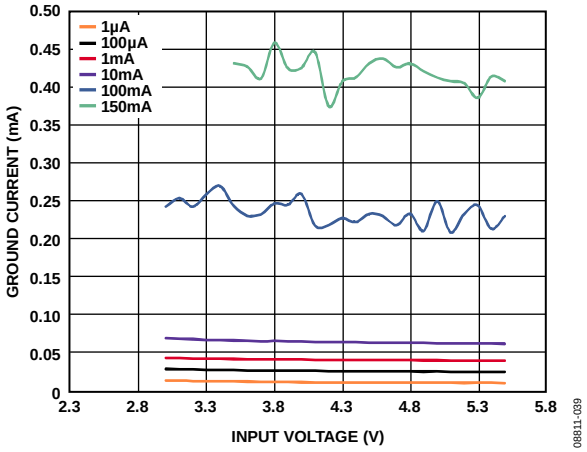

Figure 39. LDO2 Ground Current vs. Input Voltage, Across Output Load, VOUT3 = 2.8 V

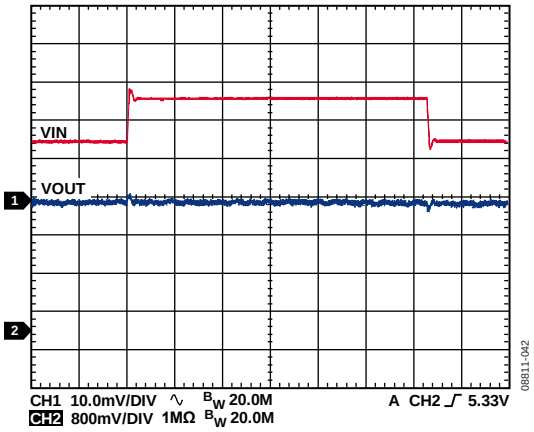

Figure 42. LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, VOUT3 = 3.3 V

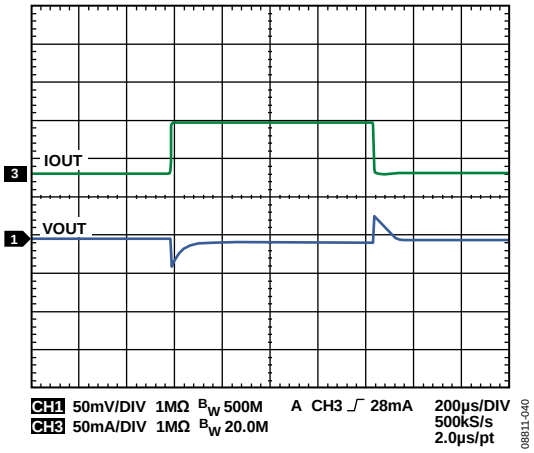

Figure 40. LDO2 Response to Load Transient, IOUT3 from 1 mA to 80 mA, VOUT3 = 3.3 V

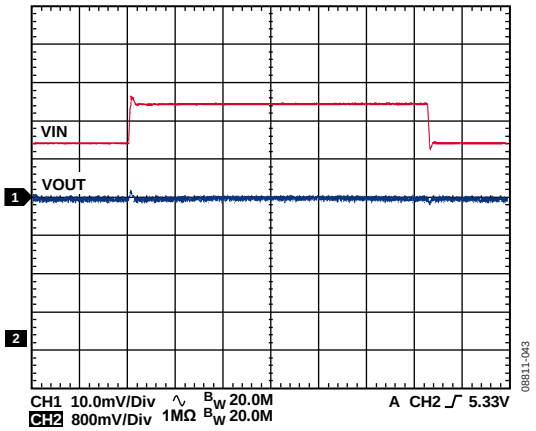

Figure 43. LDO1 Line Transient VIN = 4.5 V to 5.5 V, VOUT2 = 1.5 V

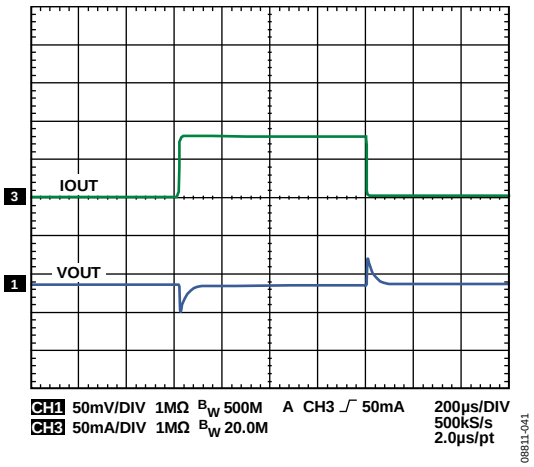

Figure 41. LDO1 Response to Load Transient, IOUT3 from 1 mA to 80 mA, VOUT2 = 1.5 V

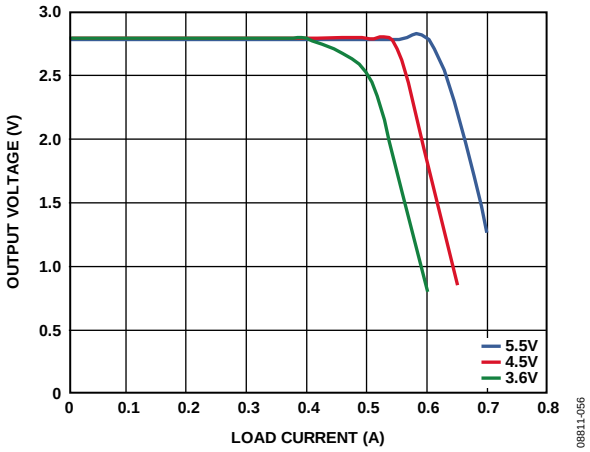

Figure 44. LDO1, LDO2 Output Current Capability vs. Input Voltage

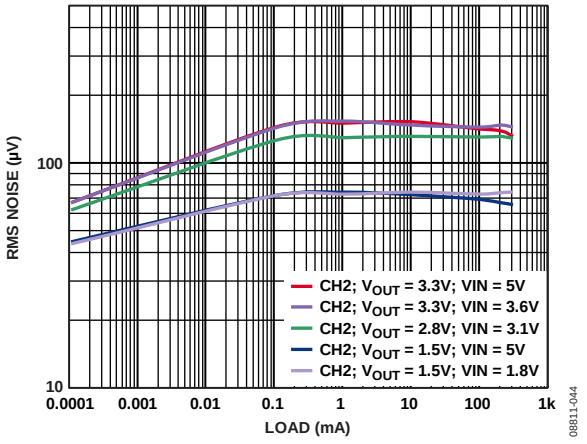

Figure 45. LDO1 Output Noise vs. Load Current, Across Input and Output Voltage

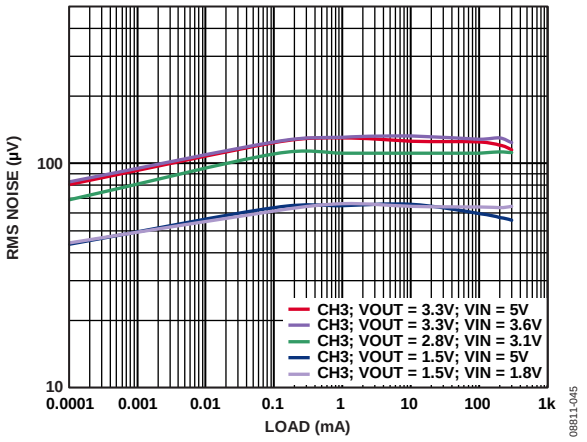

Figure 46. LDO2 Output Noise vs. Load Current, Across Input and Output Voltage

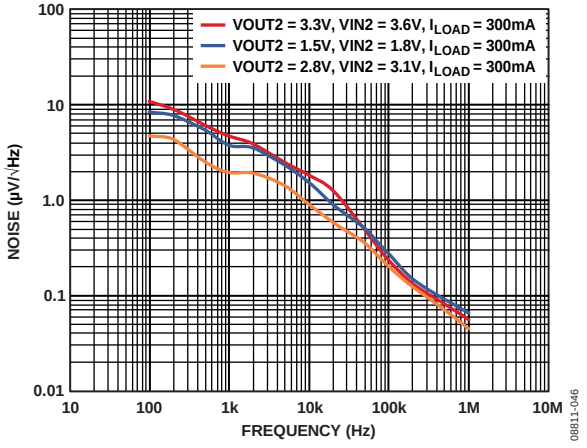

Figure 47. LDO1 Noise Spectrum Across Output Voltage, VIN = VOUT + 0.3 V

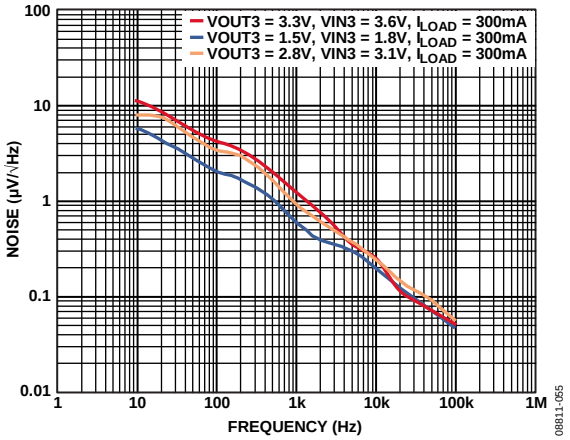

Figure 48. LDO2 Noise Spectrum Across Output Voltage, VIN = VOUT + 0.3 V

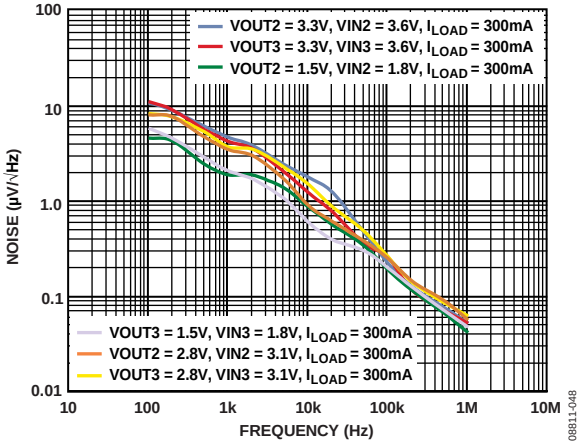

Figure 49. LDO1 vs. LDO2 Noise spectrum

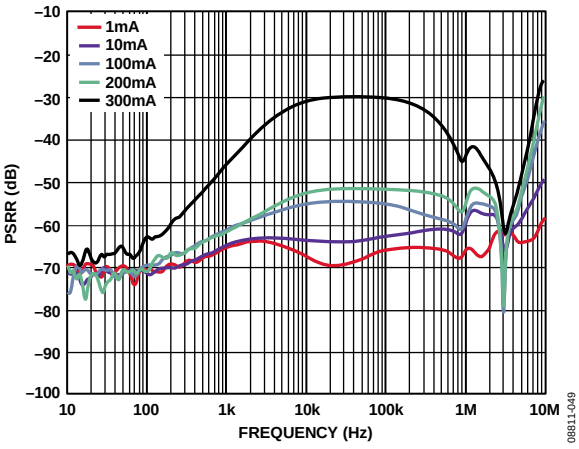

Figure 50. LDO2 PSRR Across Output Load, VIN3 = 3.3 V, VOUT3 = 2.8 V

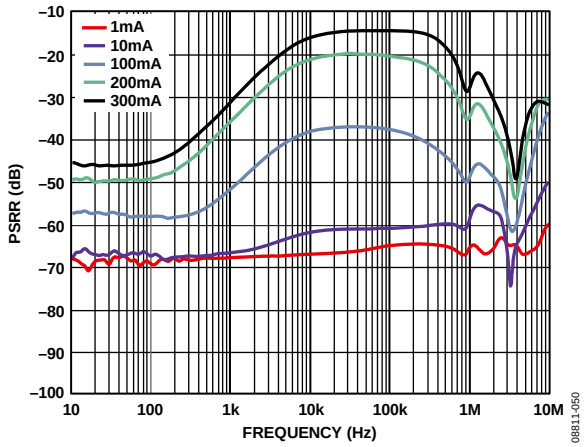

Figure 51. LDO2 PSRR Across Output Load, VIN3 = 3.1 V, VOUT3 = 2.8 V

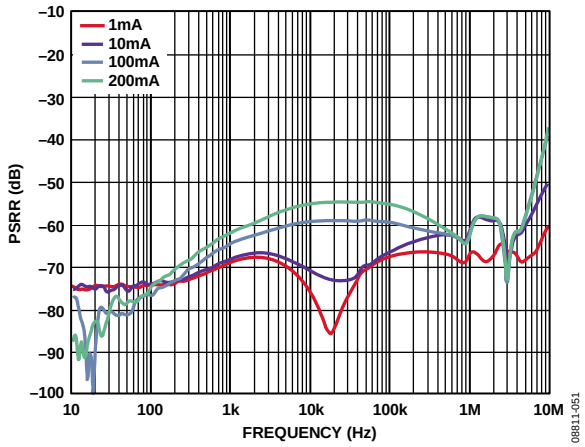

Figure 52. LDO2 PSRR Across Output Load, VIN3 = 5 V, VOUT3 = 3.3 V

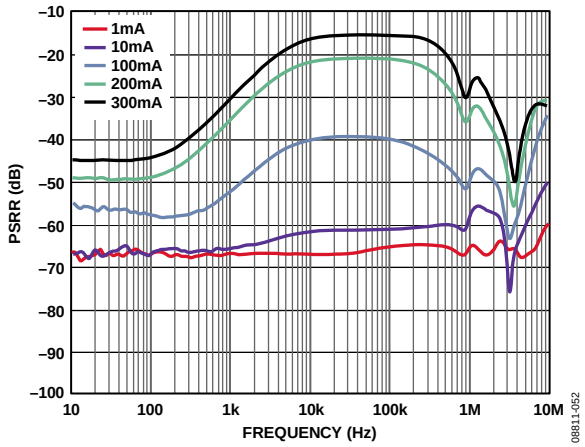

Figure 53. LDO2 PSRR Across Output Load, VIN3 = 3.6 V, VOUT3 = 3.3 V

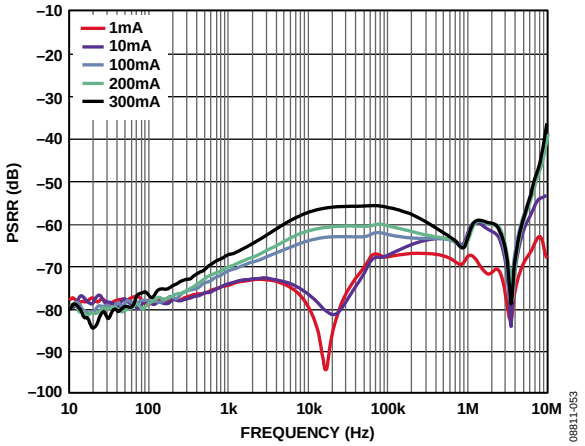

Figure 54. LDO1 PSRR Across Output Load, VIN2 = 5.0 V, VOUT2 = 1.5 V

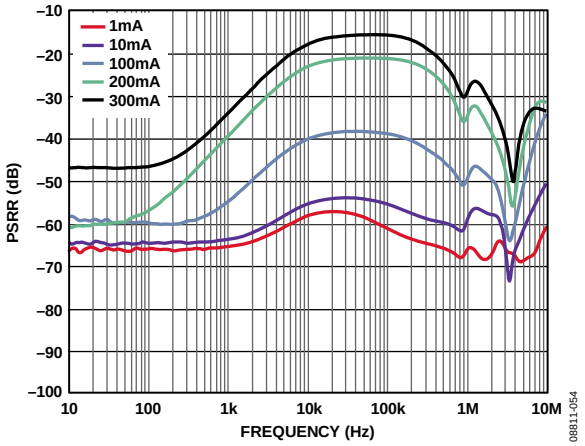

Figure 55. LDO1 PSRR Across Output Load, VIN2 = 1.8 V, VOUT2 = 1.5 V

THEORY OF OPERATION

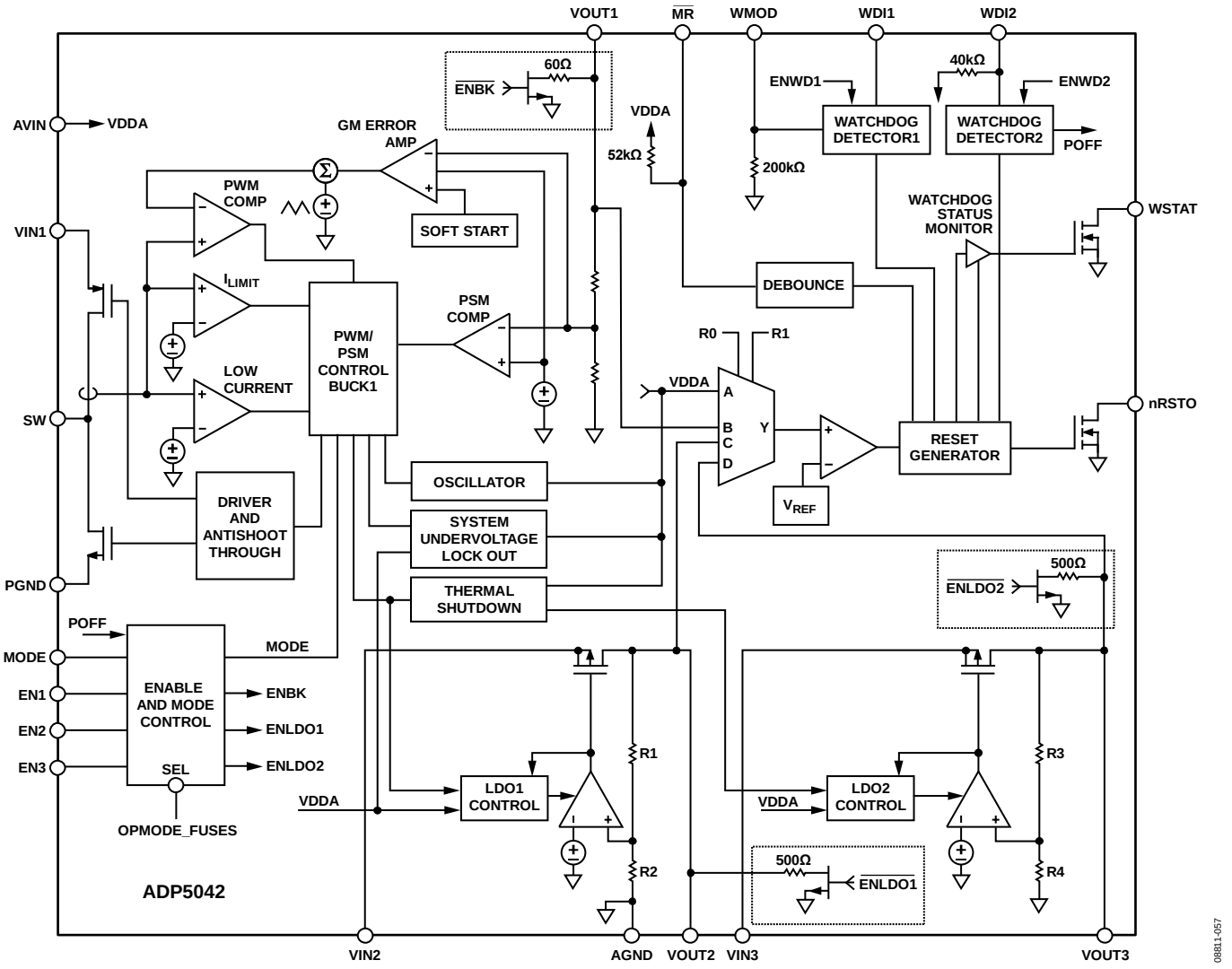

Figure 56. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5042 is a micro power management unit (micro PMU) combing one step-down (buck) dc-to-dc convertor, two low dropout linear regulators (LDOs), and a supervisory circuit, with dual watchdog, for processor control. The regulators are activated by a logic level high applied to the respective EN pin. The EN1 controls the buck regulator, the EN2 controls LDO1, and the EN3 controls LDO2. The ADP5042 has factory programmed output voltages and reset voltage threshold. Other features available in this device are the mode pin to control the buck switching operation, a status pin informing the external processor which watchdog caused a reset and push-button reset input.

When a regulator is turned on, the output voltage is controlled through a soft start circuit to avoid a large inrush current due to the discharged output capacitors.

The buck regulator can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the switching frequency of the buck is always constant and does not change with the load current. If the MODE pin is at logic low level, the switching regulator operates in auto PWM/PSM mode. In this mode, the regulator operates at fixed PWM frequency when the load current is above the power saving current threshold. When the load current falls below the power saving current threshold, the regulator enters power saving mode, where the switching occurs in bursts. The burst repetition is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off the buck and the LDOs. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the buck and LDOs do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, soft start is initiated.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated in the system. If the input voltage on AVIN drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck channel, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can select device models with a UVLO set at a higher level, suitable for 5 V applications. For these models, the device hits the turn-off threshold when the input supply drops to 3.65 V typical.

Enable/Shutdown

The ADP5042 has individual control pins for each regulator. A logic level high applied to the ENx pin activates a regulator, a logic level low turns off a regulator.

When regulators are turned off after a Watchdog 2 event (see the Watchdog 2 Input section), the reactivation of the regulator occurs with a factory programmed order (see Table 9). The delay between the regulator activation (t_{D1}, t_{D2}) is 2 ms.

Table 9. ADP5042 Regulators Sequencing

REGSEQ[1:0]		Regulators Sequence (First to Last)
0	0	LDO1 → LDO2 → Buck
0	1	Buck → LDO1 → LDO2
1	0	LDO1 → Buck → LDO2
1	1	No sequence, all regulators start at same time

BUCK SECTION

The buck uses a fixed frequency and high speed current mode architecture. The buck operates with an input voltage of 2.3 V to 5.5 V.

Control Scheme

The buck operates with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency but shift to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the buck operates at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The buck smoothly transitions to PSM operation when the load current decreases below the PSM current threshold. When the buck enters power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level that is approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

PSM Current Threshold

The PSM current threshold is set to 100 mA. The buck employs a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to and exit from the PSM. The PSM current threshold is optimized for excellent efficiency over all load currents.

Short-Circuit Protection

The buck includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Soft Start

The buck has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

The buck has protection circuitry to limit the amount of positive current flowing through the PFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits

the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

With a dropping input voltage or with an increase in load current, the buck may reach a limit where, even with the PFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

LDO SECTION

The ADP5042 contains two LDOs with low quiescent current, low dropout linear regulator, and provides up to 300 mA of output current. Drawing a low 15 µA quiescent current (typical) at no load makes the LDO ideal for battery-operated portable equipment.

The LDO operates with an input voltage range of 1.7 V to 5.5 V. The wide operating range makes these LDOs suitable for cascading configurations where the LDO supply voltage is provided from the buck regulator.

The LDOs also provide high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with just a small 1 µF ceramic input and output capacitor.

LDO2 is optimized to supply analog circuits because it offers better noise performance compared to LDO1. LDO1 should be used in applications where noise performance is not critical.

Internally, one LDO consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, reducing the current flowing to the output.

SUPERVISORY SECTION

The ADP5042 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a dual-watchdog timer.

Reset Output

The ADP5042 has an active-low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail that is no higher than 6 V. The resistor should comply with the logic low and logic high voltage level requirements of the microprocessor while supplying input current and leakage paths on the nRSTO pin. A 10 kΩ resistor is adequate in most situations.

The reset output is asserted when the monitored rail is below the reset threshold (V_{TH}), when WDI1 or WDI2 is not serviced within the watchdog timeout period (t_{WD1} and t_{WD12}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold or after the watchdog timer times out. Figure 57 illustrates the behavior of the reset output, nRSTO, and it assumes that VOUT2 is selected as the rail to be monitored and supplies the external pull-up connected to the nRSTO output.

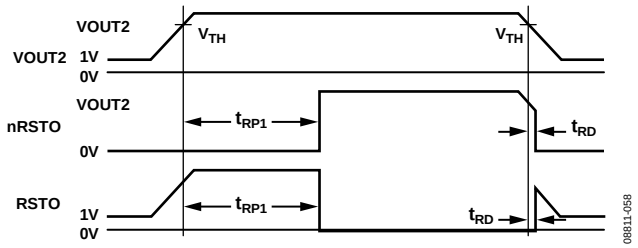

Figure 57. Reset Timing Diagram

The reset threshold voltage and the sensed rail (VOUT1, VOUT2, VOUT3, or AVIN) are factory programmed. Refer to Table 16 for a complete list of the reset thresholds available for the ADP5042.

When monitoring the input supply voltage, AVIN, if the selected reset threshold is below the UVLO level (factory programmable to 2.25 V or 3.6 V) the reset output, nRSTO, is asserted low as soon as the input voltage falls below the UVLO threshold. Below the UVLO threshold, the reset output is maintained low down to ~1 V VIN. This it to ensure that the reset output is not released when there is sufficient voltage on the rail supplying a processor to restart the processor operations.

Manual Reset Input

The ADP5042 features a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kΩ, internal pull-up, connected to AVIN, so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

Watchdog 1 Input

The ADP5042 features a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI1), which detects pulses as short as 80 ns. If the timer counts through the preset watchdog timeout period (t_{WD1}), reset is asserted. The microprocessor is required to toggle the WDI1 pin to avoid being reset. Failure of the microprocessor to toggle WDI1 within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

As well as logic transitions on WDI1, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on the monitored rail. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts. Watchdog 1 timer can be disabled by leaving WDI1 floating or by three-stating the WDI1 driver. The pin WMOD controls the Watchdog 1 operating mode. If WMOD is set to logic level low, Watchdog 1 is enabled as long as WDI1 is not in three-state. If WMOD is set to logic level high, Watchdog 1 is always active and cannot be disabled by a three-state condition. WMOD input has an internal 200 kΩ pull-down resistor.

Watchdog 1 timeout is factory set to two possible values as indicated in Table 18.

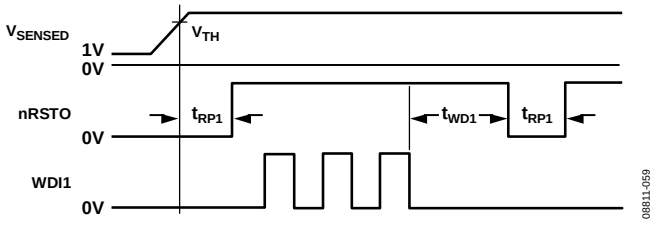

Figure 58. Watchdog 1 Timing Diagram

Watchdog 2 Input

The ADP5042 features an additional watchdog timer that monitors microprocessor activity in parallel to the first watchdog with a much longer timeout. This provides additional security and safety in case Watchdog 1 is incorrectly strobed. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI2), which detects pulses as short as 8 µs. If the timer counts through the preset watchdog timeout period (t_{WD2}), reset is asserted, followed by a power cycle of all regulators . The microprocessor is required to toggle the WDI2 pin to avoid being reset and powered down. Failure of the microprocessor to toggle WDI2 within the timeout period, therefore, indicates a code execution error, and the reset output nRSTO is forced low for t_{RP2}. Then, all the regulators are turned off for the t_{POFF} time. After the t_{POFF} period, the regulators are re-activated according to a predefined sequence (see Table 9). Finally, the reset line (nRSTO) is asserted for t_{RP1}. This guarantees a clean power-up of the system and proper reset.

As well as logic transitions on WDI2, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on the VTH monitored rail which can be factory programmable between VOUT1, VOUT2, VOUT3, and AVIN (see Table 21). When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts.

Watchdog 2 timeout is factory set to seven possible values as indicated in Table 19. One additional option allows Watchdog 2 to be factory disabled.

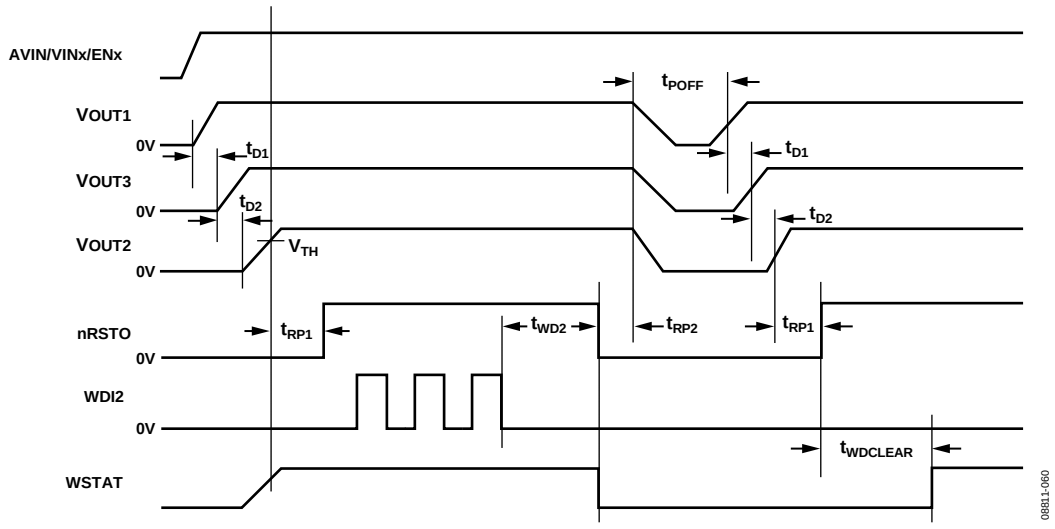

Figure 59. Watchdog 2 Timing Diagram (Assuming That VOUT2 Is the Monitored Rail)

Watchdog Status Indicator

In addition to the dual watchdog function, the ADP5042 features a watchdog status monitor available on the WSTAT pin. This pin can be queried by the external processor to determine the origin of a reset. WSTAT is an open-drain output.

WSTAT outputs a logic level depending on the condition that has generated a reset. WSTAT is forced low if the reset was generated because of a Watchdog 2 timeout. WSTAT is pulled high, through external pull-up, for any other reset cause (Watchdog 1 timeout, power failure or monitored voltage below threshold). The status monitor is automatically cleared (set to logic level high) 10 seconds after the nRSTO low to high transition ($t_{WDCLEAR}$), processor firmware must be designed being able to read the WSTAT flag before $t_{WDCLEAR}$ expiration after a Watchdog 2 reset.

The WSTAT flag is not updated in the event of a reset due to a low voltage threshold detection or Watchdog 1 event occurring within 10 seconds after nRSTO low to high transition. In this situation, WSTAT maintains the previous state (see state flow in Figure 60).

The external processor can further distinguish a reset caused by a Watchdog 1 timeout from a power failure, status monitor WSTAT indicating a high level, by implementing a RAM check or signature verification after reset. A RAM check or signature failure indicates that a power failure has occurred, whereas a RAM check or signature validation indicates that a Watchdog 1 timeout has occurred.

Table 10 shows the possible watchdog decoded statuses.

Table 10. Watchdog Status Decoding

WSTAT	RAM CHECKSUM	RESET ORIGIN
High	Failed	Power failure
High	Ok	Watchdog 1
Low	Don't care	Watchdog 2

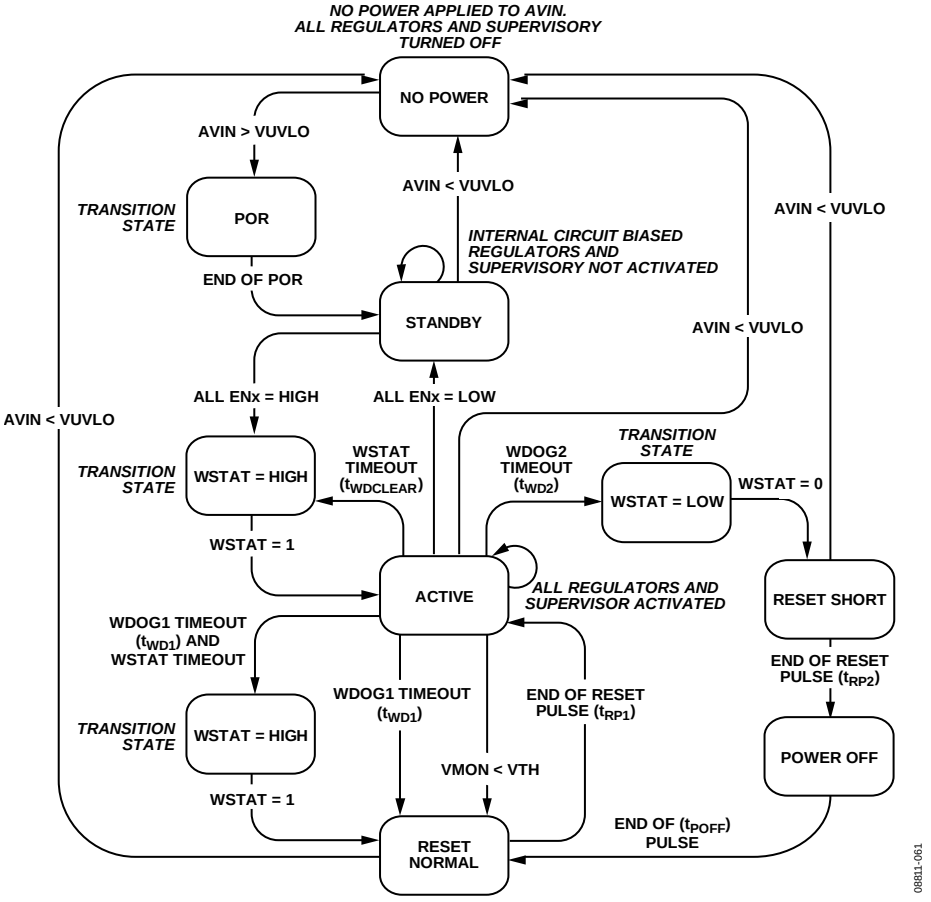

Figure 60. ADP5042 State Flow

APPLICATIONS INFORMATION

BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 66.

Inductor

The high switching frequency of the ADP5042 buck allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Suggested inductors are shown in Table 11.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck is high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low EMI.

Table 11. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
Murata	LQM18FN1R0M00B	1.6 × 0.8 × 0.8	150	26
Taiyo Yuden	CBMF1608T1R0M	1.6 × 0.8 × 0.8	290	90
Coilcraft	EPL2014-102ML	2.0 × 2.0 × 1.4	900	59
TDK	GLFR1608T1R0M-LR	1.6 × 0.8 × 0.8	230	80
Coilcraft	0603LS-102	1.8 × 1.69 × 1.1	400	81
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1350	85

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.2481 µF at 1.8 V, as shown in Figure 61.

Substituting these values in the equation yields

$$C_{EFF} = 9.2481\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.0747\ \mu F$$

To guarantee the performance of the buck, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

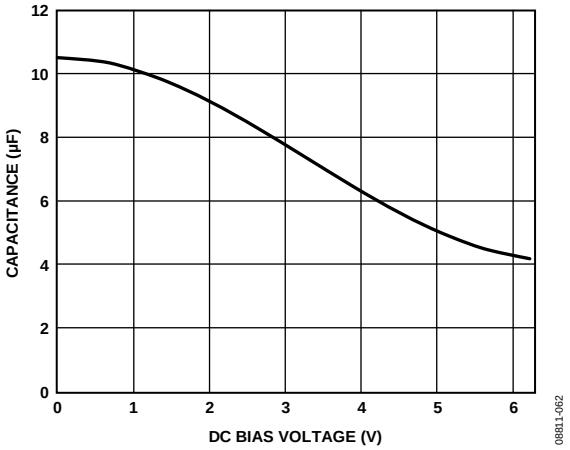

Figure 61. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

Table 12. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Panasonic	X5R	ECJ1VB0J106M	0603	6.3

The buck regulator requires 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition in and out the PWM/PSM modes. In certain applications, where the buck regulator powers a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode (see Figure 62).

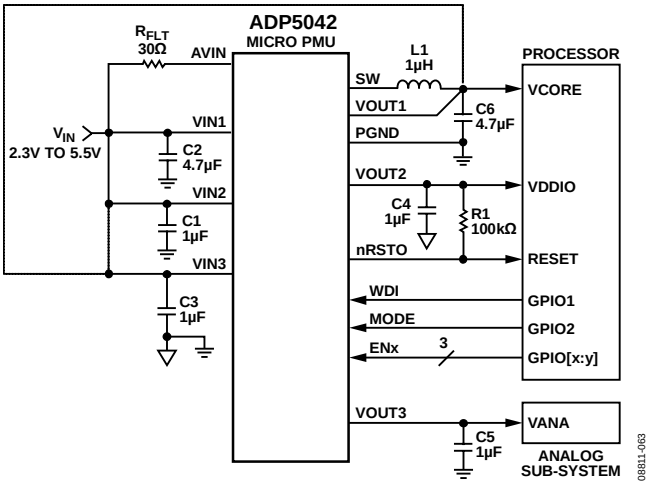

Figure 62. Processor System Power Management with PSM/PWM Control

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the buck as possible. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. A list of suggested capacitors is shown in Table 13.

Table 13. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

LDO CAPACITOR SELECTION

Output Capacitor

The ADP5042 LDOs are designed for operation with small, space-saving ceramic capacitors, but they function with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP5042. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5042 to large changes in load current.

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN2 and VIN3 to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance is encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

Table 14. Suggested 1.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155R61A105ME15	0402	10.0
TDK	X5R	C1005JB0J105KT	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP5042 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 63 depicts the capacitance vs. voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

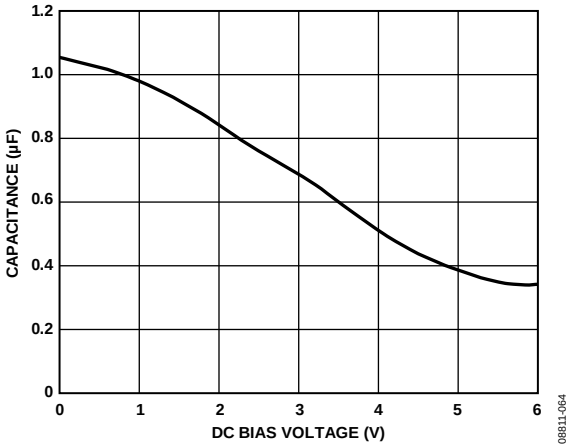

Figure 63. Capacitance vs. Voltage Characteristic

Use the following equation to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V as shown in Figure 63.

Substituting these values into the following equation yields:

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5042, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

SUPERVISORY SECTION

Watchdog 1 Input Current

To minimize watchdog input current (and minimize overall power consumption), leave WDI1 low for the majority of the watchdog timeout period. When driven high, WDI1 can draw as much as 25 µA. Pulsing WDI1 low-to-high-to-low at a low duty cycle reduces the effect of the large input current. When WDI1 is unconnected and WMOD is set to logic level low, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

Negative-Going V_{CC} Transients

To avoid unnecessary resets caused by fast power supply transients, the ADP5042 is equipped with glitch rejection circuitry. The typical performance characteristic in Figure 64 plots the monitored rail voltage, V_{TH}, transient duration vs. the transient magnitude. The curve shows combinations of transient magnitude and duration for which a reset is not generated for a 2.93 V reset threshold part. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated.

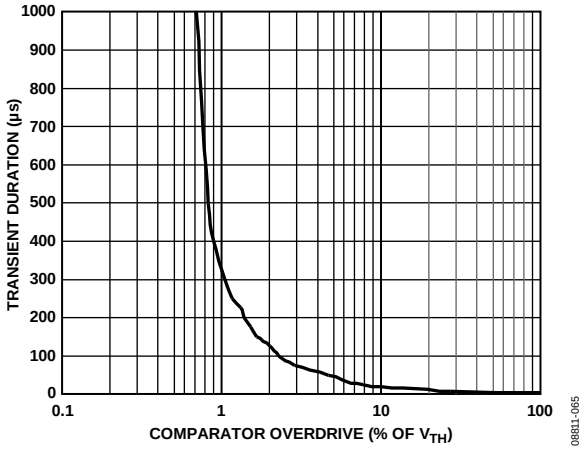

Figure 64. Maximum V_{TH} Transient Duration vs. Reset Threshold Overdrive

Watchdog Software Considerations

In implementing the watchdog strobe code of the microprocessor, quickly switching WDI1 low to high and then high to low (minimizing WDI1 high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-to-high-to-low WDI1 pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI1. A more effective coding scheme for detecting this error involves

using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI1 is set high. The subroutine sets WDI1 low when it is called. If the program executes without error, WDI1 is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI1 is kept low, the watchdog times out, and the microprocessor is reset (see Figure 65).

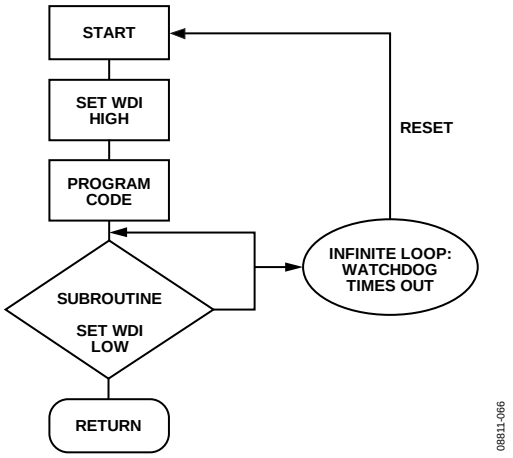

Figure 65. Watchdog Flow Diagram

The second watchdog, refreshed through the WDI2 pin, is useful in applications where safety is a very critical factor and the system must recover from unwanted operations, for example, a processor stuck in a continuous loop where Watchdog 1 is kept refreshed or environmental conditions that may unset or damage the processor port controlling the WDI1 pin. In the event of a Watchdog 2 timeout, the ADP5042 power cycles all the supplied rails to guarantee a clean processor start.

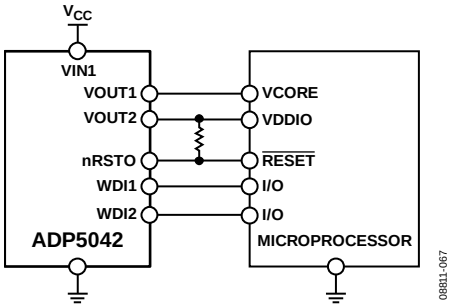

Figure 66. Typical Applications Circuit

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5042 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

EVALUATION BOARD SCHEMATICS AND ARTWORK

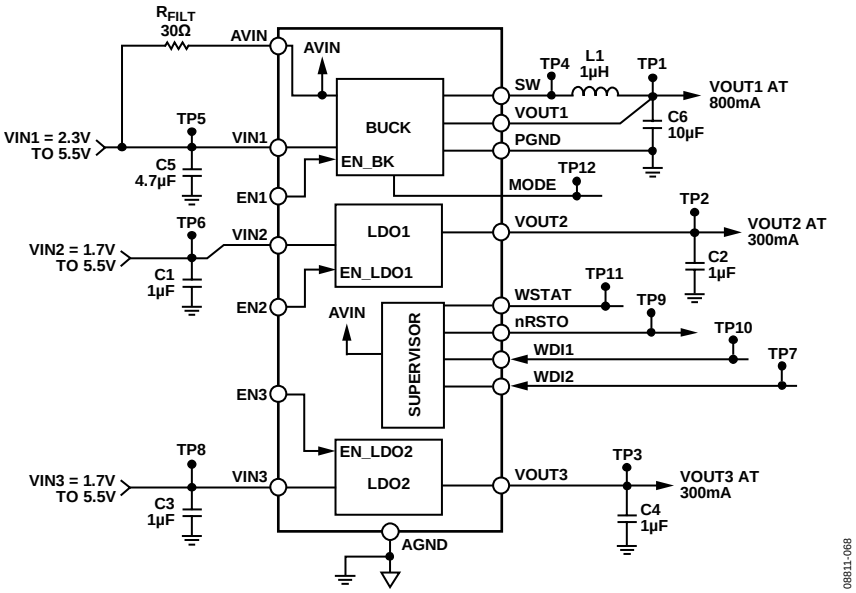

Figure 67. Evaluation Board Schematic

SUGGESTED LAYOUT

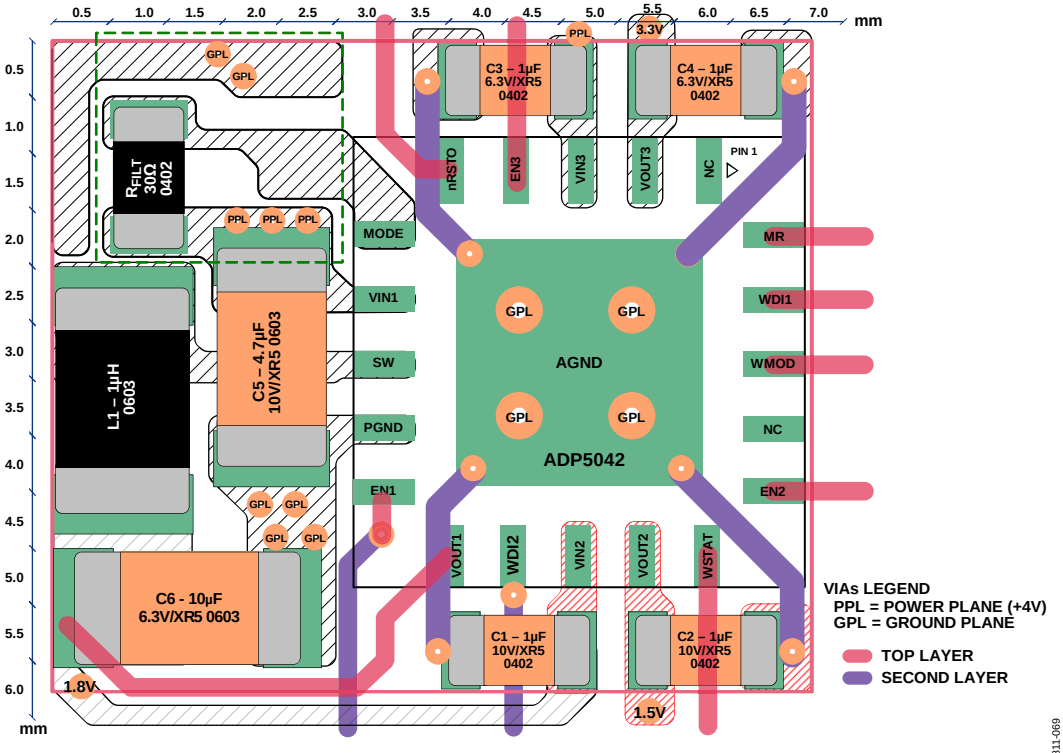

Figure 68. Layout

BILL OF MATERIALS

Table 15.

Reference	Value	Part Number	Vendor	Package
C1, C2, C3, C4	1 µF, X5R, 6.3 V	LMK105BJ105MV-F	Taiyo Yuden	0402
C5	4.7 µF, X5R, 10 V	LMK107BJ475MA-T	Taiyo Yuden	0603
C6	10 µF, X5R, 6.3 V	JMK107BJ106MA-T	Taiyo Yuden	0603
R_{FILT}	30 Ω			0201/0402
L1	1 µH, 0.09 Ω, 290 mA	BRC1608T1R0M	Taiyo Yuden	0603
	1 µH, 0.08 Ω, 230 mA	GLFR1608T1R0M-LR	TDK	0603
IC1	3-regulator micro PMU	ADP5042	Analog Devices	20-Lead LFCSP

APPLICATION DIAGRAM

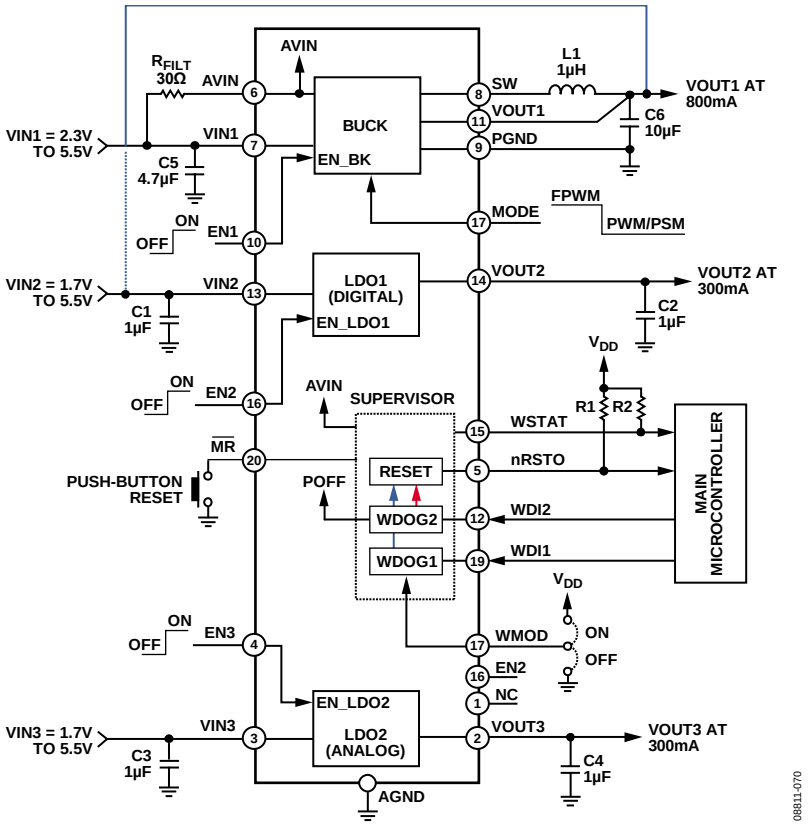

Figure 69. Application Diagram

FACTORY PROGRAMMABLE OPTIONS

Table 16. Reset Voltage Threshold Options[1]

	T_A = +25°C			T_A = −40°C to +85°C		
Selection	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
111 (For VIN = 5 V − 6%)		4.630			4.700	V
110 (For VOUT = 3.3 V)	3.034	3.080	3.126	3.003	3.157	V
101 (For VOUT = 3.3 V)	2.886	2.930	2.974	2.857	3.000	V
100 (For VOUT = 2.8 V)	2.591	2.630	2.669	2.564	2.696	V
011 (For VOUT = 2.8 V)	2.463	2.500	2.538	2.438	2.563	V
010 (For VOUT = 2.5 V − 6%)		2.350			2.385	V
001 (For VOUT = 2.2 V − 6%)		2.068			2.099	V
000 (For VOUT = 1.8 V − 6%)		1.692			1.717	V

Table 17. Reset Timeout Options

Selection	**Min**	**Typ**	**Max**	**Unit**
0	24	30	36	ms
1	160	200	240	ms

Table 18. Watchdog 1 Timer Options

Selection	**Min**	**Typ**	**Max**	**Unit**
0	81.6	102	122.4	ms
1	1.12	1.6	1.92	sec

Table 19. Watchdog 2 Timer Options

Selection	**Min**	**Typ**	**Max**	**Unit**
000	6	7.5	9	sec
001		Watchdog 2 disabled		
010	3.2	4	4.8	min
011	6.4	8	9.6	min
100	12.8	16	19.2	min
101	25.6	32	38.4	min
110	51.2	64	76.8	min
111	102.4	128	153.6	min

Table 20. Power-Off Timing Options

Selection	**Min**	**Typ**	**Max**	**Unit**
0	140	200	280	ms
1	280	400	560	ms

Table 21. Reset Sensing Options

Selection	**Monitored Rail**
00	VOUT1 pin
01	VOUT2 pin
10	VOUT3 pin
11	AVIN[1] pin

[1] When monitoring AVIN, the reset threshold selected, by fuse option or by the external resistor divided, must be higher than the UVLO threshold (2.25 V or 3.6 V).

OUTLINE DIMENSIONS

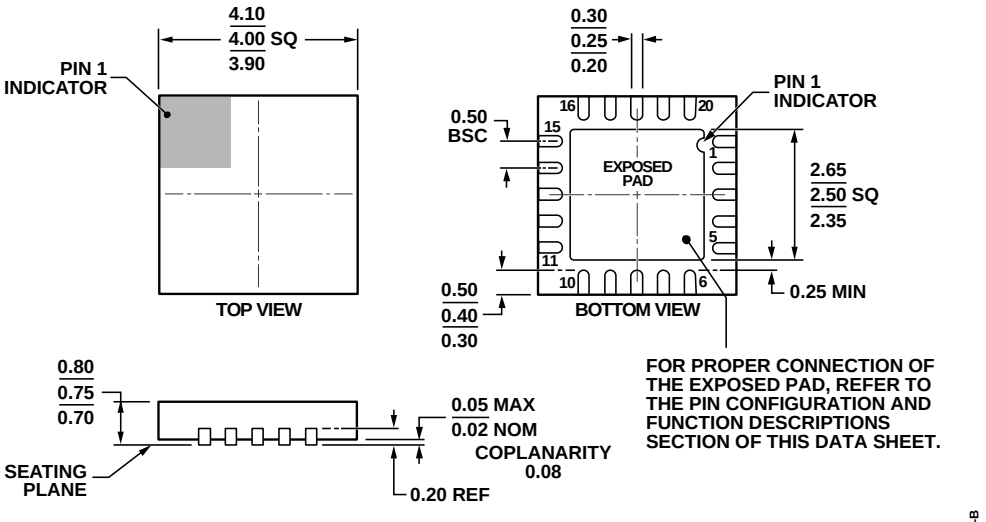

Figure 70. 20-Lead, Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Regulator Settings	Supervisory Settings	Temperature Range	Package Description	Package Option
ADP5042ACPZ-1-R7	VOUT1 = 1.8 V VOUT2 = 1.5 V VOUT3 = 3.3 V UVLO = 2.2 V Sequencing: LDO1, LDO2, buck	WD1 t_{OUT} = 1.6 sec WD2 t_{OUT} = 128 min Reset t_{OUT} = 200 ms POFF = 200 ms VTH Sensing = VOUT3, 2.93 V	T_J = −40°C to +125°C	20-Lead, Lead Frame Scale Package [LFCSP_WQ]	CP-20-10
ADP5042ACPZ-2-R7	VOUT1 = 1.5 V VOUT2 = 1.8 V VOUT3 = 3.3 V UVLO = 2.2 V Sequencing: LDO1, LDO2, buck	WD1 t_{OUT} = 1.6 sec WD2 t_{OUT} = 128 min Reset t_{OUT} = 200 ms POFF = 200 ms VTH Sensing = VOUT3, 2.93 V	T_J = −40°C to +125°C	20-Lead, Lead Frame Scale Package [LFCSP_WQ]	CP-20-10
ADP5042CP-1-EVALZ				Evaluation Board	
ADP5042CP-2-EVALZ				Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

NOTES

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