

Description

The ISL9106EVAL1Z is an evaluation kit for the ISL9106 1.6MHz 1.2A low quiescent current, high efficiency integrated step-down regulator. The ISL9106 is capable of delivering up to 1.2A output current with an output voltage range of 0.8V to $\sim V_{IN}$. The output voltage is set by two voltage divider resistors of R_1 and R_2 on the board. The default output voltage is set to be 1.6V on the evaluation board.

The complete ISL9106 regulator is located at the center of the board. On the left side of the board are the connectors for the input power source (VIN and GND). The output connectors are located on the right side (VO and GND). The other two test points are for the PG and RSI signals respectively, as labelled on the board. The RSI input needs either be driven to a low or a high logic input (Please refer to the ISL9106 datasheet, FN6509 for more details regarding RSI function). **Do not leave the RSI input signal floating.** The open-drain PG signal is pulled up to the V_{IN} through a 100k Ω resistor (R_3). Jumper JP1 allows the user to enable or disable the IC. Jumper JP2 is the mode selection input. **Do not leave the EN or the MODE signal floating.** The evaluation board also offers one oscilloscope probe tip connector connected to SW pin to minimize the switching noise during the evaluation. One test point (labeled as FB) is connected to the FB pin on the board in order to monitor the FB voltage.

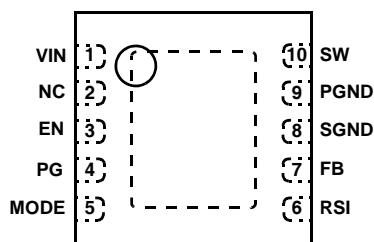
The evaluation board schematic, layout and bill-of-materials (BOM) can be found at the end of this application note.

Ordering Information

PART NUMBER	DESCRIPTION
ISL9106EVAL1Z	Evaluation Board for ISL9106

Pinout

ISL9106
10 LD DFN
TOP VIEW



Features

- A Complete Evaluation Platform for ISL9106
- Convenient Jumpers for Enable/Disable, Operation Mode Selection
- Pb-Free Plus (RoHS Compliant)

Recommended Equipment

The following instruments are recommended for testing:

- Power supplies: DC 10V/5A
- Electronic load: capable of sinking current up to 3A
- Multimeters
- Function generator
- Oscilloscope
- Cables and wires

Specifications

Table 1 shows the recommended operation conditions for using the ISL9106EVAL1Z.

TABLE 1. RECOMMENDED OPERATION CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Input Voltage	2.7	-	5.5	V
Output Voltage (Note)	-	1.6	-	V
Maximum Output Current	1.2	-	-	A

NOTE: The output voltage can be set to other values by changing the R_1 , R_2 values, $V_{OUT} = 0.8V * (1 + R_2/R_1)$. Refer to ISL9106 datasheet for some recommended R_1 , R_2 and C_3 values for different output voltages.

Evaluation Board Setup

The following are steps for setting up the evaluation board:

1. Connect Jumper JP1 at the position of "Enable" to enable the device. Connect JP1 at the position of "Disable" will disable the device.
2. Connect Jumper JP2 either at the position of "SKIP" or "Forced PWM". With JP2 connected at the position of "SKIP", the device enters skip mode under light load condition; with JP2 connected at the position of "FORCED PWM", the device always operates under PWM mode regardless of the load condition.
3. Connect the RSI input to either ground or VIN. Do not leave it floating. Please refer to the ISL9106 datasheet, FN6509 for more details regarding the function of RSI.
4. Connect a DC power supply with voltage range of 2.7V to $\sim 5.5V$ between VIN and GND connectors. Make sure the power supply has enough supply current capability. Do not adjust the V_{IN} higher than the recommended maximum supply voltage (5.5V).
5. Connect the output to a load (resistor or electronic load).
6. Turn on the input power supply and evaluate the device.

ISL9106EVAL1Z Schematic

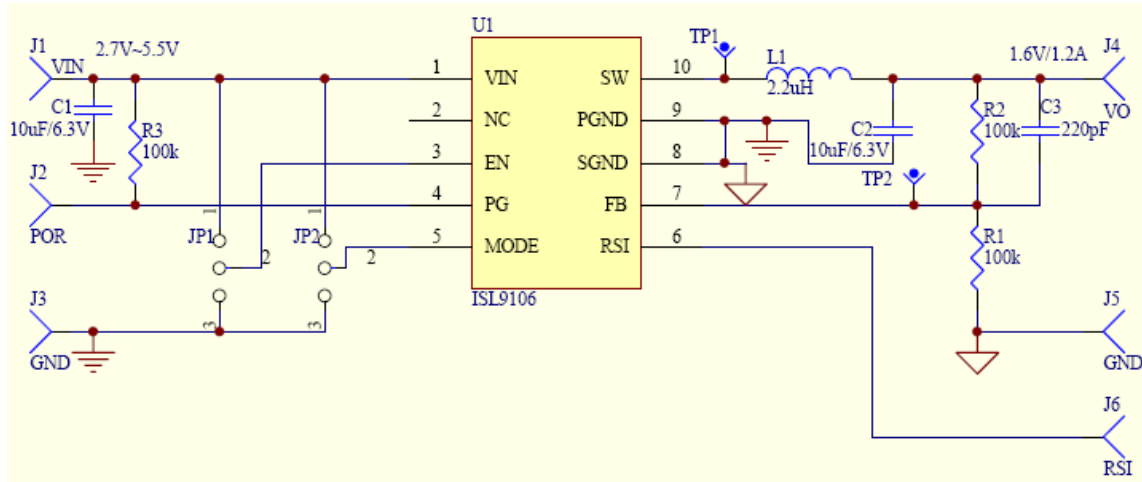


FIGURE 1. ISL9106EVAL1Z SCHEMATIC

ISL9106EVAL1Z Bill of Materials (BOM)

ITEM	QTY	REFERENCE	PART DESCRIPTION	PCB FOOTPRINT	PART NUMBER	VENDOR
1	1	U1	ISL9106	3x3 10 Ld DFN	ISL9106	Intersil
2	1	C1	Capacitor, SMD, 10µF/6.3V, 10%, X5R	0805	GRM21BR60J106KE19L	Murata
3	1	C2	Capacitor, SMD, 10µF/6.3V, 10%, X5R	0805	GRM21BR60J106KE19L	Murata
4	1	C3	Capacitor, SMD, 220pF/50V, 10%, X7R	0603	GRM188R71H221KA01D	Murata
5	3	R1, R2, R3	Resistor, SMD, 100kΩ, 1%, 0.1W	0603	RC0603FR-07100KL	Yageo
6	1	L1	Inductor, 2.2µH	3.2mm x 3.2mm	CDRH2D14NP-2R2NC	Sumida
7	6	VIN, VO, PG, RSI, GND (x2)	Turret Terminal Pin	-	3156-1-00-15-00-00-08-0	Mill-Max
8	1	TP1	Scope Probe Test Point	-	131503100	Tektronix
9	1	TP2	Test Point, Yellow	-	5014	Keystone Electronics
10	2	JP1, JP2	Connect Header, 1x3	-	68000-236-1X3	BERG/FCI

PCB Layout

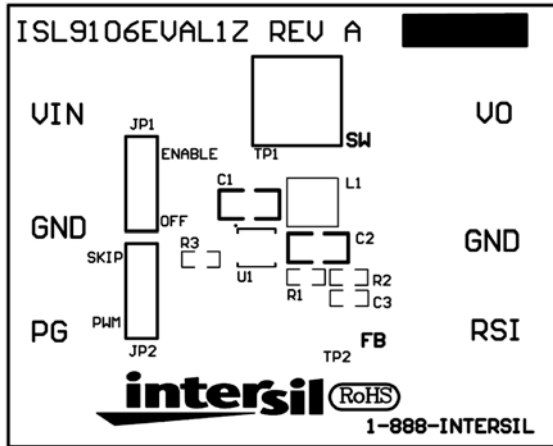


FIGURE 2. SILK LAYER

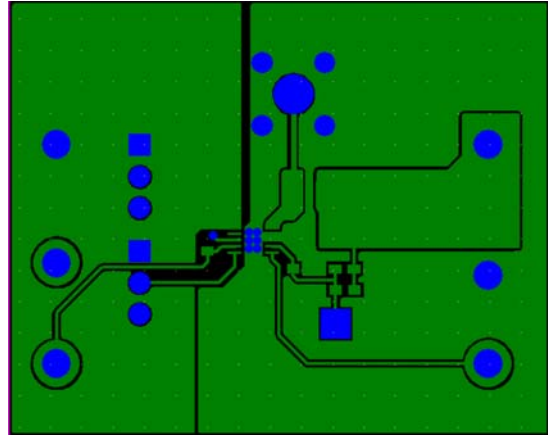


FIGURE 3. TOP LAYER

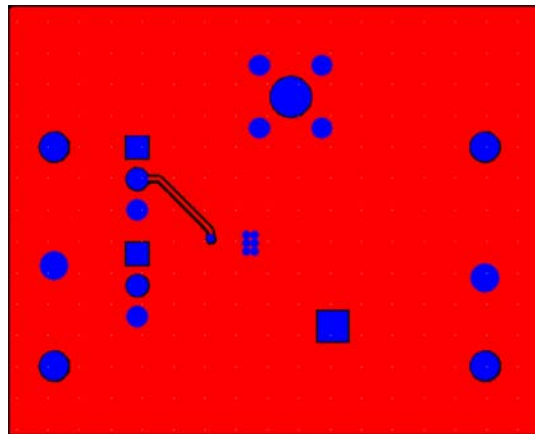


FIGURE 4. BOTTOM LAYER

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

For information regarding Intersil Corporation and its products, see www.intersil.com